

PERICOM



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1995

***Pericom Semiconductor Corporation
High Performance
CMOS/BiCMOS
Data Book***



Pericom Semiconductor Corporation

1995

High Performance

CMOS/BiCMOS

Data Book

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 - b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

Pericom Semiconductor Corporation is dedicated to providing logic solutions for critical bottlenecks in high-performance systems. Employing 0.8 and 0.6 micron CMOS and BiCMOS technologies, Pericom Semiconductor provides world class logic, clock and mixed signal products. This product line catalog demonstrates the superior performance levels of PMT with detailed information on Pericom Semiconductor's leading edge products. In almost all cases, these products are in full production. In a few instances, the products are in limited production (designated by "**Preliminary**") or will be introduced in the near future (designated by "**Advance Information**").

Pericom Semiconductor offers products that, in every case, provide the designer with leading edge cost-effective solutions. These product families consist of:

- *World's fastest FCT Bus Interface Logic with minimum propagation delays down to 3.2 ns*
- *High-speed clock distribution series including PLL implementation for high clock rates*
- *Full line of fast switching, extremely low impedance Bus Switches*
- *Wide architecture 16-bit FCT logic family in innovative space savings package*
- *Low voltage (3.3V Vcc) high-performance 16-bit FCT and LPT logic families*
- *Frequency Synthesizer Products that provide a wide number of PLL generated output frequencies for personal computer applications*
- *Active Token Ring Hub fully integrated, high-performance mixed signal solution to hub signal conditioning and skew reduction*

Pericom Semiconductor is dedicated to extensive new product development, thereby assuring our customers with a broad base of solutions to system designs.

Thank you for your support and continued interest in Pericom Semiconductor's products.

PERICOM QUALITY

Pericom supports the Quality Systems and Management concepts of the ISO-9000 series of international standards for quality. A corporate Quality Policy (detailed below) has been established that is the basis of our commitment to maintain a world class quality supplier status. Adhering to this policy is required for all employees, as Quality is not the responsibility of any one person or group; it is shared by each and every employee.

In recognition of our commitment, Pericom completed and passed an ISO-9001 Registration Assessment Audit with Underwriter's Laboratories (UL) in January, 1995.

Quality Policy:

Pericom will deliver only products and services that conform to customer requirements. We shall perform the job correctly the first time, emphasizing constant improvements in the quality of our work.

"Pericom will deliver..." - delivery, not just intentions, is one of the key measures of Pericom's commitment to deliver a quality product to customers.

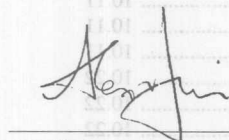
"...only products and services..." quality performance is not limited to physical products; sending a letter without spelling errors, or promptly and politely answering a telephone are services which demand our best quality.

"...that conform to customer requirements..." - a clear understanding of all requirements are needed before one can deliver quality products or services. This also signifies mutual agreement, with clear, two-way communications, which applies to customers within as well as outside the company. The entire Pericom team understands that each customer has a set of requirements and expectations that must be met.

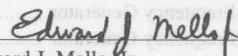
"We shall perform the job correctly the first time..." - doing it correctly means meeting agreements, that quality improvement measures are driven to determine the source of defects and preventing those defects from reoccurring. The continual process of preventing defects will drive down the costs we and our customer's experience, because costs associated with rework, redesign, etc., are dollars taken from being price competitive.

"...emphasizing constant improvements in the quality of our work..." - each employee must strive to find better, faster, more economical ways to perform their job, to ensure that quality continues to improve along with cost effectiveness.

Further information on Pericom Quality and Reliability is available upon request.



Alex Hui
President & CEO



Edward J. Mello, Jr.
Quality System Manager

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PI6C9155W-03	20-Pin CPU Frequency Generator	10.11
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PI74FCT162245T	16-Bit Bidirectional Transceiver with Balanced Output Drives	3.11
PI74FCT162373T	16-Bit Transparent Latch with Balanced Output Drives	3.16
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PI74FCT162500T	18-Bit Registered Transceiver with Balanced Output Drives	3.26
PI74FCT162501T	18-Bit Registered Transceiver with Balanced Output Drives	3.32
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PI74FCT2543T	Latched Transceivers with 25 Ohm Series Output Resistor	2.81
PI74FCT2573T	Octal Transparent Latches with 25 Ohm Series Output Resistor	2.59
PI74FCT257T	Quad 2-Input Multiplexer	2.36
PI74FCT2645T	Octal Bidirectional Transceivers with 25 Ohm Series Output Resistor	2.47
PI74FCT2646T	Octal Registered Transceivers with 25 Ohm Series Output Resistor	2.89
PI74FCT2652T	Octal Registered Transceivers with 25 Ohm Series Output Resistor	2.89
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PI74FCT280T	9-Bit Parity Generator/Checker	2.55
PI74FCT2821T	Bus Interface Registers with 25 Ohm Series Output Resistor	2.96
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PI74FCT2827T	10-Bit Buffer with 25 Ohm Series Output Resistor	2.103
PI74FCT2841T	Bus Interface Latches with 25 Ohm Series Output Resistor	2.108
PI74FCT373T	Octal Transparent Latches	2.59
PI74FCT374T	Octal D Registers (3-State)	2.65
PI74FCT377T	Octal D Flip-Flop with Clock Enable	2.71
PI74FCT399T	Quad Dual-Port Register	2.74
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PI74FCT645T	Octal Bidirectional Transceivers	2.47
PI74FCT646T	Octal Registered Transceivers	2.89
PI74FCT648T	Octal Registered Transceivers	2.89
PI74FCT651T	Octal Registered Transceivers	2.89
PI74FCT652T	Octal Registered Transceivers	2.89
PI74FCT821T	Bus Interface Registers	2.96
PI74FCT823T	Bus Interface Registers	2.96
PI74FCT825T	Bus Interface Registers	2.96
PI74FCT827T	10-Bit Buffers	2.103
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PI74FCT841T	Bus Interface Latches	2.108
PI74FCT843T	Bus Interface Latches	2.108
PI74FCT845T	Bus Interface Latches	2.108
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PI74FCT863T	Bus Transceivers	2.115

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STANDARD 5V FCT LOGIC PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI29FCT52T	Registered Transceivers	24	-15/64 mA	6.3	2.1
PI29FCT53T	Registered Transceivers	24	-15/64 mA	6.3	2.1
PI29FCT520T	Multilevel Pipeline Register	24	-15/48 mA	7.5	2.7
PI29FCT521T	Multilevel Pipeline Register	24	-15/48 mA	7.5	2.7
PI74FCT132T	Quad 2-Input NAND Schmitt Trigger	14	-15/48 mA	5.0	2.12
PI74FCT138T	1-of-8 Decoder	16	-15/48 mA	5.1	2.15
PI74FCT238T	1-of-8 Decoder	16	-15/48 mA	5.0	2.15
PI74FCT139T	Dual 1-of-4 Decoder	16	-15/48 mA	5.0	2.21
PI74FCT239T	Dual 1-of-4 Decoder	16	-15/48 mA	5.0	2.21
PI74FCT151T	8-Input Multiplexer	16	-15/48 mA	5.6	2.26
PI74FCT251T	8-Input Multiplexer	16	-15/48 mA	5.6	2.26
PI74FCT153T	High-Speed CMOS Dual 4-Input Multiplexer	16	-15/48 mA	5.6	2.31
PI74FCT253T	High-Speed CMOS Dual 4-Input Multiplexer	16	-15/48 mA	5.6	2.31
PI74FCT157T	Quad 2-Input Multiplexer	16	-15/48 mA	3.9	2.36
PI74FCT257T	Quad 2-Input Multiplexer	16	-15/48 mA	4.3	2.36
PI74FCT240T	Octal Buffer/Line Drivers	20	-15/64 mA	3.6	2.41
PI74FCT241T	Octal Buffer/Line Drivers	20	-15/64 mA	3.6	2.41
PI74FCT244T	Octal Buffer/Line Drivers	20	-15/64 mA	3.6	2.41
PI74FCT540T	Octal Buffer/Line Drivers	20	-15/64 mA	3.8	2.41
PI74FCT541T	Octal Buffer/Line Drivers	20	-15/64 mA	3.8	2.41
PI74FCT245T	Octal Bidirectional Transceivers	20	-15/64 mA	3.8	2.47
PI74FCT640T	Octal Bidirectional Transceivers	20	-15/64 mA	3.7	2.47
PI74FCT645T	Octal Bidirectional Transceivers	20	-15/64 mA	3.8	2.47
PI74FCT273T	Octal D Flip-Flop with Master Reset	20	-15/64 mA	4.4	2.51
PI74FCT280T	9-Bit Parity Generator/Checker	14/16	-15/48 mA	5.3	2.55
PI74FCT373T	Octal Transparent Latches	20	-15/64 mA	3.8	2.59
PI74FCT533T	Octal Transparent Latches	20	-15/64 mA	4.2	2.59
PI74FCT573T	Octal Transparent Latches	20	-15/64 mA	3.8	2.59
PI74FCT374T	Octal D Registers (3-State)	20	-15/64 mA	4.5	2.65
PI74FCT534T	Octal D Registers (3-State)	20	-15/64 mA	4.5	2.65
PI74FCT574T	Octal D Registers (3-State)	20	-15/64 mA	4.5	2.65
PI74FCT377T	Octal D Flip-Flop with Clock Enable	20	-15/64 mA	4.5	2.71
PI74FCT399T	Quad Dual-Port Register	16	-15/48 mA	5.6	2.74
PI74FCT521T	8-Bit Identity Comparator	20	-15/48 mA	4.2	2.77
PI74FCT543T	Latched Transceivers	24	-15/64 mA	4.4	2.81
PI74FCT544T	Latched Transceivers	24	-15/64 mA	5.3	2.81
PI74FCT623T	Octal Bus Transceiver (3-State)	20	-15/64 mA	4.8	2.86
PI74FCT646T	Octal Registered Transceivers	24	-15/64 mA	4.8	2.89
PI74FCT648T	Octal Registered Transceivers	24	-15/64 mA	4.8	2.89
PI74FCT651T	Octal Registered Transceivers	24	-15/64 mA	4.8	2.89
PI74FCT652T	Octal Registered Transceivers	24	-15/64 mA	4.8	2.89
PI74FCT821T	Bus Interface Registers	24	-15/48 mA	6.0	2.96
PI74FCT823T	Bus Interface Registers	24	-15/48 mA	6.0	2.96
PI74FCT825T	Bus Interface Registers	24	-15/48 mA	6.0	2.96
PI74FCT827T	10-Bit Buffers	24	-15/48 mA	4.4	2.103

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STANDARD 5V FCT LOGIC PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74FCT828T	10-Bit Buffers	24	-15/48 mA	4.4	2.103
PI74FCT841T	Bus Interface Latches	24	-15/48 mA	5.5	2.108
PI74FCT843T	Bus Interface Latches	24	-15/48 mA	5.5	2.108
PI74FCT845T	Bus Interface Latches	24	-15/48 mA	5.5	2.108
PI74FCT861T	Bus Transceivers	24	-15/48 mA	5.5	2.115
PI74FCT863T	Bus Transceivers	24	-15/48 mA	5.5	2.115
PI74FCT864T	Bus Transceivers	24	-15/48 mA	5.5	2.115
PI74FCT890T	High-Speed Inverted Hex Driver	16/20	-32/100 mA	9.0	2.121

STANDARD 5V FCT LOGIC PRODUCTS WITH 25Ω SERIES OUTPUT RESISTOR

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74FCT2153T	Dual 4-Input Multiplexer w/25Ω Series Output Resistor	16	-15/12 mA	5.6	2.311
PI74FCT2253T	Dual 4-Input Multiplexer w/25Ω Series Output Resistor	16	-15/12 mA	5.6	2.311
PI74FCT2157T	Quad 2-Input Multiplexer w/25Ω Series Output Resistor	16	-15/12 mA	4.3	2.36
PI74FCT2257T	Quad 2-Input Multiplexer w/25Ω Series Output Resistor	16	-15/12 mA	4.3	2.36
PI74FCT2240T	Octal Buffer/Line Driver w/25Ω Series Output Resistor	20	-15/12 mA	4.1	2.41
PI74FCT2241T	Octal Buffer/Line Driver w/25Ω Series Output Resistor	20	-15/12 mA	4.1	2.41
PI74FCT2244T	Octal Buffer/Line Driver w/25Ω Series Output Resistor	20	-15/12 mA	4.8	2.41
PI74FCT2541T	Octal Buffer/Line Driver w/25Ω Series Output Resistor	20	-15/12 mA	4.1	2.41
PI74FCT2245T	Octal Bidirectional Transceivers w/25Ω Series Output Resistor	20	-15/12 mA	4.1	2.47
PI74FCT2645T	Octal Bidirectional Transceivers w/25Ω Series Output Resistor	20	-15/12 mA	4.1	2.47
PI74FCT2273T	Octal D Flip-Flop w/Master Reset w/25Ω Series Output Resistor	20	-15/12 mA	5.8	2.51
PI74FCT2373T	Octal Transparent Latch w/25Ω Series Output Resistor	20	-15/12 mA	4.2	2.59
PI74FCT2574T	Octal D Register (3-State) w/25Ω Series Output Resistor	20	-15/12 mA	5.2	2.65
PI74FCT2543T	Latched Transceivers w/25Ω Series Output Resistor	24	-15/12 mA	5.3	2.81
PI74FCT2573T	Octal Transparent Latches w/25Ω Series Output Resistor	20	-15/12 mA	5.2	2.59
PI74FCT2646T	Octal Registered Transceivers w/25Ω Series Output Resistor	24	-15/12 mA	6.3	2.89
PI74FCT2652T	Octal Registered Transceivers w/25Ω Series Output Resistor	24	-15/12 mA	6.3	2.89
PI74FCT2821T	Bus Interface Registers w/25Ω Series Output Resistor	24	-15/12 mA	6.0	2.96
PI74FCT2823T	Bus Interface Registers w/25Ω Series Output Resistor	24	-15/12 mA	6.0	2.96
PI74FCT2827T	10-Bit Buffer w/25Ω Series Output Resistor	24	-15/12 mA	5.0	2.103
PI74FCT2841T	Bus Interface Latches w/25Ω Series Output Resistor	24	-15/12 mA	6.5	2.108

DOUBLE DENSITY STANDARD 5V FCT LOGIC PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74FCT16240T	16-Bit Buffer/Line Driver	48	-32/64 mA	3.2	3.1
PI74FCT16244T	16-Bit Buffer/Line Driver	48	-32/64 mA	3.2	3.6
PI74FCT16245T	16-Bit Bidirectional Transceiver	48	-32/64 mA	3.2	3.11
PI74FCT16373T	16-Bit Transparent Latch	48	-32/64 mA	3.4	3.16
PI74FCT16374T	16-Bit Octal Register	48	-32/64 mA	3.7	3.21
PI74FCT16500T	18-Bit Registered Transceiver	56	-32/64 mA	3.8	3.26
PI74FCT16501T	18-Bit Registered Transceiver	56	-32/64 mA	3.8	3.32
PI74FCT16511T	16-Bit Registered/Latched Transceiver with Parity	56	-32/64 mA	5.7	3.38
PI74FCT16540T	16-Bit Buffer/Line Driver	48	-32/64 mA	3.6	3.46

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74FCT16541T	16-Bit Buffer/Line Driver	48	-32/64 mA	3.6	3.51
PI74FCT16543T	16-Bit Latched Transceiver	56	-32/64 mA	3.4	3.56
PI74FCT16646T	16-Bit Registered Transceiver	56	-32/64 mA	3.8	3.61
PI74FCT16652T	16-Bit Registered Transceiver	56	-32/64 mA	3.8	3.67
PI74FCT16823T	18-Bit Registers	56	-32/64 mA	4.4	3.73
PI74FCT16827T	20-Bit Buffers	56	-32/64 mA	3.2	3.79
PI74FCT16841T	20-Bit Transparent Latch	56	-32/64 mA	3.4	3.84
PI74FCT16952T	16-Bit Non-inverting Registered Transceiver	56	-32/64 mA	3.7	3.90

DOUBLE DENSITY STANDARD 5V FCT LOGIC PRODUCTS WITH BALANCED OUTPUT DRIVE

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74FCT162240T	16-Bit Buffer/Line Driver with Balanced Output Drives	48	-24/24 mA	3.2	3.1
PI74FCT162244T	16-Bit Buffer/Line Driver with Balanced Output Drives	48	-24/24 mA	3.2	3.6
PI74FCT162245T	16-Bit Bidirectional Transceiver with Balanced Output Drives	48	-24/24 mA	3.2	3.11
PI74FCT162373T	16-Bit Transparent Latch with Balanced Output Drives	48	-24/24 mA	3.4	3.16
PI74FCT162374T	16-Bit Octal Register with Balanced Output Drives	48	-24/24 mA	3.7	3.21
PI74FCT162500T	18-Bit Registered Transceiver with Balanced Output Drives	56	-24/24 mA	3.8	3.26
PI74FCT162501T	18-Bit Registered Transceiver with Balanced Output Drives	56	-24/24 mA	3.8	3.32
PI74FCT162511T	16-Bit Registered/Latched Transceiver with Parity	56	-24/24 mA	5.7	3.38
PI74FCT162540T	16-Bit Buffer/Line Driver with Balanced Output Drives	48	-24/24 mA	3.6	3.46
PI74FCT162541T	16-Bit Buffer/Line Driver with Balanced Output Drives	48	-24/24 mA	3.6	3.51
PI74FCT162543T	16-Bit Latched Transceiver with Balanced Output Drives	56	-24/24 mA	3.4	3.56
PI74FCT162646T	16-Bit Registered Transceiver with Balanced Output Drives	56	-24/24 mA	3.8	3.61
PI74FCT162652T	16-Bit Registered Transceiver with Balanced Output Drives	56	-24/24 mA	3.8	3.67
PI74FCT162823T	18-Bit Registers with Balanced Output Drives	56	-24/24 mA	4.4	3.73
PI74FCT162827T	20-Bit Buffers with Balanced Output Drives	56	-24/24 mA	3.2	3.79
PI74FCT162841T	20-Bit Transparent Latch with Balanced Output Drives	56	-24/24 mA	3.4	3.84
PI74FCT162952T	16-Bit Non-inverting Registered Transceiver with Balanced Output Drives	56	-24/24 mA	3.7	3.90

DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74FCT163240	Fast CMOS 3.3V 16-Bit Octal Buffer/Line Drivers	48	-24/24 mA	4.3	4.1
PI74FCT163244	Fast CMOS 3.3V 16-Bit Octal Buffer/Line Drivers	48	-24/24 mA	4.1	4.6
PI74FCT163245	Fast CMOS 3.3V 16-Bit Bidirectional Transceivers	48	-24/24 mA	4.1	4.11
PI74FCT163373	Fast CMOS 3.3V 16-Bit Transparent Latches	48	-24/24 mA	4.2	4.16
PI74FCT163374	Fast CMOS 3.3V 16-Bit Registers (3-State)	48	-24/24 mA	5.2	4.21

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STANDARD 3.3V LOGIC PRODUCTS WITH 5V TOLERANT I/O

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74LPT244	Fast CMOS 3.3V, 5V Tolerant I/O, 8-Bit Buffer/Line Driver	20	-24/24 mA	4.1	5.1
PI74LPT245	Fast CMOS 3.3V, 5V Tolerant I/O, 8-Bit Bidirectional Transceiver	20	-24/24 mA	4.1	5.5
PI74LPT373	Fast CMOS 3.3V, 5V Tolerant I/O, 8-Bit Transparent Latch	20	-24/24 mA	4.2	5.9
PI74LPT541	Fast CMOS 3.3V, 5V Tolerant I/O, 8-Bit Register (3-State)	20	-24/24 mA	4.1	5.13
PI74LPT573	Fast CMOS 3.3V, 5V Tolerant I/O, 8-Bit Transparent Latch	20	-24/24 mA	4.2	5.17

DOUBLE DENSITY 3.3V LOGIC PRODUCTS WITH 5V TOLERANT I/O

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI74LPT16240	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Buffer/Line Driver	48	-24/24 mA	4.3	6.1
PI74LPT16244	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Buffer/Line Driver	48	-24/24 mA	4.1	6.6
PI74LPT16245	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Bidirectional Transceiver	48	-24/24 mA	4.1	6.11
PI74LPT16373	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Transparent Latch	48	-24/24 mA	4.2	6.16
PI74LPT16374	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Register (3-State)	48	-24/24 mA	5.2	6.21
PI74LPT16501	Fast CMOS 3.3V, 5V Tolerant I/O 18-Bit Register (3-State)	56	-24/24 mA	4.6	6.26
PI74LPT16543	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Transceiver	56	-24/24 mA	5.3	6.31
PI74LPT16646	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Transceiver	56	-24/24 mA	5.4	6.36
PI74LPT16652	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Transceiver	56	-24/24 mA	5.4	6.42
PI74LPT16827	Fast CMOS 3.3V, 5V Tolerant I/O 20-Bit Buffer	56	-24/24 mA	4.4	6.48
PI74LPT16952	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Register (3-State)	56	-24/24 mA	6.3	6.53

SPECIALTY LOGIC PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI6M1010T	SIMM Decoder Chip	16/20	-15/12 mA	4.9	7.1

BUS SWITCH PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI5C3125	Quad Analog Switch with Individual Enables	14/16	—	0.25	8.1
PI5C3126	Quad Analog Switch with Individual Enables	14/16	—	0.25	8.1
PI5C3244	Bus Switch Buffer	20	—	0.25	8.5
PI5C3245	8-Bit, 2-Port Bus Switch	20	—	0.25	8.8
PI5C3251	8:1 Multiplexer/Demultiplexer	16	—	0.25	8.11
PI5C3253	Dual 4:1 Multiplexer/Demultiplexer	16	—	0.25	8.14
PI5C3257	Quad 2:1 Multiplexer/Demultiplexer	16	—	0.25	8.17
PI5C3383	5-Bit, 4-Port Bus Switch	24	—	0.25	8.20
PI5C3384	10-Bit, 2-Port Bus Switch	24	—	0.25	8.23
PI5C32384	10-Bit, 2-Port Bus Switch (25Ω Series)	24	—	0.25	8.23
PI5C3400	4-Bit, 4-Port Bus Switch	24	—	0.25	8.27
PI5C3401	6-Bit, 3-Port Bus Switch	24	—	0.25	8.31
PI5C3861	10-Bit, 2-Port Bus Switch	24	—	0.25	8.34

PRODUCT SELECTION GUIDE (Continued)

CLOCK DISTRIBUTION PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (ns)	Databook Page No.
PI49FCT804T	Buffer/Clock Driver	16	-24/64 mA	5.8	9.1
PI49FCT805T	Buffer/Clock Driver	20	-24/64 mA	4.5	9.7
PI49FCT806T	Buffer/Clock Driver	20	-24/64 mA	4.5	9.7
PI49FCT3805	3.3V Buffer/Clock Driver	20	-8/24 mA	4.5	9.13
PI49FCT3806	3.3V Buffer/Clock Driver	20	-8/24 mA	4.5	9.13
PI49FCT807T	Clock Driver	20	-32/48 mA	3.5	9.19
PI49FCT3807	3.3V Clock Driver	20	-8/24 mA	3.5	9.23
PI49FCT811T	Programmable Buffer/Clock Driver	24	-24/64 mA	5.0	9.28
PI6B2407	BiCMOS PLL Universal Clock Distribution Chip	44	—	—	9.3

CLOCK GENERATOR PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Frequency (MHz)	Databook Page No.
PI6C9107U-03	Low Cost 14-Pin CPU Frequency Generator	14	-4/8 mA	100	10.1
PI6C9107U-05	Low Cost 8-Pin CPU Frequency Generator	8	-8/8 mA	80	10.5
PI6C9108-05	Low Cost 3V 8-Pin CPU Frequency Generator	8	-8/8 mA	80	10.8
PI6C9155U-01	20-Pin CPU Frequency Generator	20	-12/8 mA	100	10.11
PI6C9155U-02	20-Pin CPU Frequency Generator	20	-12/8 mA	100	10.11
PI6C9155U-03	20-Pin CPU Frequency Generator	20	-12/8 mA	100	10.11
PI6C9155W-01	20-Pin CPU Frequency Generator	20	-12/8 mA	100	10.11
PI6C9155W-02	20-Pin CPU Frequency Generator	20	-12/8 mA	100	10.11
PI6C9155W-03	20-Pin CPU Frequency Generator	20	-12/8 mA	100	10.11
PI6C9156U-01	20-Pin CPU Frequency Generator	20	-4/8 mA	66.6	10.22
PI6C9156U-02	20-Pin CPU Frequency Generator	20	-4/8 mA	66.6	10.22
PI6C9156U-03	20-Pin CPU Frequency Generator	20	-4/8 mA	66.6	10.22
PI6C462	28-Pin Motherboard Clock Generator	28	-12 mA	100	10.29
PI6C464	28-Pin Motherboard Clock Generator	28	-12 mA	80	10.34
PI6C468	28-Pin Motherboard Clock Generator	28	-12 mA	80	10.39
PI6C471	28-Pin Motherboard Clock Generator	28	-12 mA	80	10.44

NETWORKING PRODUCTS

Part No.	Description	No. Pins	Power Ioh/Iol	Speed (Mbps)	Databook Page No.
PI6C3000	Token Ring Active Retiming Hub Interface Chip	48	—	4/16	11.1

PRODUCT CROSS REFERENCE GUIDE

*Note: With the exception of lower VOH (TTL level), Pericom FCT is functionally and AC compatible with this device

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AMD	PERICOM
Am29C821A	PI74FCT821BT
Am29C823A	PI74FCT823BT
Am29C827A	PI74FCT827AT
Am29C828A	PI74FCT828AT
Am29C841A	PI74FCT841BT
Am29C843A	PI74FCT843BT
Am29C861A	PI74FCT861BT
Am29C863A	PI74FCT863BT
Cypress	PERICOM
CY29FCT52AT/BT/CT	PI29FCT52AT/BT/CT
CY29FCT520AT/BT	PI29FCT520AT/BT
CY74FCT138T/AT/CT	PI74FCT138T/AT/CT
CY74FCT157T/AT/CT	PI74FCT157T/AT/CT
CY74FCT2240T/AT/CT	PI74FCT2240T/AT/CT
CY74FCT2244T/AT/CT	PI74FCT2244T/AT/CT
CY74FCT2245T/AT/CT	PI74FCT2245T/AT/CT
CY74FCT2257T/AT/CT	PI74FCT2257T/AT/CT
CY74FCT2373T/AT/CT	PI74FCT2373T/AT/CT
CY74FCT2374T/AT/CT	PI74FCT2374T/AT/CT
CY74FCT240T/AT/CT	PI74FCT240T/AT/CT
CY74FCT244T/AT/CT	PI74FCT244T/AT/CT
CY74FCT245T/AT/CT	PI74FCT245T/AT/CT
CY74FCT2541T/AT/CT	PI74FCT2541T/AT/CT
CY74FCT2543T/AT/CT	PI74FCT2543T/AT/CT
CY74FCT2573T/AT/CT	PI74FCT2573T/AT/CT
CY74FCT2574T/AT/CT	PI74FCT2574T/AT/CT
CY74FCT2575T/AT/CT	PI74FCT2575T/AT/CT
CY74FCT2646T/AT/CT	PI74FCT2646T/AT/CT
CY74FCT2652T/AT/CT	PI74FCT2652T/AT/CT
CY74FCT273T/AT/CT	PI74FCT273T/AT/CT
CY74FCT373T/AT/CT	PI74FCT373T/AT/CT
CY74FCT374T/AT/CT	PI74FCT374T/AT/CT
CY74FCT377T/AT/CT	PI74FCT377T/AT/CT
CY74FCT399T/AT/CT	PI74FCT399T/AT/CT
CY74FCT540T/AT/CT	PI74FCT540T/AT/CT
CY74FCT541T/AT/CT	PI74FCT541T/AT/CT
CY74FCT543T/AT/CT	PI74FCT543T/AT/CT
CY74FCT573T/AT/CT	PI74FCT573T/AT/CT
CY74FCT574T/AT/CT	PI74FCT574T/AT/CT
CY74FCT646T/AT/CT	PI74FCT646T/AT/CT
CY74FCT648T/AT/CT	PI74FCT648T/AT/CT
CY74FCT652T/AT/CT	PI74FCT652T/AT/CT
CY74FCT821AT/BT/CT	PI74FCT821AT/BT/CT
CY74FCT823AT/BT/CT	PI74FCT823AT/BT/CT
CY74FCT825AT/BT/CT	PI74FCT825AT/BT/CT
CY74FCT827AT/BT/CT	PI74FCT827AT/BT/CT
CY74FCT841AT/BT/CT	PI74FCT841AT/BT/CT

Bus Switch	
CYBUS3384	PI5C3384A

IDT	PERICOM
IDT74FBT2240/A	PI74FCT2240T/AT
IDT74FBT2244/A	PI74FCT2244T/AT
IDT74FBT2373/A	PI74FCT2373T/AT
IDT74FBT2827A/B	PI74FCT2827AT/BT
IDT74FBT2828A/B	PI74FCT2828AT/BT
IDT74FBT2841A/B	PI74FCT2841AT/BT
IDT74FCT2240T/AT/CT	PI74FCT2240T/AT/CT
IDT74FCT2244T/AT/CT	PI74FCT2244T/AT/CT
IDT74FCT2373T/AT/CT	PI74FCT2373T/AT/CT
IDT74FCT2374T/AT/CT	PI74FCT2374T/AT/CT
IDT74FCT2541T/AT/CT	PI74FCT2541T/AT/CT
IDT74FCT2543T/AT/CT	PI74FCT2543T/AT/CT
IDT74FCT2573T/AT/CT	PI74FCT2573T/AT/CT
IDT74FCT2574T/AT/CT	PI74FCT2574T/AT/CT
IDT74FCT2645T/AT/CT	PI74FCT2645T/AT/CT
IDT74FCT2646T/AT	PI74FCT2646T/AT
IDT74FCT2652T/AT	PI74FCT2652T/AT
IDT74FCT2821AT/BT/CT	PI74FCT2821AT/BT/CT
IDT74FCT2823AT/BT/CT	PI74FCT2823AT/BT/CT
IDT74FCT2827AT/BT	PI74FCT2827AT/BT
IDT74FCT2841AT/BT/CT	PI74FCT2841AT/BT/CT
IDT29FCT52A/B/C*	PI29FCT52AT/BT/CT
IDT29FCT52AT/BT/CT	PI29FCT52AT/BT/CT
IDT29FCT53A/B/C*	PI29FCT53AT/BT/CT
IDT29FCT53AT/BT/CT	PI29FCT53AT/BT/CT
IDT29FCT520A/B*	PI29FCT520AT/BT
IDT29FCT520AT/BT	PI29FCT520AT/BT
IDT29FCT521A/B*	PI29FCT521AT/BT
IDT29FCT521AT/BT	PI29FCT521AT/BT
IDT74FCT138/A/C*	PI74FCT138T/AT/CT
IDT74FCT138T/AT/CT	PI74FCT138T/AT/CT
IDT74FCT139/A/C*	PI74FCT139T/AT/CT
IDT74FCT139T/AT/CT	PI74FCT139T/AT/CT
IDT74FCT151A/C*	PI74FCT151T/AT/CT
IDT74FCT157T/AT/CT/DT	PI74FCT157T/AT/CT/DT
IDT74FCT240/A/C*	PI74FCT240T/AT/CT
IDT74FCT240T/AT/CT/DT	PI74FCT240T/AT/CT/DT
IDT74FCT241/A/C*	PI74FCT241T/AT/CT
IDT74FCT241T/AT/CT/DT	PI74FCT241T/AT/CT/DT
IDT74FCT244/A/C*	PI74FCT244T/AT/CT
IDT74FCT244T/AT/CT/DT	PI74FCT244T/AT/CT/DT
IDT74FCT245/A/C*	PI74FCT245T/AT/CT
IDT74FCT245T/AT/CT/DT	PI74FCT245T/AT/CT/DT
IDT74FCT251T/AT/CT	PI74FCT251T/AT/CT
IDT74FCT257T/AT/CT	PI74FCT257T/AT/CT
IDT74FCT273/A/C*	PI74FCT273T/AT/CT
IDT74FCT273T/AT/CT/DT	PI74FCT273T/AT/CT/DT
IDT74FCT373/A/C*	PI74FCT373T/AT/CT
IDT74FCT373T/AT/CT/DT	PI74FCT373T/AT/CT/DT

IDT	PERICOM
IDT74FCT374/A/C*	PI74FCT374T/AT/CT
IDT74FCT374T/AT/CT	PI74FCT374T/AT/CT
IDT74FCT377/A/C*	PI74FCT377T/AT/CT
IDT74FCT377T/AT/CT/DT	PI74FCT377T/AT/CT/DT
IDT74FCT399/A/C*	PI74FCT399T/AT/CT
IDT74FCT399T/AT/CT	PI74FCT399T/AT/CT
IDT74FCT521/A/C*	PI74FCT521T/AT/BT/CT
IDT74FCT521T/AT/BT/CT	PI74FCT521T/AT/BT/CT
IDT74FCT533/A/C*	PI74FCT533T/AT/CT
IDT74FCT533T/AT/CT	PI74FCT533T/AT/CT
IDT74FCT534/A/C*	PI74FCT534T/AT/CT
IDT74FCT534T/AT/CT	PI74FCT534T/AT/CT
IDT74FCT540/A/C*	PI74FCT540T/AT/CT
IDT74FCT540T/AT/CT	PI74FCT540T/AT/CT
IDT74FCT541/A/C*	PI74FCT541T/AT/CT
IDT74FCT541T/AT/CT	PI74FCT541T/AT/CT
IDT74FCT543/A/C*	PI74FCT543T/AT/CT
IDT74FCT543T/AT/CT/DT	PI74FCT543T/AT/CT/DT
IDT74FCT573/A/C*	PI74FCT573T/AT/CT
IDT74FCT573T/AT/CT	PI74FCT573T/AT/CT
IDT74FCT574/A/C*	PI74FCT574T/AT/CT
IDT74FCT574T/AT/CT	PI74FCT574T/AT/CT
IDT74FCT623T/AT/CT	PI74FCT623T/AT/CT
IDT74FCT640/A/C*	PI74FCT640T/AT/CT
IDT74FCT640T/AT/CT	PI74FCT640T/AT/CT
IDT74FCT645/A/C*	PI74FCT645T/AT/CT
IDT74FCT645T/AT/CT/DT	PI74FCT645T/AT/CT/DT
IDT74FCT646/A/C*	PI74FCT646T/AT/CT
IDT74FCT646T/AT/CT	PI74FCT646T/AT/CT
IDT74FCT648T/AT/CT	PI74FCT648T/AT/CT
IDT74FCT651T/AT/CT	PI74FCT651T/AT/CT
IDT74FCT652T/AT/CT/DT	PI74FCT652T/AT/CT/DT
IDT74FCT821A/B/C*	PI74FCT821AT/BT/CT
IDT74FCT821AT/BT/CT	PI74FCT821AT/BT/CT
IDT74FCT823A/B/C*	PI74FCT823AT/BT/CT
IDT74FCT823AT/BT/CT	PI74FCT823AT/BT/CT
IDT74FCT825A/B/C*	PI74FCT825AT/BT/CT
IDT74FCT825AT/BT/CT	PI74FCT825AT/BT/CT
IDT74FCT827A/B/C*	PI74FCT827AT/BT/CT
IDT74FCT827AT/BT/CT	PI74FCT827AT/BT/CT
IDT74FCT828A/BT/CT	PI74FCT828AT/BT/CT
IDT74FCT841A/B/C*	PI74FCT841AT/BT/CT
IDT74FCT841AT/BT/CT	PI74FCT841AT/BT/CT
IDT74FCT843A/B/C*	PI74FCT843AT/BT/CT
IDT74FCT843AT/BT/CT	PI74FCT843AT/BT/CT
IDT74FCT845A/B/C*	PI74FCT845AT/BT/CT
IDT74FCT845AT/BT/CT	PI74FCT845AT/BT/CT
IDT74FCT861A/B*	PI74FCT861AT/BT
IDT74FCT863A/B*	PI74FCT863AT/BT
IDT74FCT864A/B*	PI74FCT864AT/BT

PRODUCT CROSS REFERENCE GUIDE (Continued)

*Note: With the exception of lower VOH (TTL level), Pericom FCT is functionally and AC compatible with this device

IDT	PERICOM
5V 16-Bit with High Drive	
IDT74FCT16240T/AT/CT	PI74FCT16240T/AT/CT
IDT74FCT16244T/AT/CT	PI74FCT16244T/AT/CT
IDT74FCT16245T/AT/CT	PI74FCT16245T/AT/CT
IDT74FCT16373T/AT/CT	PI74FCT16373T/AT/CT
IDT74FCT16374T/AT/CT	PI74FCT16374T/AT/CT
IDT74FCT16500AT/CT	PI74FCT16500AT/CT
IDT74FCT16501AT/CT	PI74FCT16501AT/CT
IDT74FCT16543T/AT/CT	PI74FCT16543T/AT/CT
IDT74FCT16646T/AT/CT	PI74FCT16646T/AT/CT
IDT74FCT16652T/AT/CT	PI74FCT16652T/AT/CT
IDT74FCT16823AT/BT/CT	PI74FCT16823AT/BT/CT
IDT74FCT16827AT/BT/CT	PI74FCT16827AT/BT/CT
IDT74FCT16841AT/BT/CT	PI74FCT16841AT/BT/CT
IDT74FCT16952T/AT/CT	PI74FCT16952T/AT/CT
5V 16-Bit with Bal. drive	
IDT74FCT162240T/AT/CT	PI74FCT162240T/AT/CT
IDT74FCT162244T/AT/CT	PI74FCT162244T/AT/CT
IDT74FCT162245T/AT/CT	PI74FCT162245T/AT/CT
IDT74FCT162373T/AT/CT	PI74FCT162373T/AT/CT
IDT74FCT162374T/AT/CT	PI74FCT162374T/AT/CT
IDT74FCT162500AT/CT	PI74FCT162500AT/CT
IDT74FCT162501AT/CT	PI74FCT162501AT/CT
IDT74FCT162543T/AT/CT	PI74FCT162543T/AT/CT
IDT74FCT162646T/AT/CT	PI74FCT162646T/AT/CT
IDT74FCT162652T/AT/CT	PI74FCT162652T/AT/CT
IDT74FCT162823AT/BT/CT	PI74FCT162823AT/BT/CT
IDT74FCT162827AT/BT/CT	PI74FCT162827AT/BT/CT
IDT74FCT162841AT/BT/CT	PI74FCT162841AT/BT/CT
IDT74FCT162952T/AT/CT	PI74FCT162952T/AT/CT
3.3V 16-Bit FCT Logic	
IDT74FCT163244/A/C	PI74FCT163244/A/C
IDT74FCT163245/A/C	PI74FCT163245/A/C
IDT74FCT163373/A	PI74FCT163373/A
IDT74FCT163374/A	PI74FCT163374/A
IDT74FCT163244/A/C	PI74LPT16244/A/C
IDT74FCT163245/A/C	PI74LPT16245/A/C
IDT74FCT163373/A	PI74LPT16373/A
IDT74FCT163374/A	PI74LPT16374/A
Clock Driver	
IDT49FCT805/A*	PI49FCT805T/AT
IDT74FCT805BT/CT	PI49FCT805BT/CT
IDT49FCT806/A*	PI49FCT806/A
IDT74FCT806BT/CT	PI49FCT806BT/CT
IDT74FCT807AT/BT	PI49FCT807AT/BT
ICS	
Clock Generator	
AV9107C	PI6C9107
AV9108	PI6C9108
AV9155	PI6C9155

IMI	PERICOM
Clock Generator	
IMISC462	PI6C462
IMISC464	PI6C464
IMISC468	PI6C468
IMISC471	PI6C471
QSI	
PERICOM	
QS29FCT520AT/BT	PI29FCT520AT/BT
QS29FCT521AT/BT	PI29FCT521AT/BT
QS29FCT52AT/BT/CT	PI29FCT52AT/BT/CT
QS29FCT53AT/BT/CT	PI29FCT53AT/BT/CT
QS74FCT138T/AT/CT	PI74FCT138T/AT/CT
QS74FCT139T/AT/CT	PI74FCT139T/AT/CT
QS74FCT151T/AT/CT	PI74FCT151T/AT/CT
QS74FCT153T/AT/CT	PI74FCT153T/AT/CT
QS74FCT157T/AT/CT/DT	PI74FCT157T/AT/CT/DT
QS74FCT2153T/AT/CT	PI74FCT2153T/AT/CT
QS74FCT2157T/AT/CT	PI74FCT2157T/AT/CT
QS74FCT2240T/AT/CT	PI74FCT2240T/AT/CT
QS74FCT2241T/AT/CT	PI74FCT2241T/AT/CT
QS74FCT2244T/AT/CT	PI74FCT2244T/AT/CT
QS74FCT2245T/AT/CT	PI74FCT2245T/AT/CT
QS74FCT2253T/AT/CT	PI74FCT2253T/AT/CT
QS74FCT2257T/AT/CT	PI74FCT2257T/AT/CT
QS74FCT2273T/AT/CT	PI74FCT2273T/AT/CT
QS74FCT2373T/AT/CT	PI74FCT2373T/AT/CT
QS74FCT2374T/AT/CT	PI74FCT2374T/AT/CT
QS74FCT238T/AT/CT	PI74FCT238T/AT/CT
QS74FCT239T/AT/CT	PI74FCT239T/AT/CT
QS74FCT240T/AT/CT/DT	PI74FCT240T/AT/CT/DT
QS74FCT241T/AT/CT/DT	PI74FCT241T/AT/CT/DT
QS74FCT244T/AT/CT/DT	PI74FCT244T/AT/CT/DT
QS74FCT245T/AT/CT/DT	PI74FCT245T/AT/CT/DT
QS74FCT251T/AT/CT	PI74FCT251T/AT/CT
QS74FCT253T/AT/CT	PI74FCT253T/AT/CT
QS74FCT2541T/AT/CT	PI74FCT2541T/AT/CT
QS74FCT2543T/AT/CT	PI74FCT2543T/AT/CT
QS74FCT2573T/AT	PI74FCT2573T/AT
QS74FCT2574T/AT/CT	PI74FCT2574T/AT/CT
QS74FCT257T/AT/CT	PI74FCT257T/AT/CT
QS74FCT2646T/AT	PI74FCT2646T/AT
QS74FCT2652T/AT	PI74FCT2652T/AT
QS74FCT273T/AT/CT/DT	PI74FCT273T/AT/CT/DT
QS74FCT280AT/BT/CT	PI74FCT280AT/BT/CT
QS74FCT2823AT/BT/CT	PI74FCT2823AT/BT/CT
QS74FCT2827AT/BT	PI74FCT2827AT/BT
QS74FCT2841AT/BT/CT	PI74FCT2841AT/BT/CT
QS74FCT373T/AT/CT/DT	PI74FCT373T/AT/CT/DT
QS74FCT374T/AT/CT	PI74FCT374T/AT/CT
QS74FCT377T/AT/CT/DT	PI74FCT377T/AT/CT/DT
QS74FCT521T/AT/BT/CT/DT	PI74FCT521T/AT/BT/CT/DT

QSI	PERICOM
QS74FCT533T/AT/CT/DT	PI74FCT533T/AT/CT/DT
QS74FCT534T/AT/CT/DT	PI74FCT534T/AT/CT/DT
QS74FCT540T/AT/CT/DT	PI74FCT540T/AT/CT/DT
QS74FCT541T/AT/CT/DT	PI74FCT541T/AT/CT/DT
QS74FCT543T/AT/CT/DT	PI74FCT543T/AT/CT/DT
QS74FCT544T/AT/CT/DT	PI74FCT544T/AT/CT/DT
QS74FCT573T/AT/CT	PI74FCT573T/AT/CT
QS74FCT574T/AT/CT	PI74FCT574T/AT/CT
QS74FCT640T/AT/CT/DT	PI74FCT640T/AT/CT/DT
QS74FCT646T/AT/CT	PI74FCT646T/AT/CT
QS74FCT648T/AT/CT	PI74FCT648T/AT/CT
QS74FCT651T/AT/CT/DT	PI74FCT651T/AT/CT/DT
QS74FCT652T/AT/CT/DT	PI74FCT652T/AT/CT/DT
QS74FCT821AT/BT/CT	PI74FCT821AT/BT/CT
QS74FCT823AT/BT/CT	PI74FCT823AT/BT/CT
QS74FCT825AT/BT/CT	PI74FCT825AT/BT/CT
QS74FCT827AT/BT/CT	PI74FCT827AT/BT/CT
QS74FCT828AT/BT/CT	PI74FCT828AT/BT/CT
QS74FCT841AT/BT/CT	PI74FCT841AT/BT/CT
QS74FCT843AT/BT/CT	PI74FCT843AT/BT/CT
QS74FCT845AT/BT/CT	PI74FCT845AT/BT/CT
QS74FCT861AT/BT/CT	PI74FCT861AT/BT/CT
QS74FCT863AT/BT/CT	PI74FCT863AT/BT/CT
QS74FCT864AT/BT/CT	PI74FCT864AT/BT/CT
Bus Switch	
QS3125	PI5C3125
QS3126	PI5C3126
QS3245	PI5C3245
QS3257	PI5C3257
QS3383	PI5C3383
QS3384	PI5C3384
QS32384	PI5C32384
Clock Driver	
QS5805T/AT	PI49FCT805T/AT
QS5806T/AT	PI49FCT806T/AT
National	
PERICOM	
74ACT138*	PI74FCT138T
74ACT139*	PI74FCT139T
74ACT151*	PI74FCT151T
74ACT153*	PI74FCT153T
74ACT157*	PI74FCT157T
74ACT240*	PI74FCT240T
74ACT241*	PI74FCT241T
74ACT244*	PI74FCT244T
74ACT245*	PI74FCT245T
74ACT251*	PI74FCT251T
74ACT253*	PI74FCT253T
74ACT257*	PI74FCT257T
74ACT273*	PI74FCT273T
74ACT373*	PI74FCT373T

PRODUCT CROSS REFERENCE GUIDE (Continued)

1

*Note: With the exception of lower VOH (TTL level), Pericom FCT is functionally and AC compatible with this device

National	PERICOM
74ACT374*	PI74FCT374T
74ACT377*	PI74FCT377T
74ACT521*	PI74FCT521T
74ACT534*	PI74FCT534T
74ACT573*	PI74FCT573T
74ACT574*	PI74FCT574T
74ACT646*	PI74FCT646T
74ACT821*	PI74FCT821AT
74ACT823*	PI74FCT823AT
74ACT825*	PI74FCT825AT
74ACT841*	PI74FCT841AT
74ACT843*	PI74FCT843AT
74ACT845*	PI74FCT845AT
74ACTQ240*	PI74FCT240T
74ACTQ241*	PI74FCT241T
74ACTQ244*	PI74FCT244T
74ACTQ245*	PI74FCT245T
74ACTQ273*	PI74FCT273T
74ACTQ373*	PI74FCT373T
74ACTQ374*	PI74FCT374T
74ACTQ377*	PI74FCT377T
74ACTQ533*	PI74FCT533T
74ACTQ534*	PI74FCT534T
74ACTQ543*	PI74FCT543T
74ACTQ544*	PI74FCT544T
74ACTQ573*	PI74FCT573T
74ACTQ574*	PI74FCT574T
74ACTQ646*	PI74FCT646T
74ACTQ821*	PI74FCT821AT
74ACTQ823*	PI74FCT823AT
74ACTQ827*	PI74FCT827AT
74ACTQ841*	PI74FCT841AT
74ACTQ843*	PI74FCT843AT
74FCT138/A*	PI74FCT138T/A
74FCT240/A*	PI74FCT240T/AT
74FCT241/A*	PI74FCT241T/AT
74FCT244/A*	PI74FCT244T/AT
74FCT245/A*	PI74FCT245T/AT
74FCT273*	PI74FCT273T
74FCT373/A*	PI74FCT373T/AT
74FCT374/A*	PI74FCT374T/AT
74FCT377*	PI74FCT377T
74FCT521/A*	PI74FCT521T/AT
74FCT533/A*	PI74FCT533T/AT
74FCT534/A*	PI74FCT534T/AT
74FCT540*	PI74FCT540T
74FCT541*	PI74FCT541T
74FCT543/A*	PI74FCT543T/AT
74FCT544/A*	PI74FCT544T/AT

National	PERICOM
74FCT573/A*	PI74FCT573T/AT
74FCT574/A*	PI74FCT574T/AT
74FCT821A/B*	PI74FCT821AT/BT
74FCT823A/B*	PI74FCT823AT/BT
74FCT825A*	PI74FCT825AT
74FCT827A/B*	PI74FCT827AT/BT
74FCT841A/B*	PI74FCT841AT/BT
74FCT843A/B*	PI74FCT843AT/BT
74FCT845A/B*	PI74FCT845AT/BT
3.3V 8-Bit	
74LCX244	PI74LPT244
74LCX245	PI74LPT245
74LCX373	PI74LPT373
74LVT240	PI74LPT240C
74LVT244	PI74LPT244C
74LVT245	PI74LPT245C
74LVT373	PI74LPT373C
74LVT374	PI74LPT374C
3.3V 16-Bit	
74LCX16244	PI74LPT16244
74LCX16244	PI74LPT16245
74LCX16373	PI74LPT16373
74LCX16374	PI74LPT16374
74LVT16240	PI74LPT16240C
74LVT16244	PI74LPT16244C
74LVT16245	PI74LPT16245C
74LVT16373	PI74LPT16373A
74LVT16374	PI74LPT16374A
Philips PERICOM	
74ABT240	PI74FCT240AT
74ABT241	PI74FCT241CT
74ABT244	PI74FCT244CT
74ABT245	PI74FCT245CT
74ABT2952	PI29FCT52AT
74ABT2953	PI29FCT53AT
74ABT273	PI74FCT273AT
74ABT373	PI74FCT373AT
74ABT374	PI74FCT374AT
74ABT377	PI74FCT377CT
74ABT533	PI74FCT533AT
74ABT534	PI74FCT534CT
74ABT540	PI74FCT540AT
74ABT541	PI74FCT541CT
74ABT543	PI74FCT543AT
74ABT544	PI74FCT544AT
74ABT573	PI74FCT573AT
74ABT574	PI74FCT574AT
74ABT623	PI74FCT623CT
74ABT640	PI74FCT640CT

Philips	PERICOM
74ABT646	PI74FCT646AT
74ABT648	PI74FCT648AT
74ABT651	PI74FCT651CT
74ABT652	PI74FCT651AT
74ABT821	PI74FCT821BT
74ABT823	PI74FCT823BT
74ABT827	PI74FCT827BT
74ABT841	PI74FCT841BT
74ABT843	PI74FCT843BT
74ABT845	PI74FCT845BT
74ABT861	PI74FCT861BT
74ABT863	PI74FCT863BT
TI PERICOM	
SN74ABT2240	PI74FCT2240AT
SN74ABT2241	PI74FCT2241AT
SN74ABT2244	PI74FCT2244AT
SN74ABT2245	PI74FCT2245AT
SN74ABT240	PI74FCT240AT
SN74ABT241	PI74FCT241CT
SN74ABT244	PI74FCT244CT
SN74ABT245	PI74FCT245CT
SN74ABT2952	PI29FCT52AT
SN74ABT2953	PI29FCT53AT
SN74ABT273	PI74FCT273AT
SN74ABT373	PI74FCT373AT
SN74ABT374	PI74FCT374AT
SN74ABT377	PI74FCT377CT
SN74ABT533	PI74FCT533AT
SN74ABT534	PI74FCT534CT
SN74ABT540	PI74FCT540AT
SN74ABT541	PI74FCT541CT
SN74ABT543	PI74FCT543AT
SN74ABT544	PI74FCT544AT
SN74ABT573	PI74FCT573AT
SN74ABT574	PI74FCT574AT
SN74ABT623	PI74FCT623CT
SN74ABT640	PI74FCT640CT
SN74ABT646	PI74FCT646AT
SN74ABT646A	PI74FCT646CT
SN74ABT651	PI74FCT651CT
SN74ABT652	PI74FCT651AT
SN74ABT821	PI74FCT821BT
SN74ABT823	PI74FCT823BT
SN74ABT827	PI74FCT827BT
SN74ABT828	PI74FCT828BT
SN74ABT841	PI74FCT841BT
SN74ABT843	PI74FCT843BT

PRODUCT CROSS REFERENCE GUIDE (Continued)

*Note: With the exception of lower VOH (TTL level), Pericom FCT is functionally and AC compatible with this device

TI	PERICOM
SN74ABT861	PI74FCT861BT
SN74ABT863	PI74FCT863BT
5V 16-Bit	
SN74ABT16240	PI74FCT16240AT
SN74ABT16244	PI74FCT16244CT
SN74ABT16245	PI74FCT16245CT
SN74ABT16373	PI74FCT16373AT
SN74ABT16374	PI74FCT16374AT
SN74ABT16500A	PI74FCT16500CT
SN74ABT16540	PI74FCT16540CT
SN74ABT16541	PI74FCT16541DT
SN74ABT16543	PI74FCT16543DT
SN74ABT16646	PI74FCT16646CT
SN74ABT16652	PI74FCT16652DT
SN74ABT16823	PI74FCT16823CT
SN74ABT16952	PI74FCT16952DT
3.3V 8-Bit	
SN74LVT244/A	PI74LPT244C
SN74LVT245/A	PI74LPT245C
SN74LVT573	PI74LPT573C
3.3V 16-Bit	
SN74LVT16244A	PI74LPT16244C
SN74LVT16245A	PI74LPT16245C
SN74LVT16373	PI74LPT16373A
SN74LVT16374	PI74LPT16374A

PERICOM	PERICOM
PI74FCT861BT	PI74FCT861BT
PI74FCT863BT	PI74FCT863BT
PI74FCT16240AT	PI74FCT16240AT
PI74FCT16244CT	PI74FCT16244CT
PI74FCT16245CT	PI74FCT16245CT
PI74FCT16373AT	PI74FCT16373AT
PI74FCT16374AT	PI74FCT16374AT
PI74FCT16500CT	PI74FCT16500CT
PI74FCT16540CT	PI74FCT16540CT
PI74FCT16541DT	PI74FCT16541DT
PI74FCT16543DT	PI74FCT16543DT
PI74FCT16646CT	PI74FCT16646CT
PI74FCT16652DT	PI74FCT16652DT
PI74FCT16823CT	PI74FCT16823CT
PI74FCT16952DT	PI74FCT16952DT
PI74LPT244C	PI74LPT244C
PI74LPT245C	PI74LPT245C
PI74LPT573C	PI74LPT573C
PI74LPT16244C	PI74LPT16244C
PI74LPT16245C	PI74LPT16245C
PI74LPT16373A	PI74LPT16373A
PI74LPT16374A	PI74LPT16374A

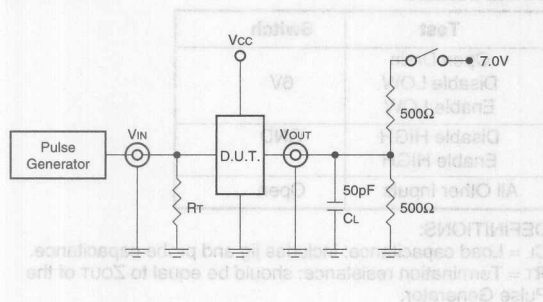
PERICOM	PERICOM
PI74FCT861BT	PI74FCT861BT
PI74FCT863BT	PI74FCT863BT
PI74FCT16240AT	PI74FCT16240AT
PI74FCT16244CT	PI74FCT16244CT
PI74FCT16245CT	PI74FCT16245CT
PI74FCT16373AT	PI74FCT16373AT
PI74FCT16374AT	PI74FCT16374AT
PI74FCT16500CT	PI74FCT16500CT
PI74FCT16540CT	PI74FCT16540CT
PI74FCT16541DT	PI74FCT16541DT
PI74FCT16543DT	PI74FCT16543DT
PI74FCT16646CT	PI74FCT16646CT
PI74FCT16652DT	PI74FCT16652DT
PI74FCT16823CT	PI74FCT16823CT
PI74FCT16952DT	PI74FCT16952DT
PI74LPT244C	PI74LPT244C
PI74LPT245C	PI74LPT245C
PI74LPT573C	PI74LPT573C
PI74LPT16244C	PI74LPT16244C
PI74LPT16245C	PI74LPT16245C
PI74LPT16373A	PI74LPT16373A
PI74LPT16374A	PI74LPT16374A

Test Circuits and Waveforms

74FCTXXXXT, 74FCT16XXXXT – 5V Families

1

Test Circuits



Switch Position

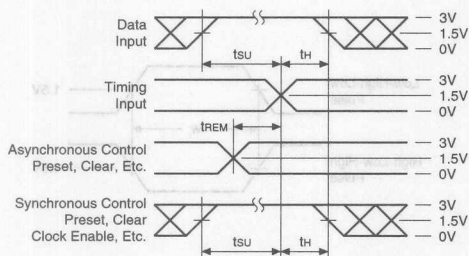
Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

DEFINITIONS:

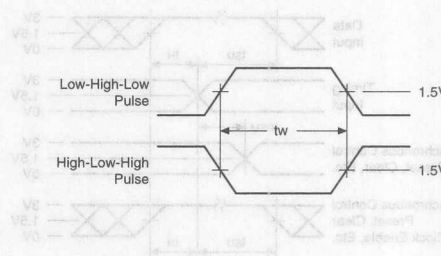
C_L = Load capacitance: includes jig and probe capacitance.

R_t = Termination resistance: should be equal to Z_{out} of the Pulse Generator.

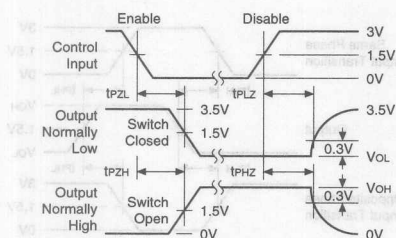
Setup, Hold, and Release Timing



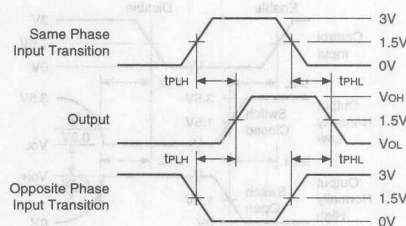
Pulse Width



Enable and Disable Timing



Propagation Delay



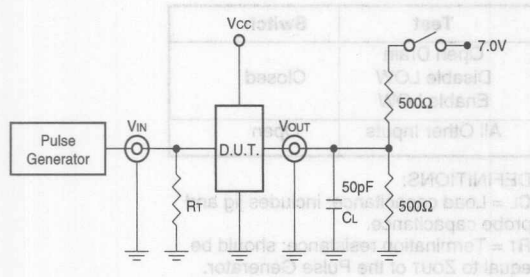
1. Input Control Enable = Low and input Control Disable = High.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_{out} \leq 50 \Omega$; t_r , $t_n \leq 2.5$ ns.

Test Circuits and waveforms

74FCT163XXX & 74LPT16XXX – 3.3V Double Density Families

LPTXXX – 3.3V Standard Family

Test Circuits



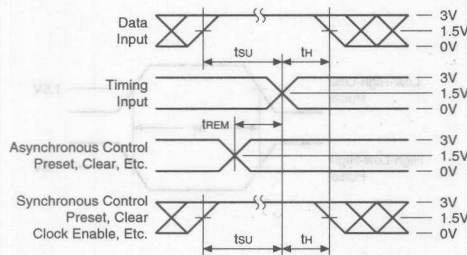
Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

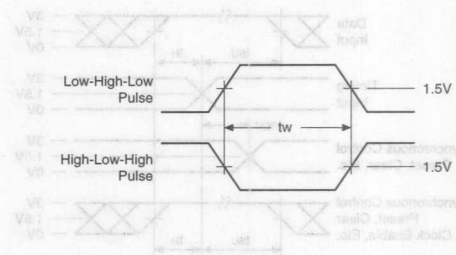
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

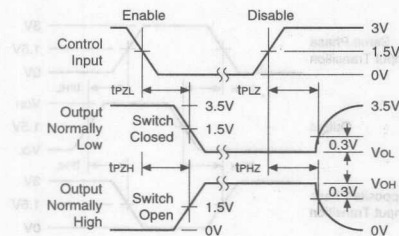
Setup, Hold, and Release Timing



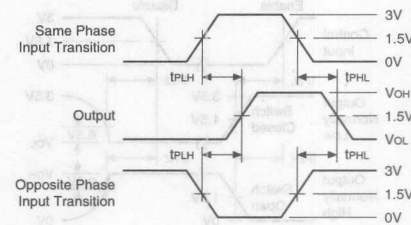
Pulse Width



Enable and Disable Timing



Propagation Delay

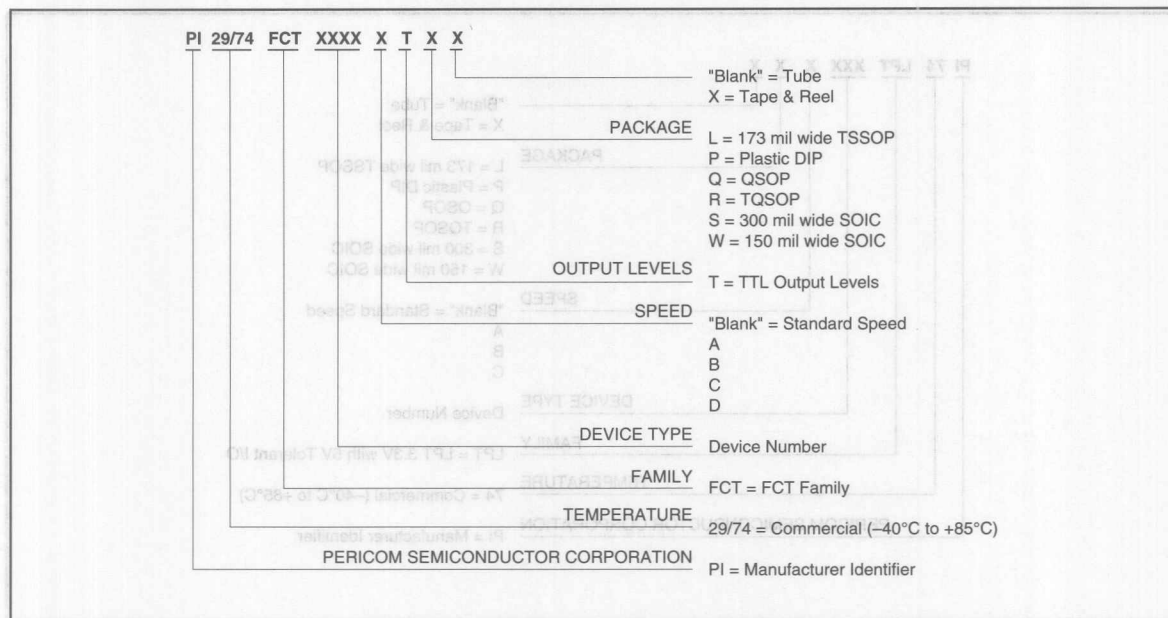


1. Input Control Enable = Low and input Control Disable = High.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_{OUT} $\leq 50 \Omega$; t_r, t_f ≤ 2.5 ns.

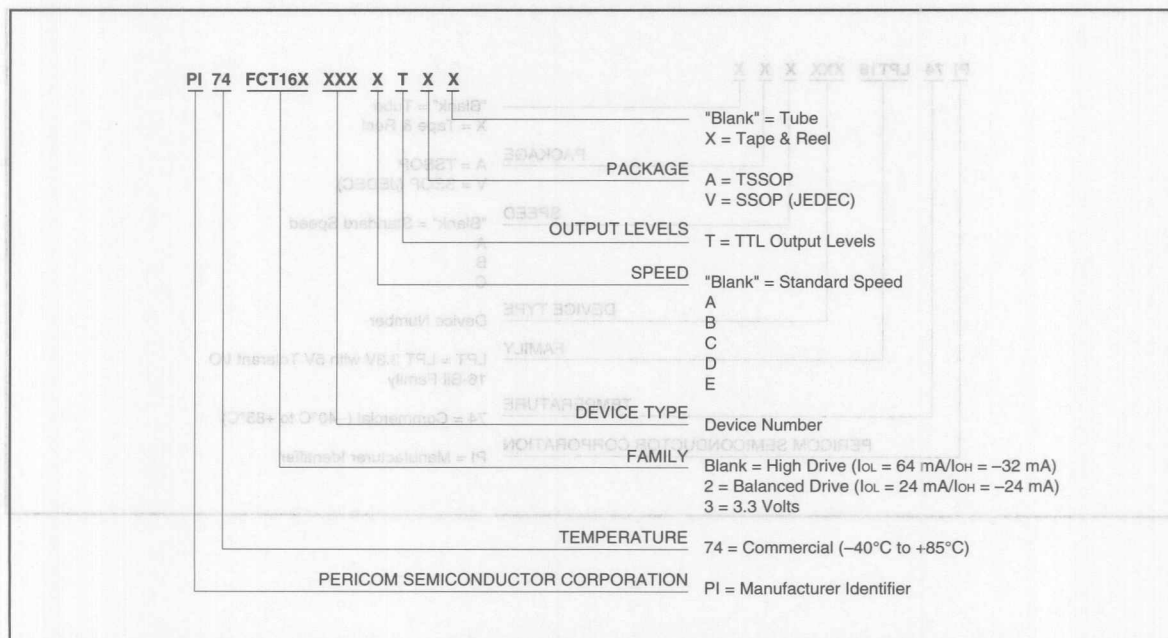
ORDERING INFORMATION

1

Ordering Number Information — FCTXXXXT

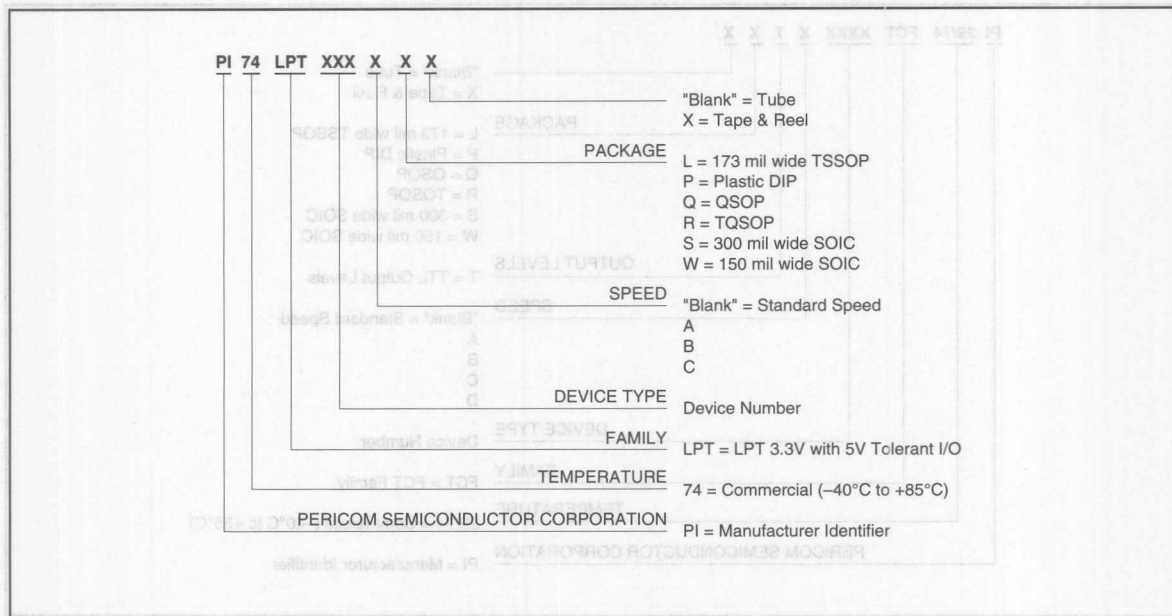


Ordering Number Information — FCT16XXXXT (Double Density)

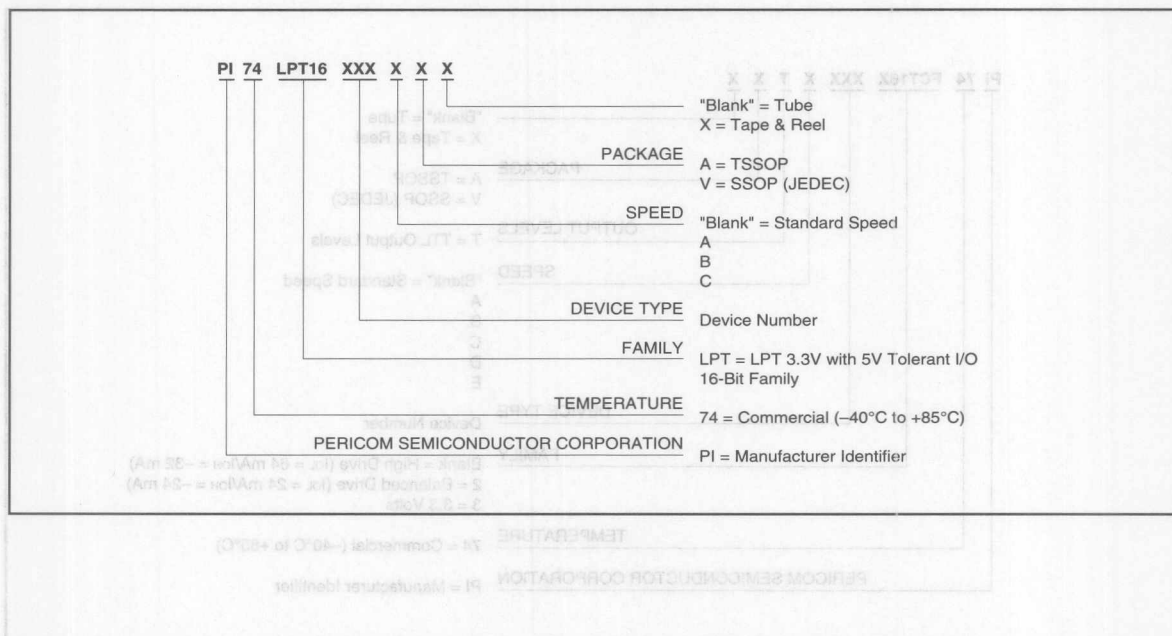


ORDERING INFORMATION

Ordering Number Information — LPTXXXX



Ordering Number Information — LPT16XXX (Double Density)



TAPE AND REEL PACKING REQUIREMENTS

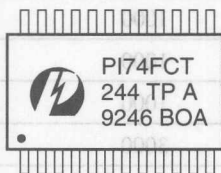
PART MARKING INFORMATION

1

The Part Marking is identical to the Ordering Number with the following exceptions:

- Speed is marked at the end of the part number so that the speed grade indicator can be added after test. The manufacturing date code is marked under the device part number.
- The 8-pin DIP, 8-pin SOIC, 14-pin SOIC and all QSOP packages are not marked with the Pericom Semiconductor logo due to space limitations on the package.

EXAMPLE:



SOIC-16	2 W	16	8	40 (11.8")	1000	62 (50")
SOIC-20	2	24	12	25 (11.8")	3000	62 (50")
SOIC-24	2	24	12	25 (11.8")	3000	62 (50")
SOIC-28	2	24	12	25 (11.8")	3000	62 (50")
QSOP-16	Q	16	8	40 (11.8")	1000	62 (50")
QSOP-20	Q	16	8	40 (11.8")	3000	62 (50")
QSOP-24	Q	16	8	40 (11.8")	3000	62 (50")
TSSOP-20	L R	16	8	40 (11.8")	3000	62 (50")
TSSOP-24	R	16	8	40 (11.8")	3000	62 (50")
SSOP-48	V	32	16	25 (11.8")	1000	42 (50")
SSOP-56	V	32	16	25 (11.8")	1000	42 (50")
TSSOP-48	A	24	12	25 (11.8")	1500	42 (50")
TSSOP-56	A	24	12	25 (11.8")	1500	42 (50")
PLCC-30	1	16	12	25 (11.8")	1000	42 (50")
PLCC-44	1	32	24	12 (12.3")	200	22 (50")

TAPE AND REEL PACKING REQUIREMENTS

Package Type	Package Code(s)	Tape Width (mm)	Pitch (mm)	Min. No. Pockets (Tape Trailer)	Devices Per Reel	Min. No. Pockets (Tape Leader)
SOIC-8	W	16	8	40 (11.8")	1000	65 (20")
SOIC-14	S, W	16	8	40 (11.8")	1000	65 (20")
SOIC-16	S, W	16	8	40 (11.8")	1000	65 (20")
SOIC-20	S	24	12	25 (11.8")	1000	45 (20")
SOIC-24	S	24	12	25 (11.8")	1000	45 (20")
SOIC-28	S	24	12	25 (11.8")	1000	45 (20")
QSOP-16	Q	16	8	40 (11.8")	3000	65 (20")
QSOP-20	Q	16	8	40 (11.8")	3000	65 (20")
QSOP-24	Q	16	8	40 (11.8")	3000	65 (20")
TSSOP-20	L, R	16	8	40 (11.8")	3000	65 (20")
TSSOP-24	R	16	8	40 (11.8")	3000	65 (20")
SSOP-48	V	32	16	25 (11.8")	1000	42 (20")
SSOP-56	V	32	16	25 (11.8")	1000	42 (20")
TSSOP-48	A	24	12	25 (11.8")	1500	42 (20")
TSSOP-56	A	24	12	25 (11.8")	1500	42 (20")
PLCC-20	J	16	12	25 (11.8")	1000	45 (20")
PLCC-44	J	32	24	15 (12.3")	500	22 (20")

PACKAGE CROSS REFERENCE

1

Package Type	Pin mils	Pitch mm	Length mils mm	Width mils mm	Height mils mm	TI Code	IDT Code	QSI Code	Cyp. Code	AMD Code	Nat'l Code	Phil. Code	Pericom Code
SOIC 8	50	1.27	190 4.82	150 3.82	63 1.59								W
SOIC 14	50	1.27	340 8.64	150 3.82	63 1.59			S1					W
SOIC 14	50	1.27	340 8.64	295 7.50	63 1.59								S
SOIC 16	50	1.27	390 9.90	150 3.82	100 2.54			S1			M		W
SOIC 16	50	1.27	400 10.15	295 7.50	100 2.54		SO	SO	SO		WM/SC		S
SOIC 20	50	1.27	500 12.70	295 7.50	100 2.54	DW	SO	SO	SO		WM/SC	D	S
SOIC 24	50	1.27	600 15.25	295 7.50	100 2.54	DW	SO	SO	SO	SC	WM/SC	D	S
QSOP 16	25	0.64	190 4.82	150 3.82	63 1.60			Q	Q		QSC		Q
QSOP 20	25	0.64	340 8.64	150 3.82	63 1.60		Q	Q	Q		QSC		Q
QSOP 24	25	0.64	340 8.64	150 3.82	63 1.60		Q	Q	Q		QSC		Q
TQSOP 20	25	0.64	340 8.64	150 3.82	43 1.10						MTC		R
TQSOP 24	25	0.64	340 8.64	150 3.82	43 1.10						MTC		R
TSSOP 20	25.59	0.65	256 6.50	173 4.40	43 1.10	PW					MSC		L
SSOP 48	25	0.64	625 15.88	300 7.62	102 2.60	DL	PV				MEA		V
SSOP 56	25	0.64	725 18.42	300 7.62	102 2.60	DL	PV				MEA		V
TSSOP 48	25	0.50	492 12.50	240 6.10	43 1.10	DGG	PA				MTD		A
TSSOP 56	25	0.50	551 14.00	240 6.10	43 1.10	DGG	PA				MTD		A
PLCC 20	50	1.27	390 9.91	390 9.91	180 4.57		J	JR				A	J
PLCC 44	50	1.27	680 17.26	680 17.26	170 4.32		J	JR				A	J
PDIP 8	100	2.54	385 9.77	300 7.62	165 4.20	N	P	P	P		PC	N	P
PDIP 14	100	2.54	760 19.30	300 7.62	165 4.20	N	P	P	P		PC	N	P
PDIP 16	100	2.54	760 19.30	300 7.62	165 4.20	N	P	P	P		PC	N	P
PDIP 20	100	2.54	1040 26.41	300 7.62	165 4.20	N	P	P	P		PC	N	P
PDIP 24	100	2.54	1260 32.00	300 7.62	165 4.20	N	P	P	P	PC	PC	N	P
Tape & Reel						R		X	T		X	T	X

Package Type	Pin Pitch mm	Length mm	Width mm	Height mm	TT Code	DT Code	QST Code	C/p. Code	AMD Code	Ref. Code	Part Code
SOIC 8	50	1.27	100	4.82	150	3.82	63	1.29			W
SOIC 14	50	1.27	140	8.64	150	3.82	63	1.29			W
SOIC 14	50	1.27	140	8.64	202	7.50	63	1.29			Z
SOIC 16	50	1.27	160	9.30	150	3.82	100	2.54		M	W
SOIC 16	50	1.27	160	10.12	202	7.50	100	2.54		WMSC	Z
SOIC 20	50	1.27	200	12.70	202	7.50	100	2.54	DW	WMSC D	Z
SOIC 24	50	1.27	200	12.70	202	7.50	100	2.54	DW	WMSC D	Z
QSOIC 16	25	0.64	100	4.82	150	3.82	63	1.60		QSC	Q
QSOIC 20	25	0.64	140	8.64	150	3.82	63	1.60		QSC	Q
QSOIC 24	25	0.64	140	8.64	150	3.82	63	1.60		QSC	Q
TQSOIC 20	25	0.64	140	8.64	150	3.82	43	1.10		MTIC	R
TQSOIC 24	25	0.64	140	8.64	150	3.82	43	1.10		MTIC	R
TSSOP 20	25	0.65	120	4.40	173	4.40	43	1.10	PW	MSC	L
TSSOP 48	25	0.64	625	12.88	300	7.62	102	2.60	DL	MEA	V
TSSOP 56	25	0.64	725	18.42	300	7.62	102	2.60	DL	MEA	V
TSSOP 48	25	0.50	492	12.50	240	6.10	43	1.10	DGG	PA	A
TSSOP 56	25	0.50	521	14.00	240	6.10	43	1.10	DGG	PA	A
PLCC 20	50	1.27	300	9.91	300	9.91	180	4.27		1R	A
PLCC 44	50	1.27	680	17.25	680	17.25	170	4.27		1R	A
PDIP 8	100	2.54	282	9.73	300	7.62	162	4.20	N	P	P
PDIP 14	100	2.54	360	10.30	300	7.62	162	4.20	N	P	P
PDIP 16	100	2.54	380	10.30	300	7.62	162	4.20	N	P	P
PDIP 20	100	2.54	440	10.41	300	7.62	162	4.20	N	P	P
PDIP 24	100	2.54	480	12.00	300	7.62	162	4.20	N	P	P
Type & Ref.							R	X	T	X	X

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PI29FCT52T
PI29FCT53T

Fast CMOS
Registered Transceivers

2

Product Features:

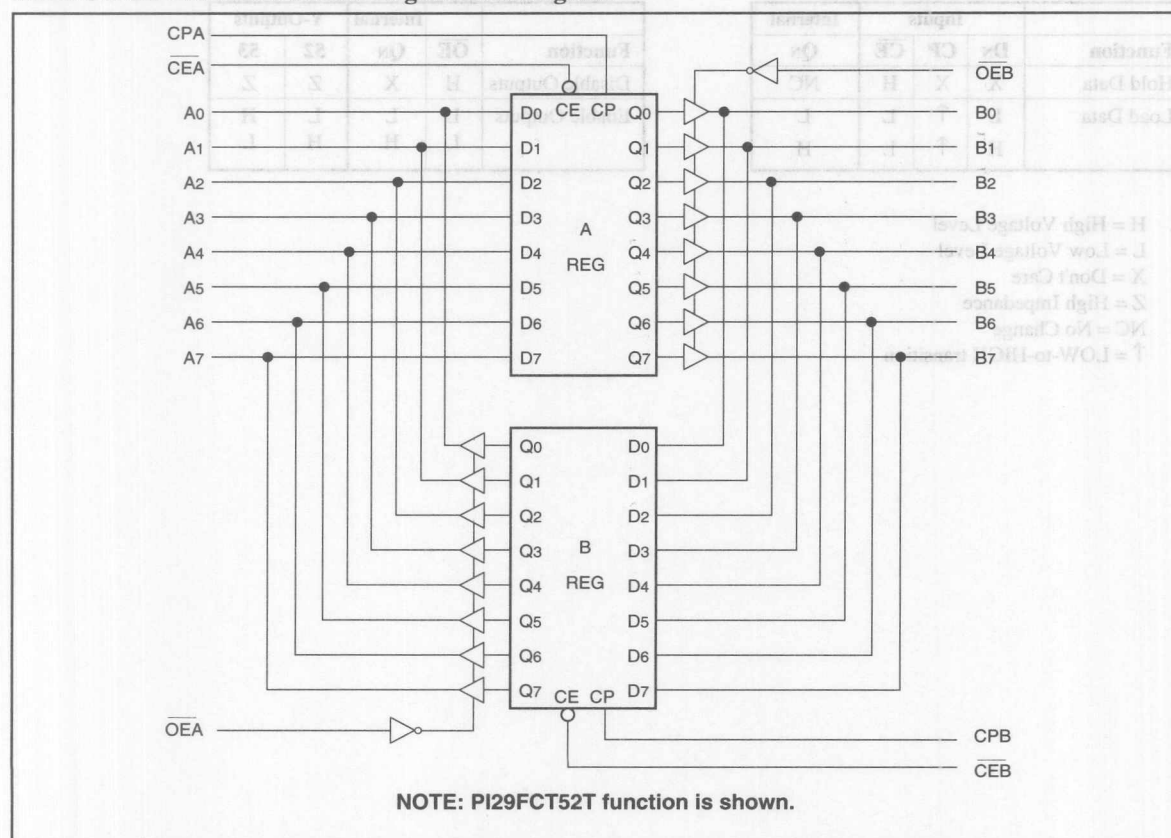
- PI29FCT52/53T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

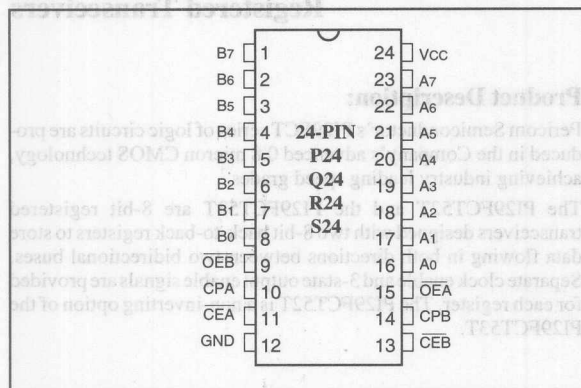
Pericom Semiconductor's PI29FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI29FCT52T and the PI29FCT53T are 8-bit registered transceivers designed with two 8-bit back-to-back registers to store data flowing in both directions between two bidirectional buses. Separate clock enable and 3-state output enable signals are provided for each register. The PI29FCT52T is a non-inverting option of the PI29FCT53T.

PI29FCT52T and PI29FCT53T Logic Block Diagram



PI29FCT52/53T Product Pin Configuration



Product Pin Description

Pin Name	Description
A0-A7	A Register Inputs or B Register Outputs
B0-B7	B Register Inputs or A Register Outputs
CPA	Clock for A Register
CPB	Clock for B Register
OEA	Output Enable for B Register
OEB	Output Enable for A Register
CEA	Clock Enable for A Register
CEB	Clock Enable for B Register
GND	Ground
Vcc	Power

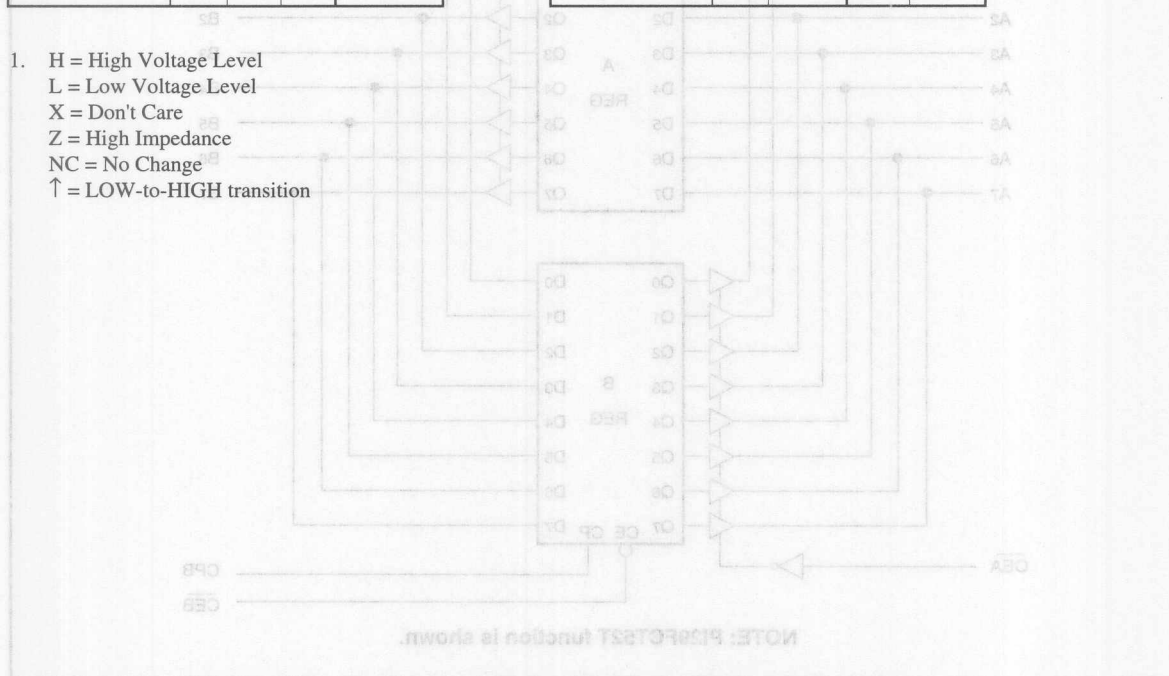
PI29FCT52/53T Register Truth Table⁽¹⁾
(Applies to A or B Register)

Function	Inputs			Internal
	D _N	CP	CE	Q _N
Hold Data	X	X	H	NC
Load Data	L	↑	L	L
	H	↑	L	H

PI29FCT52/53T Output Control Table⁽¹⁾

Function	OE	Q _N	Y-Outputs	
			52	53
Disable Outputs	H	X	Z	Z
Enable Outputs	L	L	L	H
	L	H	H	L

- H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance
 NC = No Change
 ↑ = LOW-to-HIGH transition



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IiH	Input HIGH Current	VCC = Max., VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max., VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max., VOUT = 2.7V			1	μA
IOZL	Output Current	VCC = Max., VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
Ioff	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	μA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OEA or OEB = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OEA or OEB = GND f _i = 5 MHz One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		2.0	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.5	6.0 ⁽⁵⁾	
					4.3	7.8 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OEA or OEB = GND Eight Bits Toggling f _i = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		6.5	16.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND				

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

$$I_c = I_{cc} + \Delta I_{cc} \cdot D_H \cdot N_i + I_{ccd} \cdot (f_{CP}/2 + f_i \cdot N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_i = Number of TTL Inputs at D_H

I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI29FCT52T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	29FCT52AT		29FCT52BT		29FCT52CT		Unit
			Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	ns
tPHL	CPA, CPB, to AN, BN								
tpZH	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	ns
tpZL	OE \overline{A} , OE \overline{B} , to AN, BN								
tpHZ	Output Disable Time ⁽³⁾		1.5	10.0	1.5	7.5	1.5	6.5	ns
tpLZ	OE \overline{A} , OE \overline{B} , to AN, BN								
tsu	Set-up Time HIGH or LOW, AN, BN to CPA, CPB		2.5	—	2.5	—	2.5	—	ns
th	Hold Time HIGH or LOW, AN, BN to CPA, CPB		2.0	—	1.5	—	1.5	—	ns
tsu	Set-up Time HIGH or LOW, CEA, CEB to CPA, CPB		3.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB		2.0	—	2.0	—	2.0	—	ns
tw	Pulse Width HIGH ⁽³⁾ or LOW, CPA or CPB		3.0	—	3.0	—	3.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI29FCT53T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	29FCT53AT		29FCT53BT		29FCT53CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay CPA, CPB, to AN, BN	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	ns
tPHL	Output Enable Time OEA, OEB, to AN, BN		1.5	10.5	1.5	8.0	1.5	7.0	ns
tPZH	Output Disable Time ⁽³⁾ OEA, OEB, to AN, BN		1.5	10.0	1.5	7.5	1.5	6.5	ns
tPLZ	Set-up Time HIGH or LOW, AN, BN to CPA, CPB		2.5	—	2.5	—	2.5	—	ns
th	Hold Time HIGH or LOW, AN, BN to CPA, CPB		2.0	—	1.5	—	1.5	—	ns
tsu	Set-up Time HIGH or LOW, CEA, CEB to CPA, CPB		3.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, CEA, CEB to CPA, CPB		2.0	—	2.0	—	2.0	—	ns
tw	Pulse Width HIGH ⁽³⁾ or LOW, CPA or CPB		3.0	—	3.0	—	3.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.



PI29FCT520T PI29FCT521T

Fast CMOS Multilevel Pipeline Registers

2

Product Features:

- PI29FCT520T and PI29FCT521T are pinout and function compatible with IDT29FCT520/521, QS29FCT520/521 and AMD's Am29520/521
- Four 8-bit high-speed registers
- Hold, Transfer, and load instructions
- Dual two-level or single four-level pipeline operation
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive
I_{OL} = 48 mA
- Extremely low static power (1 mW, typ.)
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

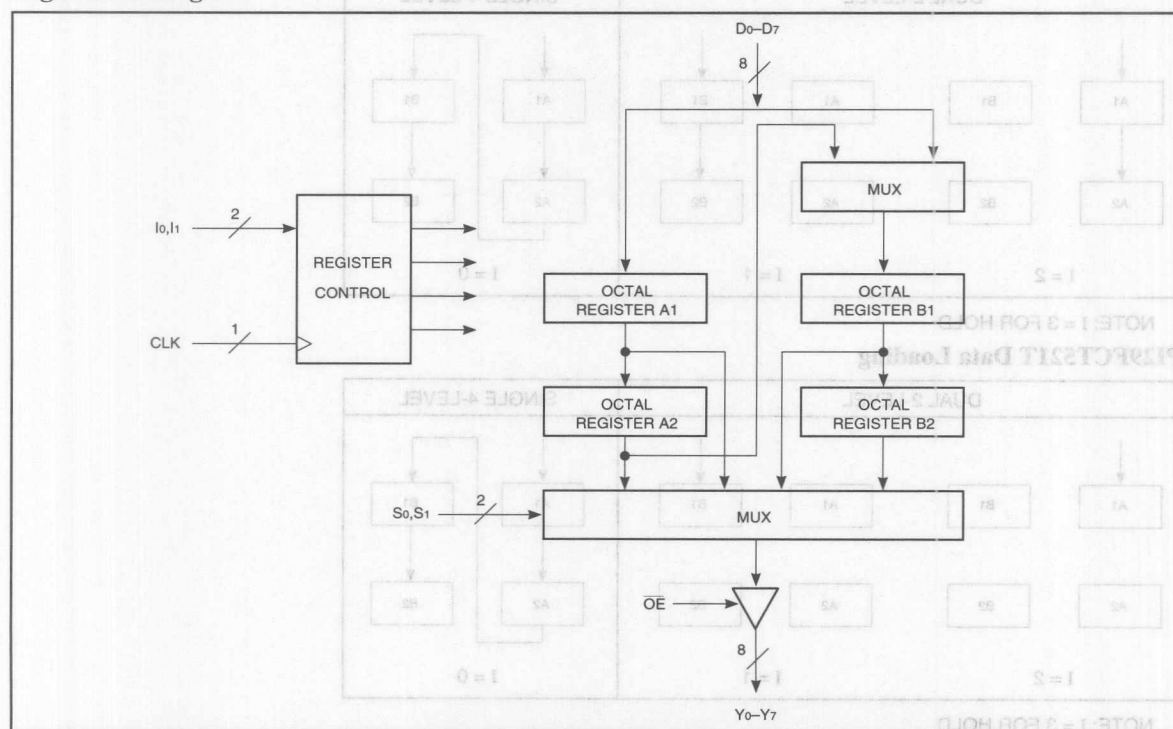
Product Description:

Pericom Semiconductor's PI29FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

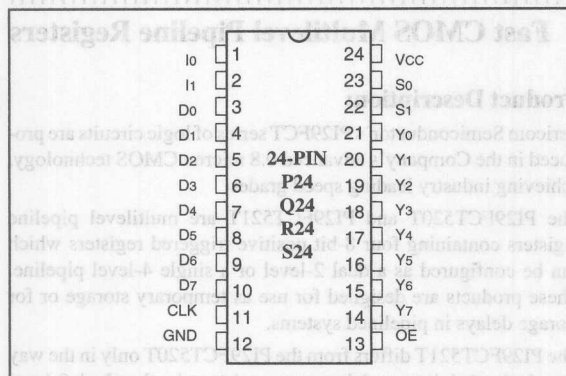
The PI29FCT520T and PI29FCT521T are multilevel pipeline registers containing four 8-bit positive triggered registers which can be configured as a dual 2-level or a single 4-level pipeline. These products are designed for use as temporary storage or for storage delays in pipelined systems.

The PI29FCT521T differs from the PI29FCT520T only in the way data is loaded into and between registers in the dual 2-level operation. When data is entered into the first level (I = 2 or I = 1) of the PI29FCT520T, the existing data in the first level is moved to the second level. In the PI29FCT521T, these instructions simply overwrite the data in the first level. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0) causing the first level to change. In either part, I = 3 shift instruction puts the registers on hold.

Logic Block Diagram



Product Pin Configuration



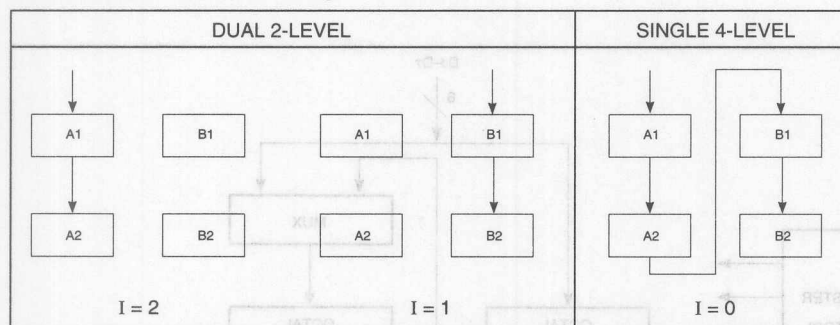
Product Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active LOW) for 3-State Output Port
CLK	Clock Input. Enter data into registers on LOW-to-HIGH transistions
I0,I1	Instruction Inputs
S0,S1	Multiplexer Select. Inputs either register A1, A2, B1, or B2 data to be avaiable at the output ports
Dx	Register Inputs
Yx	Register Outputs
GND	Ground
Vcc	Power

Register Selection

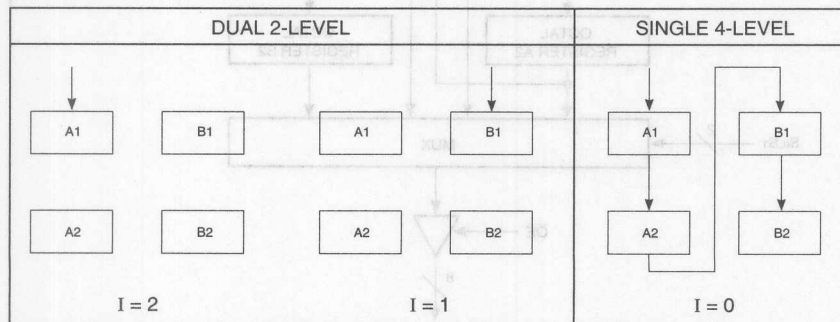
S1	S0	Register
0	0	B2
0	1	B1
1	0	A2
1	1	A1

PI29FCT520T Data Loading



NOTE: I = 3 FOR HOLD

PI29FCT521T Data Loading



NOTE: I = 3 FOR HOLD

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 48 mA		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IIH	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max. VOUT = 2.7V			1	μA
IOZL	Output Current	VCC = Max. VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	μA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE = GND One Input Toggling 50% Duty Cycle	V _{IN} = GND V _{IN} = V _{cc}		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁵⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND One Bit Toggling f _I = 5 MHz 50% Duty Cycle	V _{IN} = GND V _{IN} = V _{cc}		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V		2.2	6.0 ⁽⁵⁾	
			V _{IN} = GND				
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND Eight Bits Toggling f _I = 5 MHz 50% Duty Cycle	V _{IN} = GND V _{IN} = V _{cc}		7.0	12.8 ⁽⁵⁾	
			V _{IN} = 3.4V		9.2	21.8 ⁽⁵⁾	
			V _{IN} = GND				

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply characteristics.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

6. I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_c = I_{cc} + ΔI_{cc} D_H N_T + I_{ccD} (f_{CP}/2 + f_I N_I)

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

PI29FCT520T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT520AT		FCT520BT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay CLK to Y _x	C _L = 50 pF R _L = 500Ω	2.0	14.0	2.0	7.5	ns
t _{PLH} t _{PHL}	Propagation Delay S ₀ or S ₁ to Y _x		2.0	13.0	2.0	7.5	ns
t _{SU}	Setup Time HIGH or LOW D _x to CLK		5.0	—	2.5	—	ns
t _H	Hold Time HIGH or LOW D _x to CLK		2.0	—	2.0	—	ns
t _{SU}	Setup Time HIGH or LOW I ₀ or I ₁ to CLK		5.0	—	4.0	—	ns
t _H	Hold Time HIGH or LOW I ₀ or I ₁ to CLK		2.0	—	2.0	—	ns
t _{PZH} t _{PZL}	Output Enable Time OE to Y _x		1.5	12.0	1.5	7.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OE to Y _x		1.5	15.0	1.5	7.5	ns
t _W	Clock Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.5	—	ns

PI29FCT521T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT521AT		FCT521BT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	14.0	2.0	7.5	ns
tPHL	CLK to Yx						
tPLH	Propagation Delay		2.0	13.0	2.0	7.5	ns
tPHL	S0 or S1 to Yx						
tSU	Setup Time HIGH or LOW Dx to CLK		5.0	—	2.5	—	ns
tH	Hold Time HIGH or LOW Dx to CLK		2.0	—	2.0	—	ns
tSU	Setup Time HIGH or LOW I0 or I1 to CLK		5.0	—	4.0	—	ns
tH	Hold Time HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	ns
tPZH	Output Enable Time		1.5	12.0	1.5	7.0	ns
tPZL	OE to Yx						
tPHZ	Output Disable Time ⁽³⁾		1.5	15.0	1.5	7.5	ns
tPLZ	OE to Yx						
tW	Clock Pulse Width ⁽³⁾		7.0	—	5.5	—	ns
	HIGH or LOW						

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

Quad 2-Input NAND Schmitt Trigger

Product Features:

- PI74FCT132T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 14-pin 150 mil wide plastic SOIC (W14)

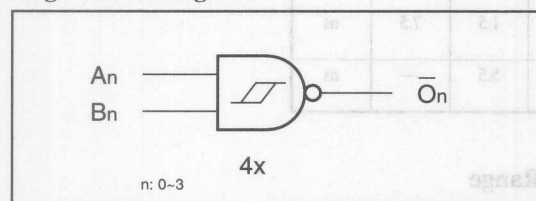
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

PI74FCT132 consists of four 2-input NAND gates that are able to transform slowly changing input signals into highly defined, jitter-free output signals.

Each gate contains a 2-input Schmitt trigger which uses positive feedback to speed-up slow input transitions, and offer different input threshold voltages for positive and negative-going transitions. Resistor-ratios are used to determine this hysteresis between the positive-going and negative-going input threshold.

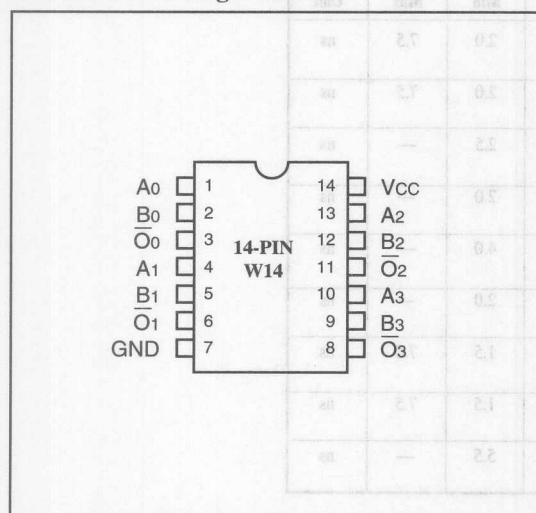
Logic Block Diagram



Product Pin Description

Pin Name	Description
A0-A3	Inputs
B0-B3	Inputs
O0-O3	Outputs
GND	Ground
VCC	Power

Product Pin Configuration



Truth Table ⁽¹⁾

Inputs		Outputs
A_n	B_n	\bar{O}_n
L	L	H
L	H	H
H	L	H
H	H	L

Note:

- H = HIGH Voltage Level
L = LOW Voltage Level

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 48 mA		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IiH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
VT+	Positive-going Threshold	VCC = 5.0V		1.5		2.0	V
VT-	Negative-going Threshold	VCC = 5.0V		0.7		1.1	V
ΔVT	Hysteresis (VT+ - VT-)	VCC = 5.0V		0.4			V
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA				-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120	-150	mA
ICCH	Power Supply Current	VCC = Max.	Vo = HIGH			17.0	mA
ICCL	Power Supply Current	VCC = Max.	Vo = LOW			18.0	mA

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.3	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle Toggle E1, E2, or E3 One Bit toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{CP}/2 + f_i N_i)$
I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Output Frequency
N_i = Number of Outputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT132 Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	132T		132AT		132CT		132DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF	3.0	10.0	3.0	8.0	3.0	6.0	3.0	5.0	ns
t _{PHL}	AN, BN to $\overline{\text{ON}}$	R _L = 500Ω									

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	8	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Note: This parameter is determined by device characterization but is not production tested.



PI74FCT138T
PI74FCT238T

Fast CMOS 1-of-8 Decoder

Product Features:

- PI74FCT138/238T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

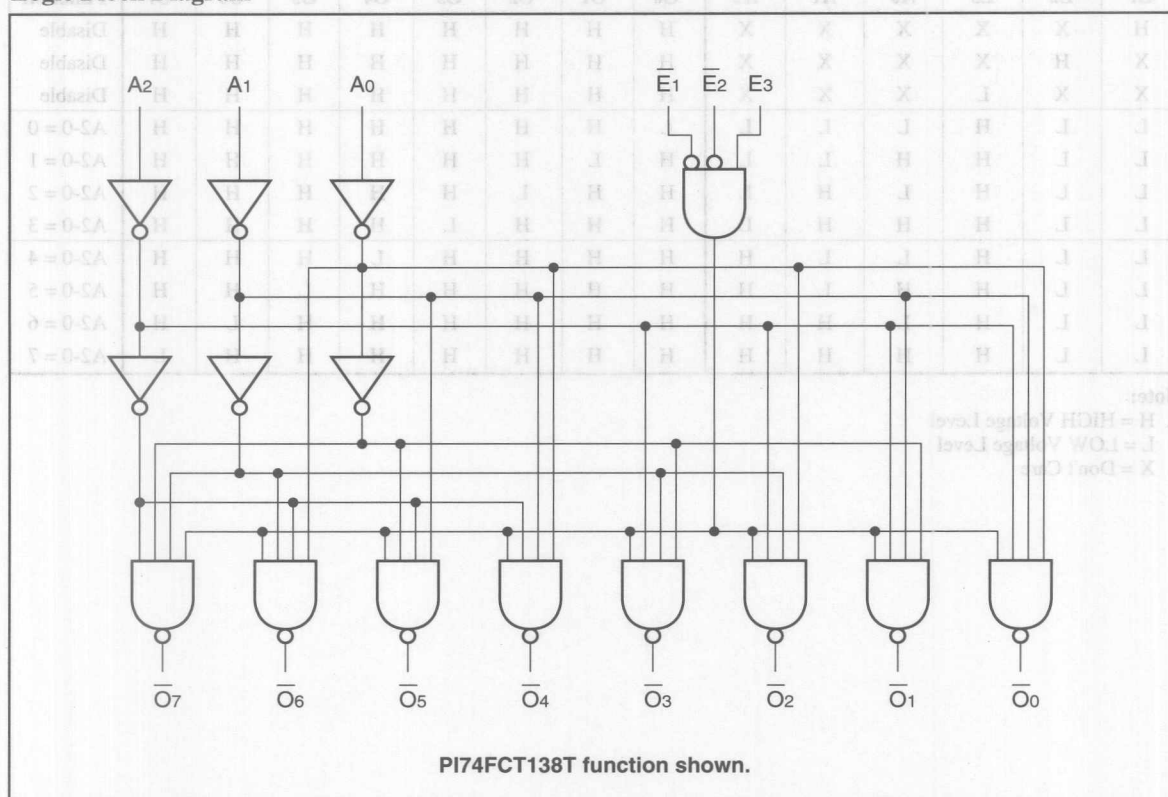
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

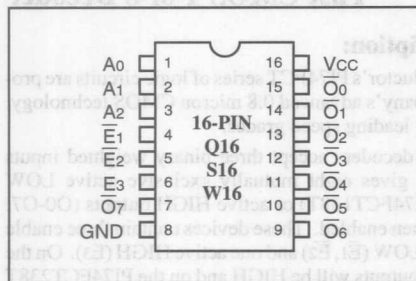
These high-speed decoders accept three binary weighted inputs (A_0 , A_1 , A_2) and gives eight mutually exclusive active LOW outputs ($\overline{O_0}$ – $\overline{O_7}$: PI74FCT138T) or active HIGH outputs (O_0 – O_7 : PI74FCT238T) when enabled. These devices contain three enable inputs, two active LOW ($\overline{E_1}$, $\overline{E_2}$) and one active HIGH (E_3). On the PI74FCT138T all outputs will be HIGH and on the PI74FCT238T all outputs will be LOW, except when $\overline{E_1}$ and $\overline{E_2}$ are LOW and E_3 is HIGH.

2

Logic Block Diagram



PI74FCT138T Product Pin Configuration



PI74FCT138T Product Pin Description

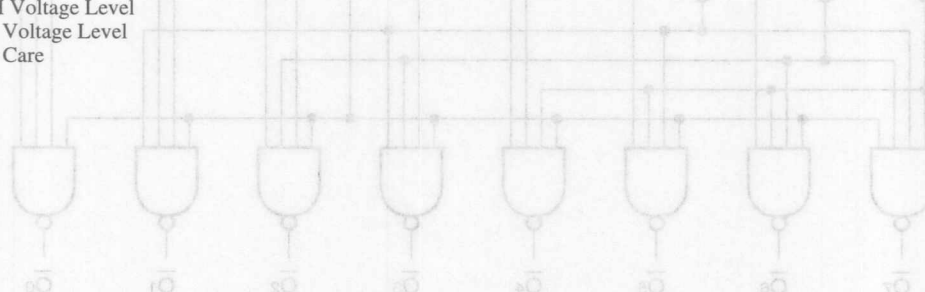
Pin Name	Description
A0-A2	Address Inputs
E1, E2	Enable Inputs (Active LOW)
E3	Enable Input (Active HIGH)
O0-O7	Outputs (Active LOW)

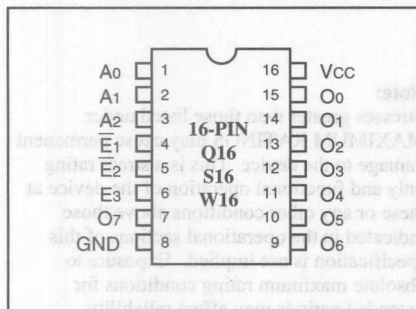
PI74FCT138T Truth Table (1)

Inputs						Outputs								Function
$\bar{E}1$	$\bar{E}2$	E3	A0	A1	A2	$\bar{O}0$	$\bar{O}1$	$\bar{O}2$	$\bar{O}3$	$\bar{O}4$	$\bar{O}5$	$\bar{O}6$	$\bar{O}7$	
H	X	X	X	X	X	H	H	H	H	H	H	H	H	Disable
X	H	X	X	X	X	H	H	H	H	H	H	H	H	Disable
X	X	L	X	X	X	H	H	H	H	H	H	H	H	Disable
L	L	H	L	L	L	L	H	H	H	H	H	H	H	A2-0 = 0
L	L	H	H	L	L	H	L	H	H	H	H	H	H	A2-0 = 1
L	L	H	L	H	L	H	H	L	H	H	H	H	H	A2-0 = 2
L	L	H	H	H	L	H	H	H	L	H	H	H	H	A2-0 = 3
L	L	H	L	L	H	H	H	H	H	L	H	H	H	A2-0 = 4
L	L	H	H	L	H	H	H	H	H	H	L	H	H	A2-0 = 5
L	L	H	L	H	H	H	H	H	H	H	H	L	H	A2-0 = 6
L	L	H	H	H	H	H	H	H	H	H	H	H	L	A2-0 = 7

Note:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



PI74FCT238T Product Pin Configuration

PI74FCT238T Product Pin Description

Pin Name	Description
A0-A2	Address Inputs
$\bar{E}1, \bar{E}2$	Enable Inputs (Active LOW)
E3	Enable Input (Active HIGH)
O0-O7	Outputs (Active HIGH)

2
PI74FCT238T Truth Table (1)

Inputs						Outputs								Function
$\bar{E}1$	$\bar{E}2$	E3	A0	A1	A2	O0	O1	O2	O3	O4	O5	O6	O7	
H	X	X	X	X	X	L	L	L	L	L	L	L	L	Disable
X	H	X	X	X	X	L	L	L	L	L	L	L	L	Disable
X	X	L	X	X	X	L	L	L	L	L	L	L	L	Disable
L	L	H	L	L	L	H	L	L	L	L	L	L	L	A2-0 = 0
L	L	H	H	L	L	L	H	L	L	L	L	L	L	A2-0 = 1
L	L	H	L	H	L	L	L	H	L	L	L	L	L	A2-0 = 2
L	L	H	H	H	L	L	L	L	H	L	L	L	L	A2-0 = 3
L	L	H	L	L	H	L	L	L	L	H	L	L	L	A2-0 = 4
L	L	H	H	L	H	L	L	L	L	L	H	L	L	A2-0 = 5
L	L	H	L	H	H	L	L	L	L	L	L	H	L	A2-0 = 6
L	L	H	H	H	H	L	L	L	L	L	L	L	H	A2-0 = 7

Note:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Parameter	Description	Test Conditions	Typ	Max	Units
C_{in}	Input Capacitance	$V_{in} = 0V$	5	10	pF
C_{out}	Output Capacitance	$V_{out} = 0V$	8	15	pF

Notes:
 1. For conditions show as Max. or Min., use appropriate values specified under Electrical Characteristics for the applicable device type.
 2. Typical values are at $V_{CC} = 5.0V$, $-55^{\circ}C$ ambient and maximum loading.
 3. Not more than one output should be asserted at one time. Duration of the test should not exceed one second.
 4. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -15.0 \text{ mA}$	2.4	3.0		V
V_{OL}	Output LOW Current	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 48 \text{ mA}$		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$			-1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_{OUT} = \text{GND}$	-60	-120	-225	mA
I_{OFF}	Power Down Disable	$V_{CC} = \text{GND}, V_{OUT} = 4.5\text{V}$	—	—	100	μA
V_H	Input Hysteresis			200		mV

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.3	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle Toggle E ₁ , E ₂ , or E ₃ One Bit toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.5 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{CC} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_O = Output Frequency

N_O = Number of Outputs at f_O

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT138T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	138T		138AT		138CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	5.8	1.5	5.1	ns
tPHL	A _n to \bar{O}_n								
tPLH	Propagation Delay		1.5	9.0	1.5	5.9	1.5	5.2	ns
tPHL	\bar{E}_1 or \bar{E}_2 to \bar{O}_n								
tPLH	Propagation Delay		1.5	9.0	1.5	5.9	1.5	5.2	ns
tPHL	E ₃ to \bar{O}_n								

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

PI74FCT238T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	238T		238AT		238CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	5.8	1.5	5.0	ns
tPHL	An to On								
tPLH	Propagation Delay		1.5	8.0	1.5	5.9	1.5	5.0	ns
tPHL	E1 or E2 to On								
tPLH	Propagation Delay		1.5	8.0	1.5	5.9	1.5	5.0	ns
tPHL	E3 to On								

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Fast CMOS Dual 1-of-4 Decoder

Product Features:

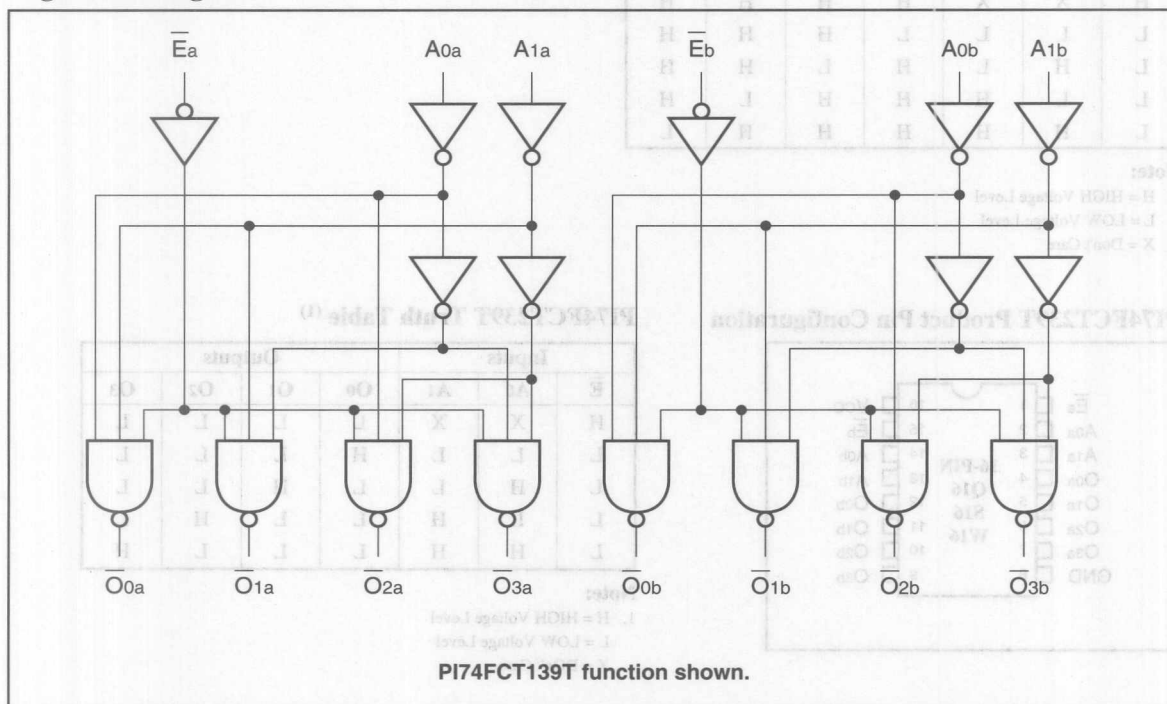
- PI74FCT139/239T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

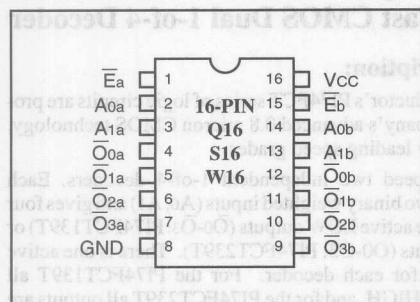
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

These are high-speed two independent 1-of-4 decoders. Each decoder accepts two binary weighted inputs (A0, A1) and gives four mutually exclusive active LOW outputs (O0-O3: PI74FCT139T) or active HIGH outputs (O0-O3: PI74FCT239T). There is one active LOW enable (E) for each decoder. For the PI74FCT139T all outputs are forced HIGH, and for the PI74FCT239T all outputs are forced LOW when E is HIGH.

Logic Block Diagram



PI74FCT139T Product Pin Configuration

PI74FCT139T Product Pin Description

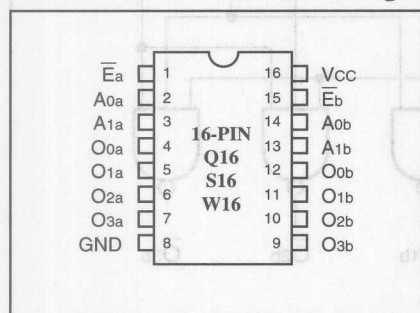
Pin Name	Description
A0, A1	Address Inputs
\bar{E}	Enable Input (Active LOW)
O0-O3	Outputs (Active LOW)

PI74FCT139T Truth Table ⁽¹⁾

Inputs			Outputs			
\bar{E}	A0	A1	O0	O1	O2	O3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Note:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

PI74FCT239T Product Pin Configuration

PI74FCT239T Truth Table ⁽¹⁾

Inputs			Outputs			
\bar{E}	A0	A1	O0	O1	O2	O3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H

Note:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = DON't Care

PI74FCT239T Product Pin Description

Pin Name	Description
A0, A1	Address Inputs
\bar{E}	Enable Input (Active LOW)
O0-O3	Outputs (Active HIGH)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL	IOL = 48 mA		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IiH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA			-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120	-225	mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
VH	Input Hysteresis				200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max. Outputs Open One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.3	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max. Outputs Open f _{CP} = 10 MHz 50% Duty Cycle One Bit toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.5	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.5	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle One Bit toggling on Each Decoder	V _{IN} = V _{cc} V _{IN} = GND		3.2	7.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		3.7	9.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- $I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccD} (f_{CP}/2 + f_i N_i)$
 I_{cc} = Quiescent Current
 ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Output Frequency
 N_i = Number of Outputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	8	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

- Notes:
- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
 - Typical values are at V_{cc} = 5.0V, +25°C ambient and maximum loading.
 - Not more than one output should be started at one time. Duration of the test should not exceed one second.
 - This parameter is determined by device characterization for in production tested.

PI74FCT139T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	139T		139AT		139CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	5.9	1.5	5.0	ns
t _{PHL}	A ₀ or A ₁ to O _n								
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	5.5	1.5	4.8	ns
t _{PHL}	\bar{E} to O _n								

Notes:

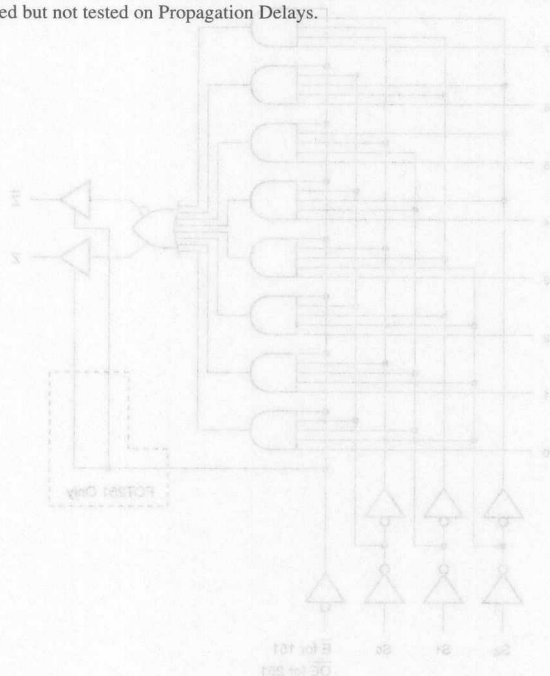
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

PI74FCT239T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	239T		239AT		239CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	5.9	1.5	5.0	ns
t _{PHL}	A ₀ or A ₁ to O _n								
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	5.5	1.5	4.8	ns
t _{PHL}	\overline{E} to O _n								

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.





PI74FCT151T/251T

Fast CMOS 8-Input Multiplexer

Product Features:

- PI74FCT151/251T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

Product Description:

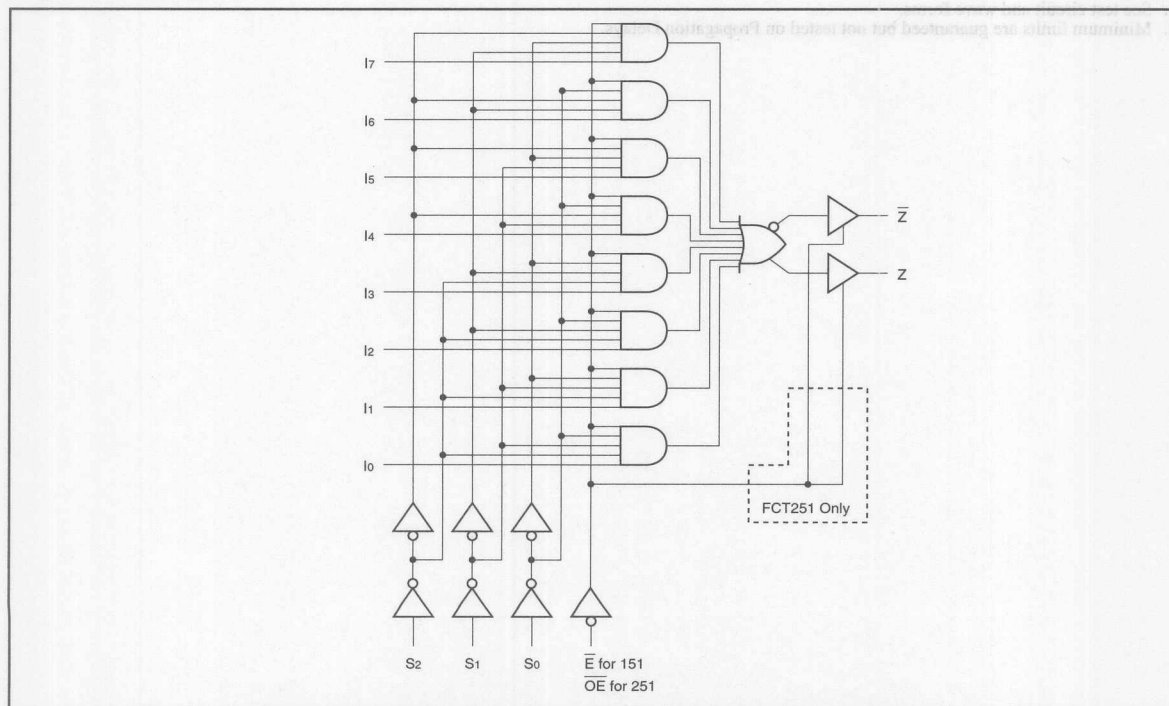
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT151T and PI74FCT251T are high-speed 8-input multiplexers. They select one bit from a source of eight under the control of three select inputs. Both assertion and negation outputs are provided.

The PI74FCT151T has a common, active-LOW, Enable input (\bar{E}). When \bar{E} is LOW, data from one of eight inputs is directed to the complementary outputs based on the 3-bit code applied to the Select (S_0 - S_2) inputs. The PI74FCT151T can be used as a data routing device from one of eight sources.

The PI74FCT251 has a common Active-LOW Output Enable (\bar{OE}) input. When \bar{OE} is LOW, data from one of eight inputs is directed to the complementary outputs. When \bar{OE} is HIGH, both outputs are switched to a high-impedance state allowing multiplexer expansion by tying several outputs together.

Logic Block Diagram



Product Pin Description

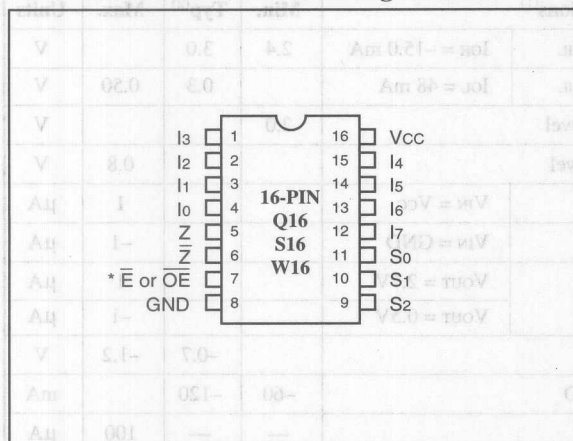
Pin Name	Description
I0-I7	Data Inputs
S0-S2	Select Inputs
\overline{E}	Enable Input (Active LOW) FCT151T
\overline{OE}	Output Enable (Active LOW) FCT251T
Z	Data Output
\overline{Z}	Inverted Data Output
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs				Outputs	
S2	S1	S0	$\overline{E}/\overline{OE}^{(2)}$	Z	\overline{Z}
X	X	X	H	L(151)	H(151)
X	X	X	H	Z(251)	Z(251)
L	L	L	L	I0	$\overline{I0}$
L	L	H	L	I1	$\overline{I1}$
L	H	L	L	I2	$\overline{I2}$
L	H	H	L	I3	$\overline{I3}$
H	L	L	L	I4	$\overline{I4}$
H	L	H	L	I5	$\overline{I5}$
H	H	L	L	I6	$\overline{I6}$
H	H	H	L	I7	$\overline{I7}$

2

PI74FCT151T Product Pin Configuration



NOTES:

1. E for 151, OE for 251
2. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

* \overline{E} for 151 only, \overline{OE} for 251 only

Parameters ⁽³⁾	Description	Test Conditions	Typ	Max.	Units
C_{in}	Input Capacitance	$V_{in} = 0V$	8	10	pf
C_{out}	Output Capacitance	$V_{out} = 0V$	8	12	pf

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at $V_{cc} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
3. Not more than one output should be shorted to one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48 mA		0.3	0.50	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current		V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-60	-120		mA
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V		—	—	100	μA
V _H	Input Hysteresis				200		mV

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open \bar{E} or \bar{OE} = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle \bar{E} or \bar{OE} = GND One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		3.5	7.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_I = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT151T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	151T		151AT		151CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay S _n to Z	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
tPLH tPHL	Propagation Delay S _n to Z		1.5	10.5	1.5	6.8	1.5	5.8	ns
tPLH tPHL	Propagation Delay E to Z		1.5	7.0	1.5	5.6	1.5	4.8	ns
tPLH tPHL	Propagation Delay E to Z		1.5	9.5	1.5	5.8	1.5	5.0	ns
tPLH tPHL	Propagation Delay In to Z		1.5	6.5	1.5	5.2	1.5	4.4	ns
tPLH tPHL	Propagation Delay In to Z		1.5	7.5	1.5	5.5	1.5	4.7	ns

PI74FCT251T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	251T		251AT		251CT		Unit
			Com.		Com.		Com.		
tPLH	Propagation Delay S _n to \overline{Z}	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
tPHL	Propagation Delay S _n to Z		1.5	11.0	1.5	6.8	1.5	5.8	ns
tPLH	Propagation Delay I _n to \overline{Z}		1.5	7.0	1.5	5.2	1.5	4.4	ns
tPHL	Propagation Delay I _n to Z		1.5	7.0	1.5	5.5	1.5	4.7	ns
tPZH	Output Enable Time OE to Z		1.5	9.0	1.5	6.7	1.5	5.7	ns
tPZL	Output Disable Time ⁽³⁾ OE to \overline{Z}		1.5	7.5	1.5	6.0	1.5	5.0	ns
tPZH	Output Enable Time OE to Z	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.7	1.5	5.7	ns
tPZL	Output Disable Time ⁽³⁾ OE to Z		1.5	7.0	1.5	6.0	1.5	5.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.



PI74FCT153T/253T
(25 Ω Series) PI74FCT2153T/2253T

High-Speed CMOS Dual 4-Input Multiplexer

2

Product Features:

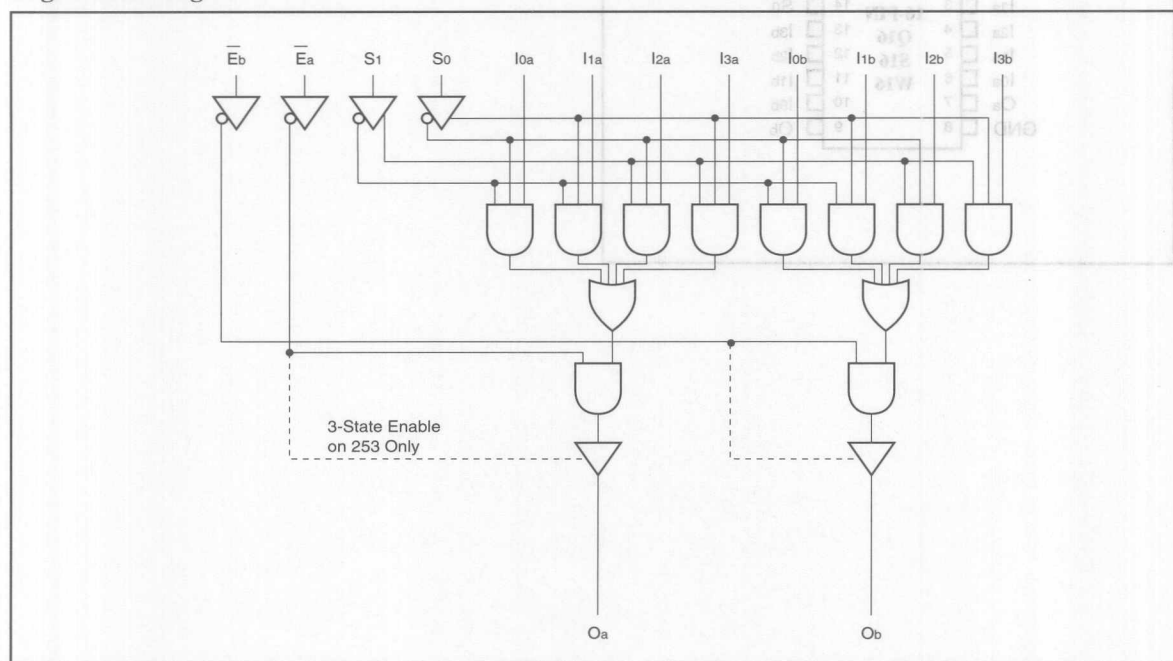
- PI74FCT153T/253T/2153T/2253T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25 Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs (25 Ω series only)
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT153T/253T and PI74FCT2153T/2253T are high-speed dual 4-input multiplexers. The PI74FCT153T/2153T has TTL outputs, while the PI74FCT253T/2253T has 3-state outputs. The output buffers are designed with a power-off disable allowing "live insertion" of boards when used as backplane drivers.

Logic Block Diagram



Product Pin Description

Pin Name	Description
I0a-I3a, I0b-I3b	Data Inputs
S0, S1	Select Inputs
$\bar{E}a, \bar{E}b$	Enable Input
Oa, Ob	Data Outputs
GND	Ground
Vcc	Power

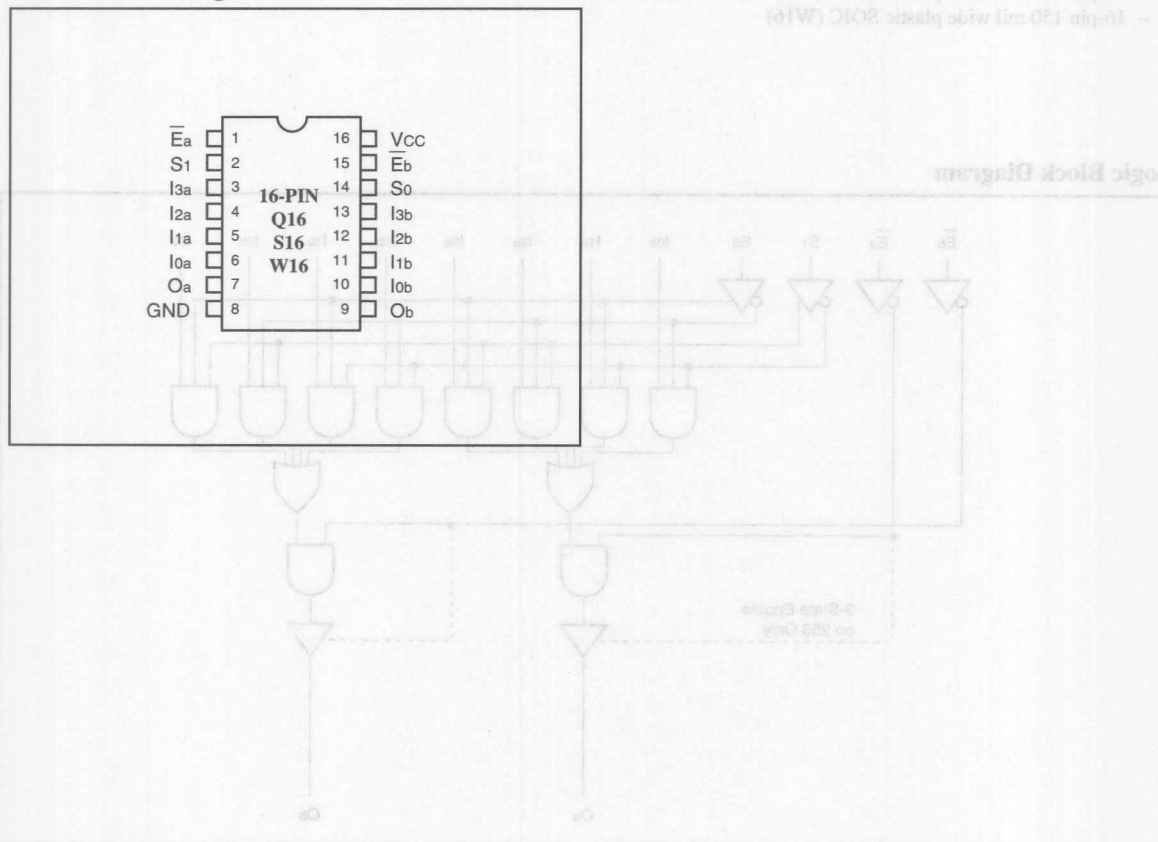
Truth Table⁽¹⁾

Inputs				Outputs			
				'153/2153		'253/2253	
$\bar{E}a$	$\bar{E}b$	S1	S0	Oa	Ob	Oa	Ob
H	X	X	X	L	X	Z	X
X	H	X	X	X	L	X	Z
L	L	L	L	I0a	I0b	I0a	I0b
L	L	L	H	I1a	I1b	I1a	I1b
L	L	H	L	I2a	I2b	I2a	I2b
L	L	H	H	I3a	I3b	I3a	I3b

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 48 mA		0.3	0.50	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 12 mA (25Ω Series)		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IIH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
IOZH	High Impedance	VCC = MAX.	VOUT = 2.7V			1	μA
IOZL	Output Current		VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2		V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120		mA
VH	Input Hysteresis				200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open Other inputs at GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle Other inputs at GND One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		3.5	7.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_H N_I + I_{CCD} (f_{CP}/2 + f_i N_I)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_I = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_I = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Parameters	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

- Notes:
- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
 - Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
 - Not more than one output should be shifted at one time. Duration of the test should not exceed one second.
 - This parameter is determined by device characterization but is not production tested.

PI74FCT153/2153T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	153T/2153T		153AT/2153AT		153CT/2153CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
TP _{LH} TP _{HL}	Propagation Delay S _n to O	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
TP _{LH} TP _{HL}	Propagation Delay I _n to O		1.5	7.0	1.5	5.2	1.5	4.5	ns

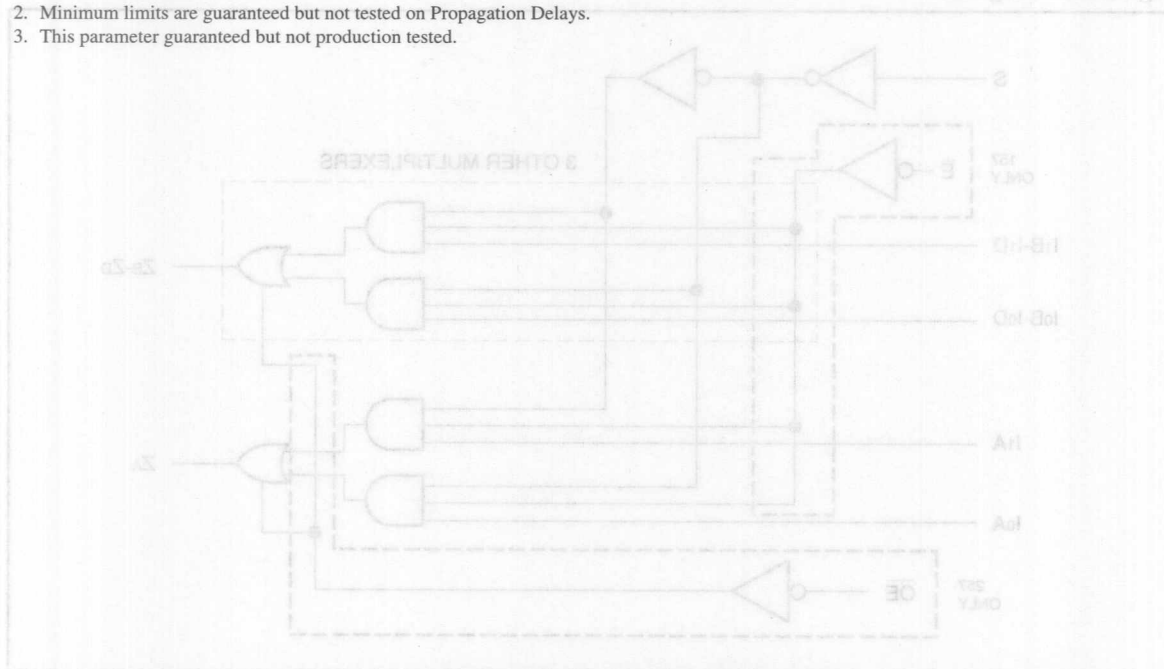
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PI74FCT253/2253T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	253T/2253T		253AT/2253AT		253CT/2253CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay S _n to O	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
t _{PLH} t _{PHL}	Propagation Delay I _n to O		1.5	7.0	1.5	5.2	1.5	4.5	ns
t _{PEZH} t _{PEZL}	Output Enable Time E to O		1.5	9.0	1.5	6.0	1.5	5.0	ns
t _{PDZH} t _{PDZL}	Output Disable Time ⁽³⁾ E to O		1.5	7.0	1.5	6.0	1.5	5.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.





PI74FCT157T/257T
(25Ω Series)PI74FCT2157T/2257T

Fast CMOS Quad 2-Input Multiplexer

Product Features:

- PI74FCT157/257/2157/2257T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs (25Ω series only)
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

Product Description:

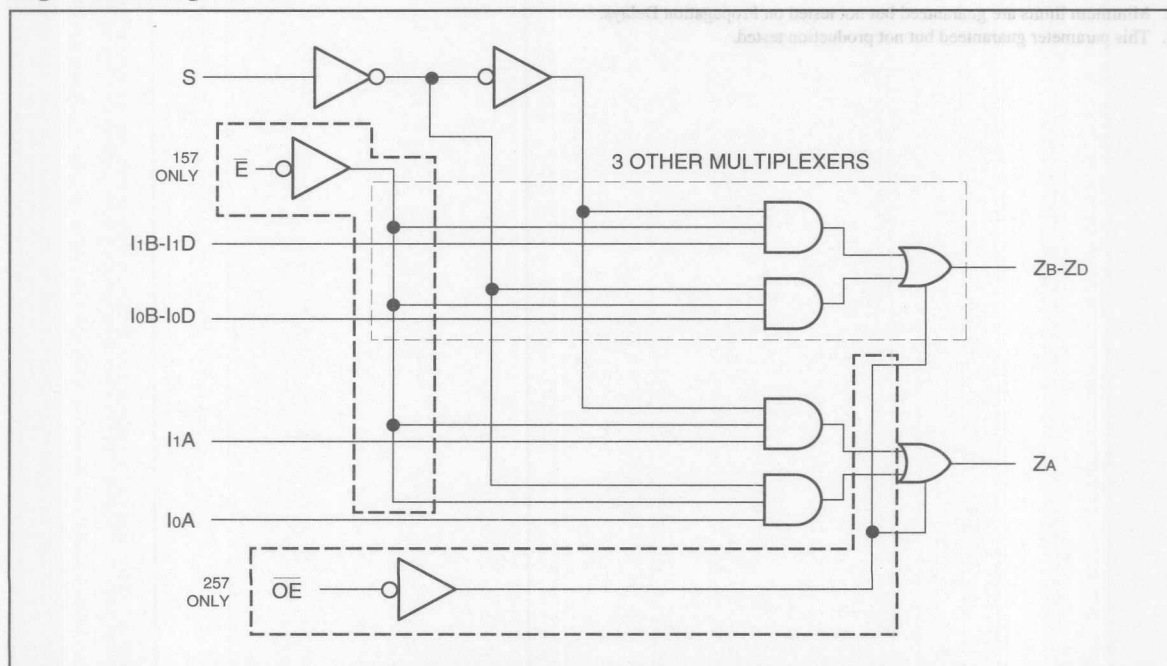
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT157T/257T and PI74FCT2157T/2257T are high-speed quad 2-input multiplexers. The common select input can be used to select four bits of data from two sources. The four buffered outputs present the selected data in the true (non-inverting) form.

The PI74FCT157T/2157T has a common, active-LOW, Enable input (E). When E is inactive, all four outputs are held LOW. The PI74FCT157T/2157T can generate any four of the 16 different functions of two variables with one common variable. The PI74FCT157T/2157T can be used as a function generator or to move data from two different groups of registers to a common bus.

The PI74FCT257/2257T has a common Output Enable (\overline{OE}) input. When \overline{OE} is HIGH, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

Logic Block Diagram



Product Pin Description

Pin Name	Description
IoA-IoD	Source 0 Data Inputs
I1A-I1D	Source 1 Data Inputs
\bar{E}	Enable Input (Active LOW) FCT157/2157
OE	Output Enable (Active LOW) FCT257/2257
S	Select Input
ZA-ZD	Outputs
GND	Ground
Vcc	Power

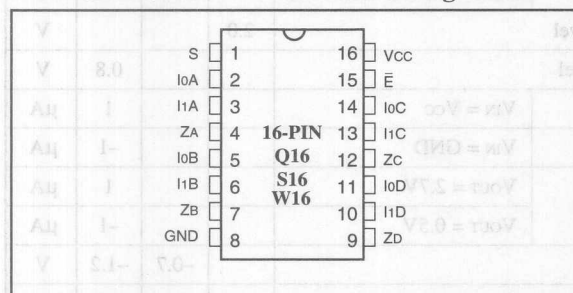
Truth Table⁽¹⁾

Inputs				Outputs Zn	
\bar{E}/OE	S	I0	I1	157/2157	257/2257
H	X	X	X	L	Z
L	H	X	L	L	L
L	H	X	H	H	H
L	L	L	X	L	L
L	L	H	X	H	H

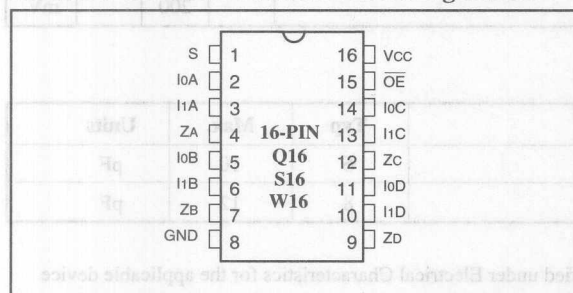
NOTE:

- H = High Voltage Level
X = Don't Care
L = Low Voltage Level
Z = High Impedance

PI74FCT157/2157T Product Pin Configuration



PI74FCT257/2257T Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 48 mA		0.3	0.50	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 12 mA (25Ω Series)		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IIH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max.	VOUT = 2.7V			1	μA
IOZL	Output Current		VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA			-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
IOS	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120		mA
VH	Input Hysteresis				200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open E or OE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle E or OE = GND One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle E or OE = GND Four Bits Toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		2.7	8.0 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{CP}/2 + f_i N_i)$$

I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT157/2157T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	157T/2157T		157AT/2157AT		157CT/2157CT		157DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	5.0	1.5	4.3	1.5	3.9	ns
tPHL	IN to ZN										
tPLH	Propagation Delay		1.5	10.5	1.5	6.0	1.5	4.8	1.5	4.4	ns
tPHL	E to ZN										
tPLH	Propagation Delay		1.5	10.5	1.5	7.0	1.5	5.2	1.5	4.6	ns
tPHL	S to ZN										

PI74FCT257/2257T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	257T/2257T		257AT/2257AT		257CT/2257CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay IN to ZN	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	5.0	1.5	4.3	ns
tPLH tPHL	Propagation Delay E to ZN		1.5	10.5	1.5	7.0	1.5	5.2	ns
tPZH tPZL	Output Enable Time OE to ZN		1.5	8.5	1.5	7.0	1.5	6.0	ns
tPZH tPZL	Output Disable Time ⁽³⁾ OE to ZN		1.5	6.0	1.5	5.5	1.5	5.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.



PI74FCT240T/241T/244T/540T/541T (25Ω Series) PI74FCT2240T/2241T/2244T/2541T

Fast CMOS Octal Buffer/Line Drivers

2

Product Features:

- PI74FCT240/241/244/540/541T and PI74FCT2240/2241/2244/2541T are pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

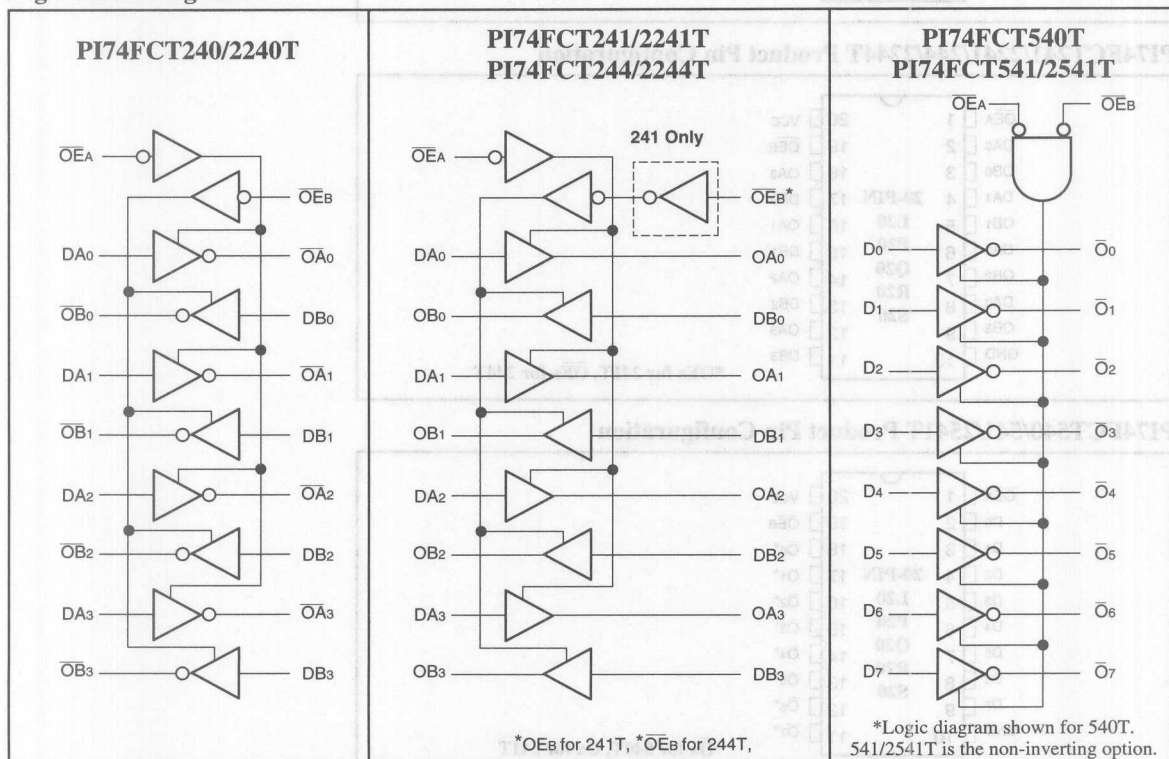
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT240T/241T/244T/540T/541T and PI74FCT2240T/2241T/2244T/2541T are 8-bit wide driver circuits, designed to be used in applications requiring high-speed and high-output drive. Ideal applications would include bus drivers, memory drivers, address drivers, and system clock drivers.

The PI74FCT540T and PI74FCT541/2541T provide similar driver capabilities, but have their pins physically grouped by function. All inputs are located on one side of the package, while outputs are on the opposite side, allowing for a much simpler and denser board layout.

Logic Block Diagrams





PI74FCT240T/241T/244T/540T/541T
(25Ω Series) PI74FCT2240T/2241T/2244T/2541T
OCTAL BUFFER/LINE DRIVERS

Product Pin Description

Pin Name	Description
\overline{OE}_A , \overline{OE}_B	3-State Output Enable Inputs (Active LOW)
$OE_B^{(1)}$	3-State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs
GND	Ground
Vcc	Power

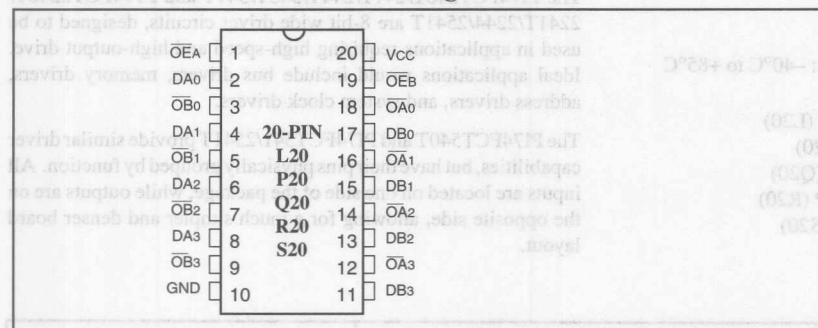
Truth Table

Inputs ⁽¹⁾				Outputs ⁽¹⁾				
\overline{OE}_A	\overline{OE}_B	$OE_B^{(2)}$	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

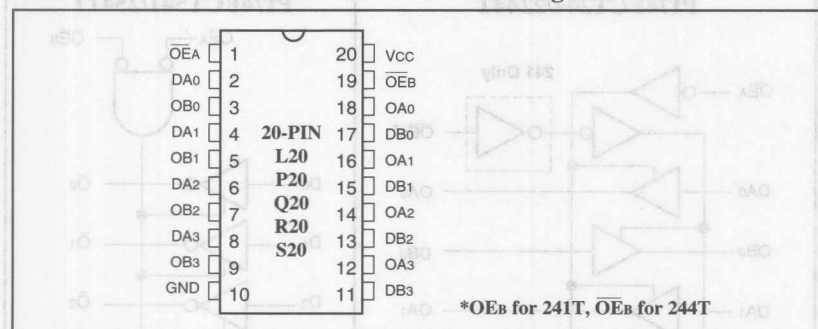
NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

2. OE_B for 241 only.

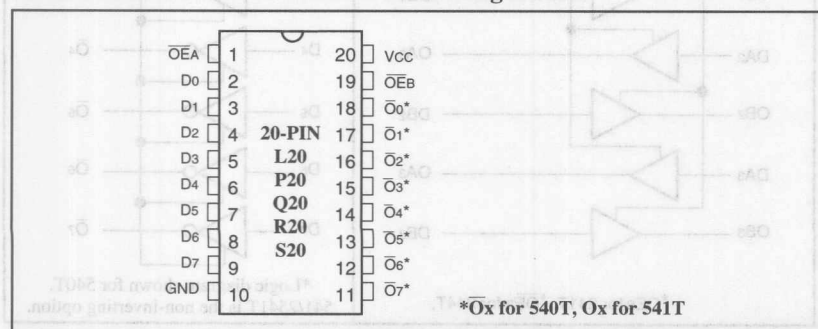
PI74FCT240/2240T Product Pin Configuration



PI74FCT241/2241/244/2244T Product Pin Configuration



PI74FCT540/541/2541T Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 64 mA		0.3	0.55	V
V _{OL}	Output LOW Current	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 12 mA (25Ω Series)		0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	VCC = Max. V _{IN} = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max. V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	VCC = Max. V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OFF}	Power Down Disable	VCC = GND, V _{OUT} = 4.5V	—	—	100	μA
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , V _{OUT} = GND	-60	-120		mA
V _H	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open O _{EA} = O _{EB} = GND or O _{EA} = GND, O _{EB} = V _{cc} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle O _{EA} = O _{EB} = GND or O _{EA} = GND, O _{EB} = V _{cc} One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
			V _{IN} = V _{cc} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle O _{EA} = O _{EB} = GND or O _{EA} = GND, O _{EB} = V _{cc} Eight Bits Toggling	V _{IN} = V _{cc} V _{IN} = GND				
			V _{IN} = 3.4V V _{IN} = GND		5.2	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

6. I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_c = I_{cc} + ΔI_{cc} D_HN_T + I_{ccd} (f_{CP}/2 + f_iN_i)

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT240/2240T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	240T/2240T		240AT/2240AT		240CT/2240CT		240DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	1.5	3.6	ns
t _{PHL}	DN to ON										
t _{PZH}	Output Enable Time		1.5	10.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
t _{PZL}	OE _X to ON										
t _{PHZ}	Output Disable Time(3)		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.0	ns
t _{PLZ}	OE _X to ON										

2

PI74FCT241/2241T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	241T/2241T		241AT/2241AT		241CT/2241CT		241DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.6	ns
t _{PHL}	DN to ON										
t _{PZH}	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
t _{PZL}	OE _A /OE _B to ON										
t _{PHZ}	Output Disable Time ⁽³⁾		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	ns
t _{PLZ}	OE _A /OE _B to ON										

PI74FCT244/2244T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	244T/2244T		244AT/2244AT		244CT		244DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.6	ns
t _{PHL}	DN to ON										
t _{PZH}	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
t _{PZL}	OE _X to ON										
t _{PHZ}	Output Disable Time ⁽³⁾		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	ns
t _{PLZ}	OE _X to ON										

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT540T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	540T		540AT		540CT		540DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	5.5	1.5	4.8	1.5	4.3	1.5	3.8	ns
tPHL	DN to ON										
tpZH	Output Enable Time		1.5	10.0	1.5	6.2	1.5	5.8	1.5	5.2	ns
tpZL	OEx to ON										
tpHZ	Output Disable Time ⁽³⁾		1.5	6.0	1.5	5.6	1.5	5.2	1.5	5.2	ns
tPLZ	OEx to ON										

PI74FCT541/2541T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	541T/2541T		541AT/2541AT		541CT/2541CT		541DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	4.8	1.5	4.1	1.5	3.8	ns
tPHL	DN to ON										
tpZH	Output Enable Time		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.2	ns
tpZL	OEx to ON										
tpHZ	Output Disable Time ⁽³⁾		1.5	6.5	1.5	5.6	1.5	5.2	1.5	5.2	ns
tPLZ	OEx to ON										

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

Parameters	Description	Conditions ⁽¹⁾	Com.									
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	4.8	1.5	4.1	1.5	3.8	1.5	3.6
tPHL	DN to ON											
tpZH	Output Enable Time		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.2	1.5	4.8
tpZL	OEx to ON											
tpHZ	Output Disable Time ⁽³⁾		1.5	6.5	1.5	5.6	1.5	5.2	1.5	5.2	1.5	4.0
tPLZ	OEx to ON											

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.



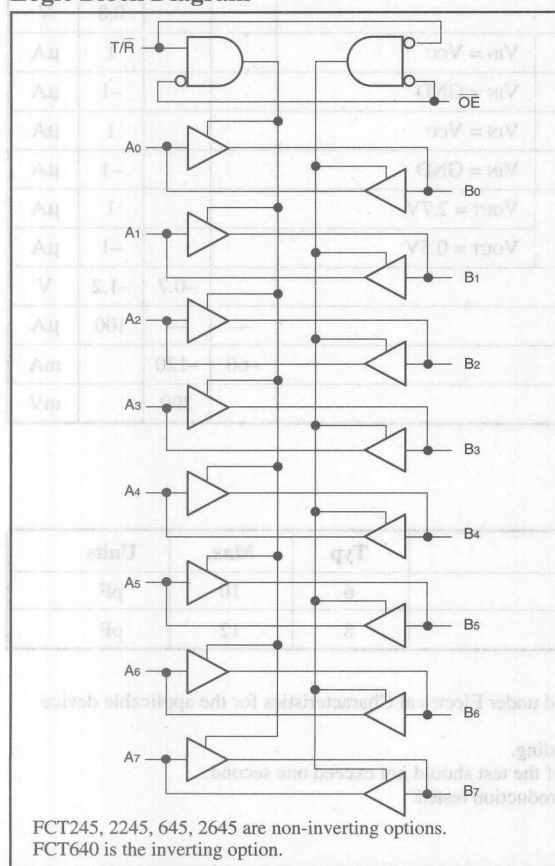
PI74FCT245T/640T/645T
(25Ω Series) PI74FCT2245T/2645T

Fast CMOS Octal Bidirectional Transceivers

Product Features:

- PI74FCT245/640/645T and PI74FCT2245/2645T are pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Logic Block Diagram

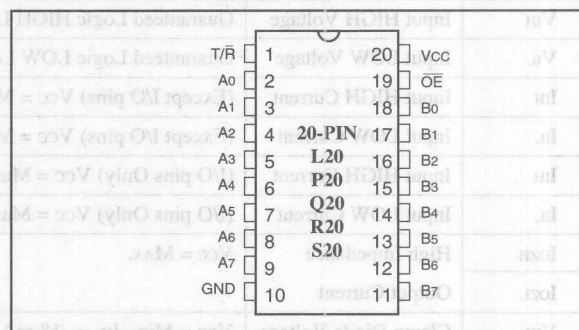


Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT245T/640T/645T and PI74FCT2245T/2645T are 8-bit wide octal buffer bidirectional transceivers designed for asynchronous two-way communication between data buses. The transmit/receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

Product Pin Configuration



Product Pin Description

Pin Name	Description
OE	3-State Output Enable Inputs (Active LOW)
T/R	Transmit/Receive Input
A0-A7	Side A Inputs or 3-State Outputs
B0-B7	Side B Inputs or 3-State Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A ⁽²⁾
L	H	Bus A Data to Bus B ⁽²⁾
H	X	High Z State

1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance
2. 640 is inverting from input to output.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA		0.3	0.55	V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA (25Ω Series)		0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	(Except I/O pins) V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	(Except I/O pins) V _{CC} = Max.	V _{IN} = GND			-1	μA
I _{IH}	Input HIGH Current	(I/O pins Only) V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	(I/O pins Only) V _{CC} = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current		V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V		—	—	100	μA
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-60	-120		mA
V _H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.,	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE = GND T/R = GND or V _{cc} One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle T/R = OE = GND One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		2.0	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.3	5.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle T/R = OE = GND Eight Bits Toggling	V _{IN} = V _{cc} V _{IN} = GND		3.5	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.5	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

6. $I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$

$I_c = I_{\text{cc}} + \Delta I_{\text{cc}} D_H N_t + I_{\text{CCD}} (f_{\text{CP}}/2 + f_i N_i)$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_t = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Parameters	Description	Conditions ⁽¹⁾	245T/2245T		245AT/2245AT		245CT/2245CT		245DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	ns
tpZH tpZL	Output Enable Time OE to A or B		1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tpHZ tPLZ	Output Disable Time OE to A or B ⁽³⁾		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns
tpZH tpZL	Output Enable Time T/R to A or B		1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ T/R to A or B ⁽³⁾		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns

PI74FCT640T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	640T		640AT		640CT		640DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	2.0	7.0	1.5	5.0	1.5	4.4	1.5	3.7	ns
tpZH tpZL	Output Enable Time OE to A or B		2.0	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tpHZ tPLZ	Output Disable Time OE to A or B ⁽³⁾		2.0	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns
tpZH tpZL	Output Enable Time T/R to A or B		2.0	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ T/R to A or B ⁽³⁾		2.0	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

PI74FCT645T/2645T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	645T/2645T		645AT/2645AT		645CT/2645CT		645DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHLL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	9.5	1.5	4.6	1.5	4.1	1.5	3.8	ns
tpZH tpZL	Output Enable Time OE to A or B		1.5	11.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tpHZ tPLZ	Output Disable Time OE to A or B ⁽³⁾		1.5	12.0	1.5	5.0	1.5	4.8	1.5	4.3	ns
tpZH tpZL	Output Enable Time T/R to A or B		1.5	11.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ T/R to A or B ⁽³⁾		1.5	12.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

Fast CMOS Octal D Flip-Flop with Master Reset

Product Features:

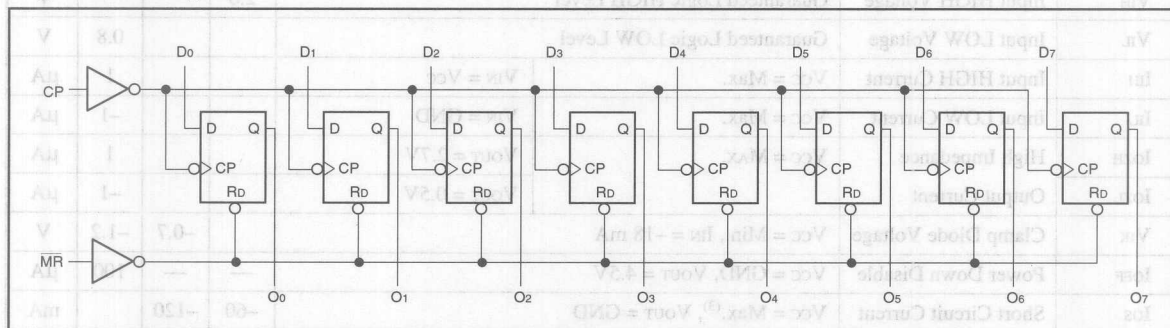
- PI74FCT273/2273T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

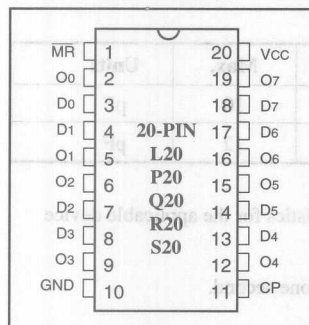
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT273T and PI74FCT2273T is an 8-bit wide octal designed with eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset (MR) load and resets (clear) all flip-flops simultaneously. The register is fully edge-triggered. The D input state, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
MR	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
D0-D7	Data Inputs
O0-O7	Data Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Mode	Inputs			Outputs
	MR	CP	D _N	O _N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

1. H = High Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = Low Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Don't Care
↑ = LOW-to-HIGH Clock Transition



PI74FCT273T
(25Ω Series) P174FCT2273T
OCTAL D FLIP-FLOP WITH MASTER RESET

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.3	0.55	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 12 mA (25Ω Series)		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IiH	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max. VOUT = 2.7V			1	μA
IOZL	Output Current	VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	μA
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open MR = V _{CC} , One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle MR = V _{CC} , 50% Duty Cycle One Bit toggling at f _I = 5 MHz	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle MR = V _{CC} , 50% Duty Cycle Eight Bits toggling at f _I = 2.5 MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.2	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	273T/2273T		273AT/2273AT		273CT/2273CT		273DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.0	13.0	2.0	7.2	2.0	5.8	2.0	4.4	ns
t _{PHL}	CP to ON										
t _{PHL}	Propagation Delay	MR to ON	2.0	13.0	2.0	7.2	2.0	6.1	2.0	5.0	ns
t _{PLH}	MR to ON										
t _{SU}	Setup Time, HIGH or LOW Dn to CP		3.0	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time, HIGH or LOW Dn to CP		2.0	—	1.5	—	1.5	—	1.5	—	ns
t _W	CP Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	6.0	—	6.0	—	3.0	—	ns
t _W	MR Pulse Width ⁽³⁾ LOW		7.0	—	6.0	—	6.0	—	3.0	—	ns
t _{REM}	Recovery Time MR to CP ⁽³⁾		4.0	—	2.0	—	2.0	—	2.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.



PI74FCT280T

Fast CMOS

9-Bit Parity Generator/Checker

2

Product Features:

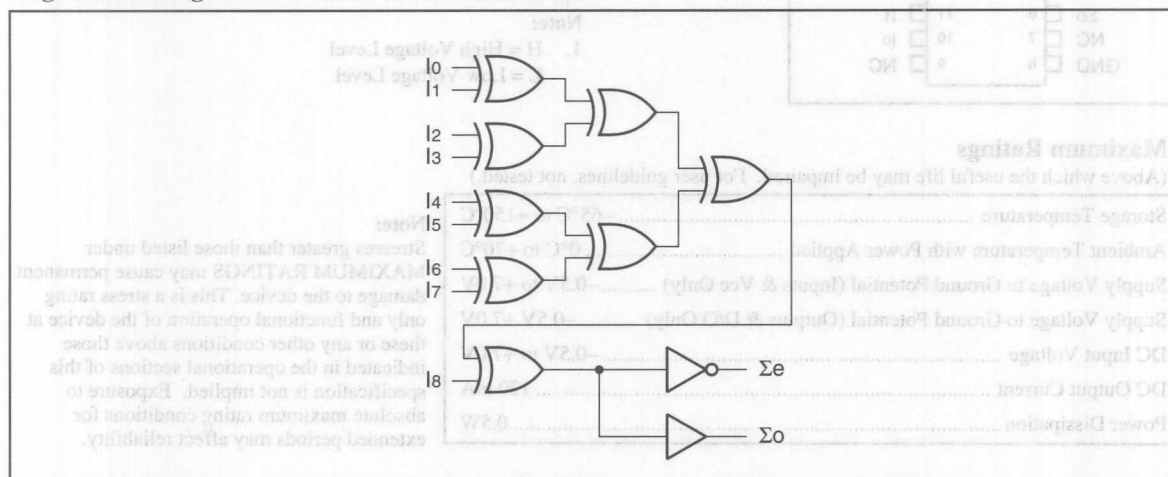
- PI74FCT280T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 14-pin 150 mil wide SOIC (W14)
 - 16-pin 150 mil wide QSOP (Q16)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT280T is a high-speed CMOS TTL-compatible 9-bit parity generator-checkers. Both odd and even parity outputs are available for generating or checking odd or even parity.

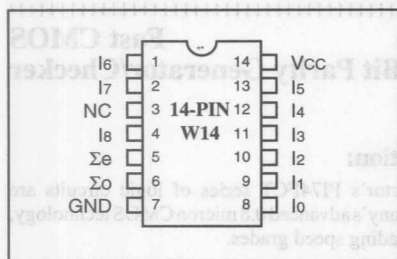
Logic Block Diagram



Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{in}	Input Capacitance	V _{in} = 0V	6	10	pF
C _{out}	Output Capacitance	V _{out} = 0V	8	12	pF

Notes:
1. This parameter is determined by device characterization but is not production tested.

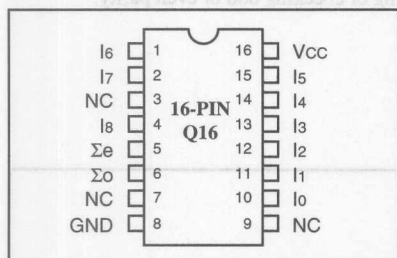
PI74FCT280T 14-Pin SOIC Configuration



Product Pin Description

Pin Name	Description
I8-I0	Data In
Σe	Even Parity Out
Σo	Odd Parity Out
GND	Ground
VCC	Power

PI74FCT280T 16-Pin QSOP Configuration



Truth Table⁽¹⁾

Function	Inputs	Outputs	
	I8-I0	Σe	Σo
Even Parity	No. of Bits at TTL High = 0, 2, 4, 6, 8	H	L
Odd Parity	No. of Bits at TTL High = 1, 3, 5, 7, 9	L	H

Note:

- H = High Voltage Level
L = Low Voltage Level

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

- This parameter is determined by device characterization but is not production tested.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -15.0 \text{ mA}$	2.4	3.0		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48 \text{ mA}$		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$	$V_{IN} = \text{GND}$			-1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18 \text{ mA}$			-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}$, $V_{OUT} = \text{GND}$		-60	-120		mA
I_{OFF}	Power Down Disable	$V_{CC} = \text{GND}$, $V_{OUT} = 4.5V$		—	—	100	μA
V_H	Input Hysteresis				200		mV

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	280T		280AT		280BT		280CT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
TPHLE TPLHE	Propagation Delay I0 – I8 to Σ_{Even}	CL = 50 pF RL = 500Ω	3.0	10.0	3.0	7.5	3.0	6.3	3.0	5.3	ns
TPHLO TPLHO	Propagation Delay I0 – I8 to Σ_{Odd}		3.0	10.0	3.0	7.5	3.0	6.3	3.0	5.3	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾			2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = EN = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND			0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = EN = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
			V _{IN} = V _{CC} V _{IN} = GND		4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.2	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Fast CMOS Octal Transparent Latches

Product Features:

- PI74FCT373/533/573/2373/2573T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

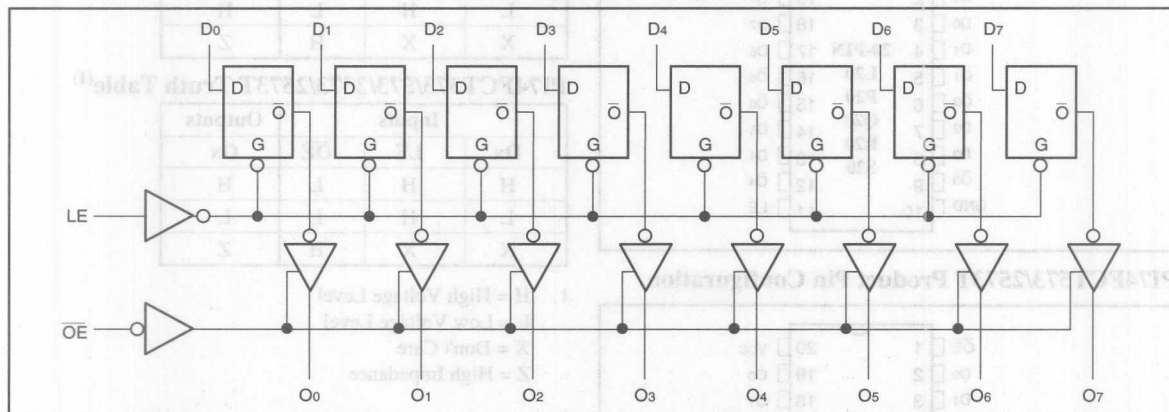
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

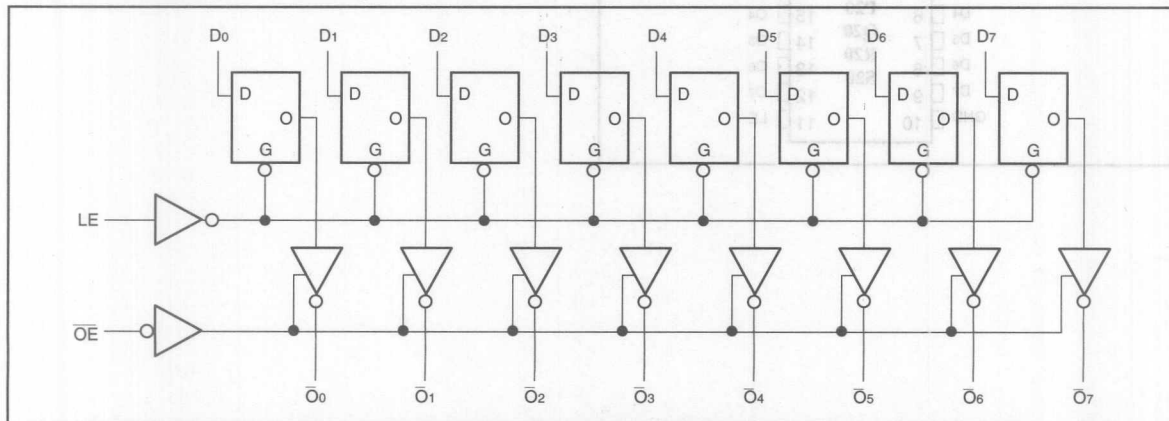
The PI74FCT373T/533T/573T and P174FCT2373T/2573T are 8-bit wide octal transparent latches designed with 3-state outputs and are intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When \overline{OE} is HIGH, the bus output is in the high impedance state.

2

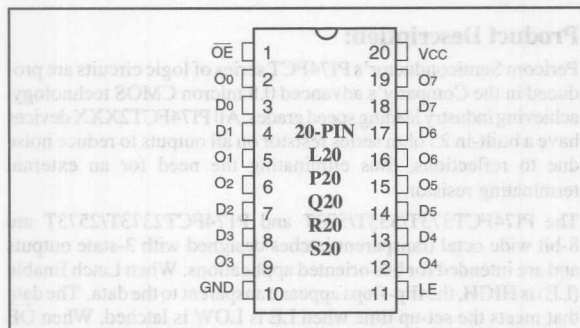
PI74FCT373/2373T and PI74FCT573/2573T Logic Block Diagram



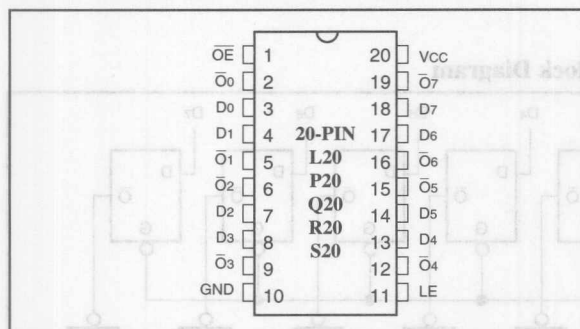
PI74FCT533T Logic Block Diagram



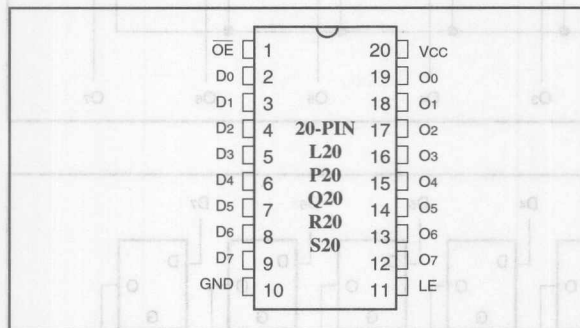
PI74FCT373/2373T Product Pin Configuration



PI74FCT533T Product Pin Configuration



PI74FCT573/2573T Product Pin Configuration



Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D0-D7	Data Inputs
O0-O7	3-State Outputs
Ö0-Ö7	Complementary 3-State Outputs
GND	Ground
Vcc	Power

PI74FCT533T Truth Table⁽¹⁾

Inputs			Outputs
D _N	LE	ÖE	Ö _N
H	H	L	L
L	H	L	H
X	X	H	Z

PI74FCT373/573/2373/2573T Truth Table⁽¹⁾

Inputs			Outputs
D _N	LE	ÖE	O _N
H	H	L	H
L	H	L	L
X	X	H	Z

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance



PI74FCT373T/533T/573T
(25Ω Series) P174FCT2373T/2573T
OCTAL TRANSPARENT LATCHES

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 64 mA		0.3	0.55	V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 12 mA (25Ω Series)		0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max. V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max. V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V	—	—	100	μA
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-60	-120		mA
V _H	Input Hysteresis			200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.,	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE = GND LE = V _{cc} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE = GND LE = V _{cc} One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
			V _{IN} = V _{cc} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.2	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccD} (f_{cp}/2 + f_i N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamperes and all frequencies are in megahertz.

PI74FCT373/2373T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	373T/2373T		373AT/2373AT		373CT/2373CT		373DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay DN to ON	C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
t _{PLH} t _{PHL}	Propagation Delay LE to ON		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.9	ns
t _{PZH} t _{PZL}	Output Enable Time OE to ON		1.5	12.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OE to ON		1.5	7.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
t _{SU}	Setup Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
t _w	LE Pulse Width ⁽³⁾ HIGH		6.0	—	5.0	—	5.0	—	4.0	—	ns

2

PI74FCT533T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	533T		533AT		533CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay DN to ON	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	8.5	2.0	5.5	ns
tPZH tPZL	Output Enable Time OE to ON		1.5	11.0	1.5	6.5	1.5	5.5	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OE to ON		1.5	7.0	1.5	5.5	1.5	5.0	ns
tSU	Setup Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	ns
tW	LE Pulse Width ⁽³⁾ HIGH		6.0	—	5.0	—	5.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.

PI74FCT573/2573T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	573T/2573T		573AT/2573AT		573CT		573DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay DN to ON	C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
t _{PLH} t _{PHL}	Propagation Delay LE to ON		2.0	12.0	2.0	8.5	2.0	5.5	2.0	4.9	ns
t _{PZH} t _{PZL}	Output Enable Time OE to ON		1.5	9.5	1.5	6.5	1.5	5.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OE to ON		1.5	6.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
t _{SU}	Setup Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	1.5	—	ns
t _H	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.0	—	ns
t _W	LE Pulse Width ⁽³⁾ HIGH		6.0	—	5.0	—	5.0	—	3.0	—	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter guaranteed but not production tested.

Parameters	Description	Conditions ⁽¹⁾	Com.		Com.		Com.		Com.		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
t _{PHL}	DN to ON										
t _{PLH}	Propagation Delay		2.0	12.0	2.0	8.5	2.0	5.5	2.0	4.9	ns
t _{PHL}	LE to ON										
t _{PZH}	Output Enable Time		1.5	11.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
t _{PZL}	OE to ON										
t _{PHZ}	Output Disable Time ⁽³⁾		1.5	7.0	1.5	5.5	1.5	5.0	1.5	5.0	ns
t _{PLZ}	OE to ON										
t _{SU}	Setup Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	1.5	—	ns
t _H	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.0	—	ns
t _W	LE Pulse Width ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	ns
	HIGH										

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter guaranteed but not production tested.

Fast CMOS Octal D Registers (3-State)

Product Features:

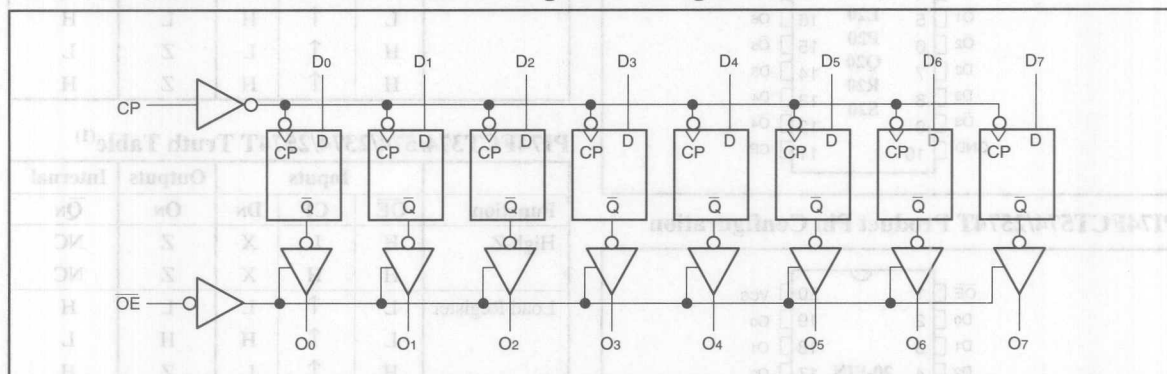
- PI74FCT374/534/574/2374/2574T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

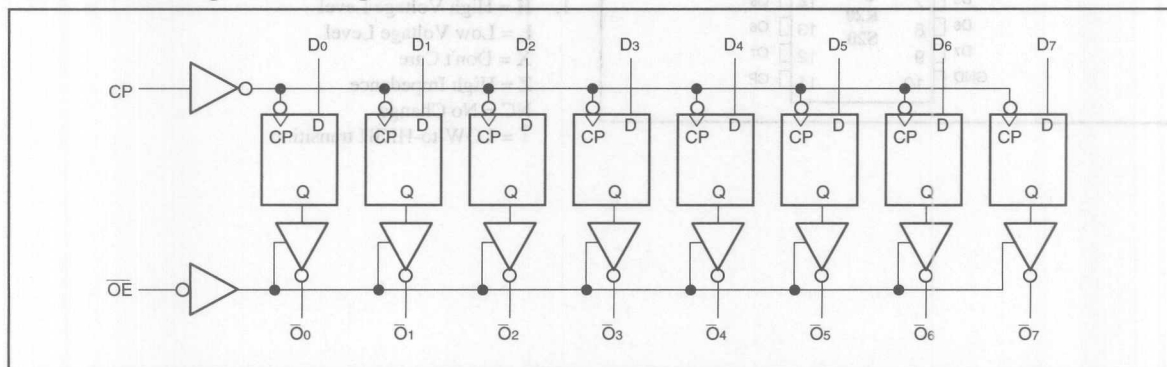
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT374T/534T/574T and PI74FCT2374T/2574T are 8-bit wide octal registers designed with eight D-type flip-flops with a buffered common clock and buffered 3-state outputs. When output enable (\overline{OE}) is LOW, the outputs are enabled. When \overline{OE} is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

PI74FCT374/2374T and PI74FCT574/2574T Logic Block Diagram



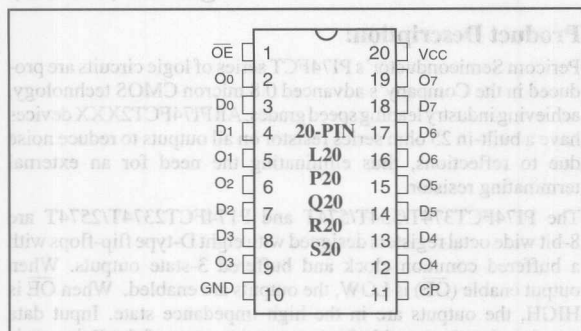
PI74FCT534T Logic Block Diagram



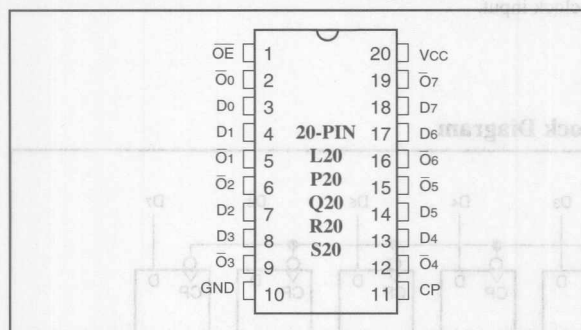


PI74FCT374T/534T/574T (25Ω Series) PI74FCT2374T/2574T OCTAL D REGISTERS (3-STATE)

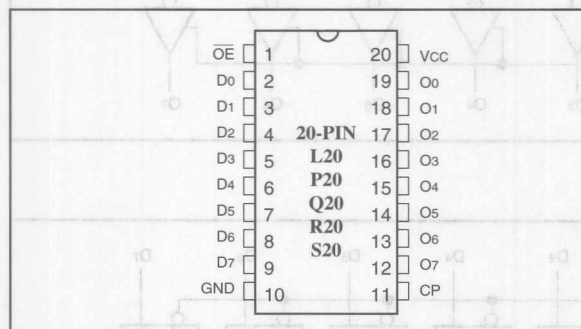
PI74FCT374/2374T Product Pin Configuration



PI74FCT534T Product Pin Configuration



PI74FCT574/2574T Product Pin Configuration



Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
D0-D7	Data Inputs
O0-O7	3-State Outputs (true)
Ö0-Ö7	3-State Outputs (inverted)
GND	Ground
Vcc	Power

PI74FCT534T Truth Table⁽¹⁾

	Inputs			Outputs	Internal
Function	OE	CP	Dn	ÖN	QN
High-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	H	L
	L	↑	H	L	H
	H	↑	L	Z	L
	H	↑	H	Z	H

PI74FCT374/574/2374/2574T Truth Table⁽¹⁾

	Inputs			Outputs	Internal
Function	OE	CP	Dn	ÖN	QN
High-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.3	0.55	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 12 mA (25Ω Series)		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IIH	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max. VOUT = 2.7V			1	μA
IOZL	Output Current	VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	μA
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND fi = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		4.0	7.8 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		6.2	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_{CP}/2 + fiN_I)

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

fi = Input Frequency

N_I = Number of Inputs at fi

All currents are in milliamperes and all frequencies are in megahertz.



PI74FCT374/2374T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	374T/2374T		374AT/2374AT		374CT/2374CT		374DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay CP to ON	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	2.0	4.5	ns
t _{PZH} t _{PZL}	Output Enable Time OE to ON		1.5	12.5	1.5	6.5	1.5	5.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OE to ON		1.5	8.0	1.5	5.5	1.5	5.0	1.5	5.0	ns
t _{SU}	Setup Time HIGH or LOW, D _N to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time HIGH or LOW, D _N to CP		1.5	—	1.5	—	1.5	—	1.0	—	ns
t _W	CP Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.0	—	5.0	—	3.0	—	ns

PI74FCT534T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	534T		534AT		534CT		534DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay CP to ON	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	2.0	4.5	ns
t _{PZH} t _{PZL}	Output Enable Time OE to ON		1.5	12.5	1.5	6.5	1.5	5.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OE to ON		1.5	8.0	1.5	5.5	1.5	5.0	1.5	5.0	ns
t _{SU}	Setup Time HIGH or LOW, D _N to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time HIGH or LOW, D _N to CP		1.5	—	1.5	—	1.5	—	1.0	—	ns
t _W	CP Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.0	—	5.0	—	3.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT574/2574T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	574T/2574T		574AT/2574AT		574CT/2574CT		574DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.0	8.5	2.0	6.5	2.0	5.2	2.0	4.5	ns
t _{PHL}	CP to \bar{O} N										
t _{PZH}	Output Enable Time		1.5	10.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
t _{PZL}	OE to ON										
t _{PHZ}	Output Disable Time ⁽³⁾		1.5	6.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
t _{PLZ}	OE to ON										
t _{SU}	Setup Time HIGH or LOW, D _N to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time HIGH or LOW, D _N to CP		1.5	—	1.5	—	1.5	—	1.0	—	ns
t _W	CP Pulse Width ⁽³⁾		7.0	—	5.0	—	5.0	—	3.0	—	ns
	HIGH or LOW										

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.

Parameters	Description	Conditions ⁽¹⁾	Min	Max	Unit
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.0	10.0	ns
t _{PHL}	CP to \bar{O} N				
t _{PZH}	Output Enable Time		1.5	12.5	ns
t _{PZL}	OE to ON				
t _{PHZ}	Output Disable Time ⁽³⁾		1.5	8.0	ns
t _{PLZ}	OE to ON				
t _{SU}	Setup Time HIGH or LOW, DN to CP		2.0	—	ns
t _H	Hold Time HIGH or LOW, DN to CP		1.5	—	ns
t _W	CP Pulse Width ⁽³⁾		7.0	—	ns
	HIGH or LOW				

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.



PI74FCT377T

Fast CMOS Octal D Flip-Flop with Clock Enable

Product Features:

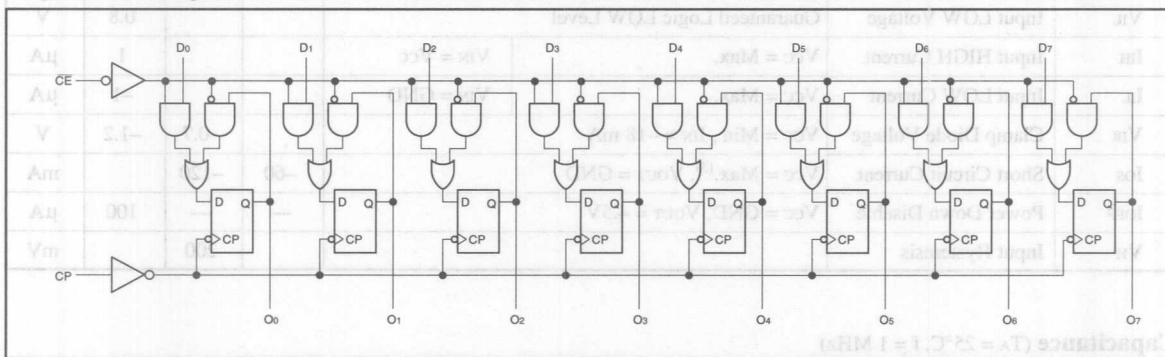
- The PI74FCT377T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Octal D flip-flops with Clock Enable
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

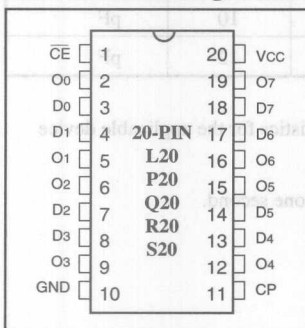
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.3 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT377T is an 8-bit wide octal designed with eight edge-triggered D-type flip-flops with individual D inputs and O outputs. When Clock Enable (CE) is LOW, the common buffered Clock (CP) loads all flip-flops simultaneously. The register is fully edge-triggered. The D input state, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The CE input must be stable only one setup time prior to the LOW-to-HIGH transition for predictable operation.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
CE	Clock Enable (Active LOW)
CP	Clock Pulse Input
D0-D7	Data Inputs
O0-O7	Data Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Mode	Inputs			Outputs
	CP	CE	DN	ON
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold	↑	h	X	NC
(Do Nothing)	H	H	X	NC

1. H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Clock Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 64 mA		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IIH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA			-0.7	-1.2	V
IOS	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120		mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
VH	Input Hysteresis				200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open CE = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle CE = GND 50% Duty Cycle One Bit toggling at f _i = 5 MHz	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle CE = GND Eight Bits toggling at f _i = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.2	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_{HNT} + I_{ccd} (f_{CP}/2 + f_i N_i)$
I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	377T		377AT		377CT		377DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.0	13.0	2.0	7.2	2.0	5.2	2.0	4.5	ns
t _{PHL}	CP to ON										
t _{su}	Setup Time, HIGH or LOW Dn to CP		2.5	—	2.0	—	2.0	—	2.0	—	ns
t _H	Hold Time, HIGH or LOW Dn to CP		2.0	—	1.5	—	1.5	—	1.5	—	ns
t _{su}	Setup Time HIGH or LOW CE to CP		4.0	—	3.5	—	3.5	—	2.0	—	ns
t _H	Hold Time HIGH or LOW CE to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t _w	Clock Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	6.0	—	6.0	—	3.0	—	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter guaranteed but not production tested.

Fast CMOS Quad Dual-Port Register

Product Features:

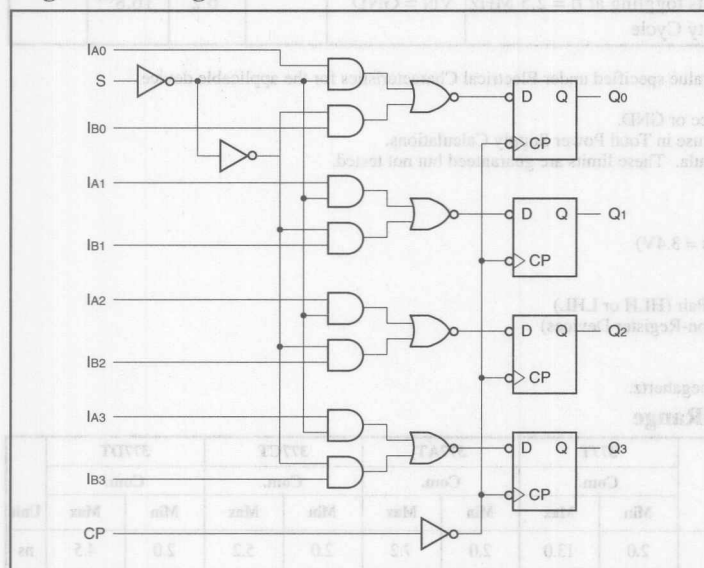
- PI74FCT399T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Packages available:
 - 16-pin 300 mil wide plastic DIP (P16)
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

These high-speed quad dual-port registers select 4-bit wide data from one of the two sources (Ports) under control of a common Select input (S). Synchronous with the LOW-to-HIGH transition of the Clock input (CP), the selected data is transferred to a 4-bit output register. The 4-bit D-type output register is fully edge-triggered. For predictable operation, the Data inputs (IAx, IBx) and Select input (S) must be stable one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input.

Logic Block Diagram



Product Pin Description

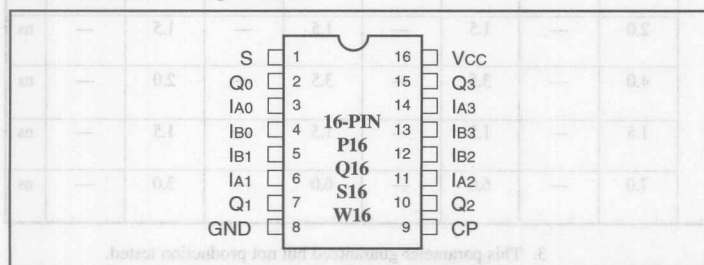
Pin Name	Description
S	Common Select Input
CP	Clock Pulse Input
IA0-IA3	Data Inputs from Source A
IB0-IB3	Data Inputs from Source B
Q0-Q3	Register True Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs			Outputs
S	IA	IB	Q
I	I	X	L
I	h	X	H
h	X	I	L
h	X	h	H

1. H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Don't Care

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2
DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 48 mA		0.3	0.50	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max. V _{IN} = GND			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA	-0.7	-1.2		V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-60	-120		mA
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V	—	—	100	μA
V _H	Input Hysteresis			200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open S = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle S = GND 50% Duty Cycle One Bit toggling at f _i = 5 MHz	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle S = GND Eight Bits toggling at f _i = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.2	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_t + I_{ccd} (f_{CP}/2 + f_i N_i)$
I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_t = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	399T		399AT		399CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	3.0	10.0	2.5	7.0	2.5	5.6	ns
t _{PHL}	CP to Q								
t _{SU}	Setup Time, HIGH or LOW D to Q		4.0	—	3.5	—	3.0	—	ns
t _H	Hold Time, HIGH or LOW D to Q		1.0	—	1.0	—	1.0	—	ns
t _{SU}	Setup Time HIGH or LOW S to CP		9.0	—	8.5	—	3.0	—	ns
t _H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	ns
t _w	Clock Pulse Width ⁽³⁾ HIGH or LOW		5.0	—	5.0	—	4.0	—	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.



PI74FCT521T

Fast CMOS 8-Bit Identity Comparator

2

Product Features:

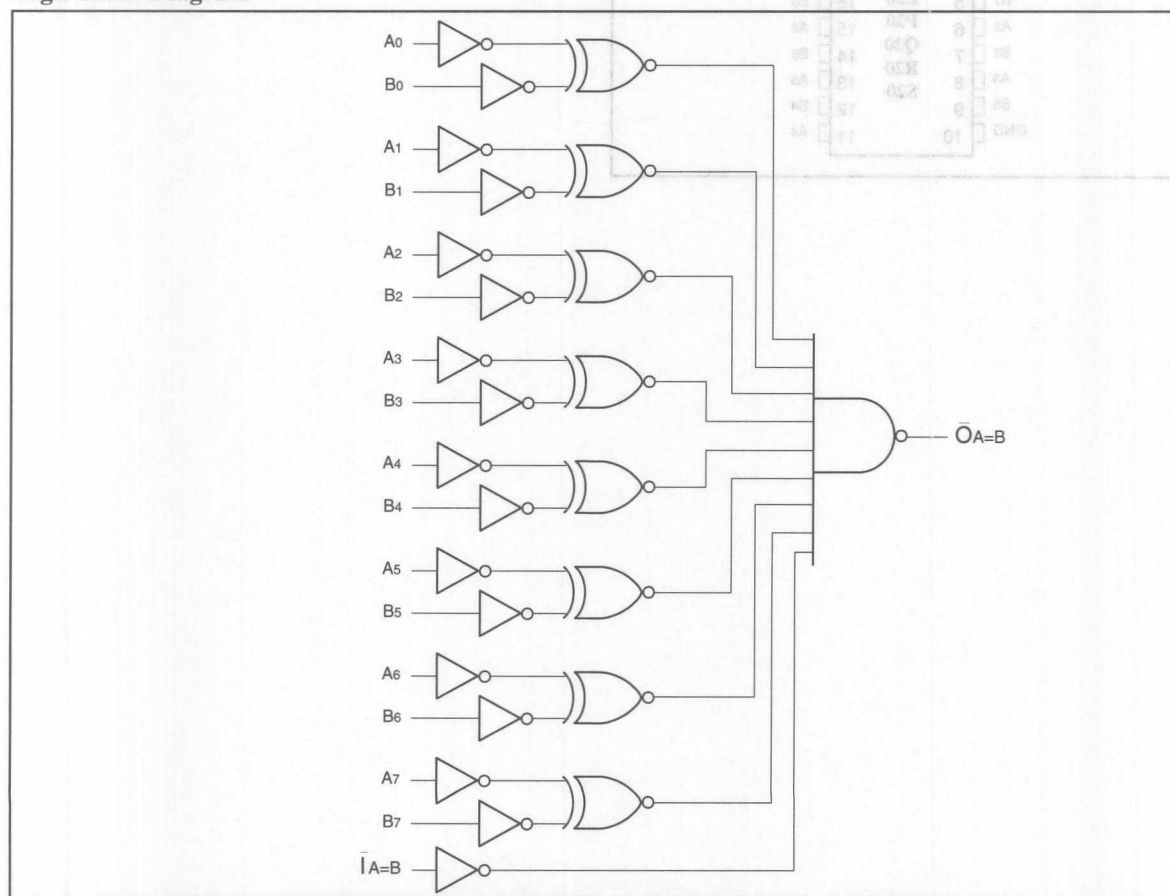
- PI74FCT521T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT521T is an 8-bit identity comparator. When two words of up to eight bits are compared, a bit-for-bit match of the two words provides a LOW output. The comparison can be extended over multiple words by the expansion input. The expansion input $\bar{A}=B$ also serves as an active LOW enable input.

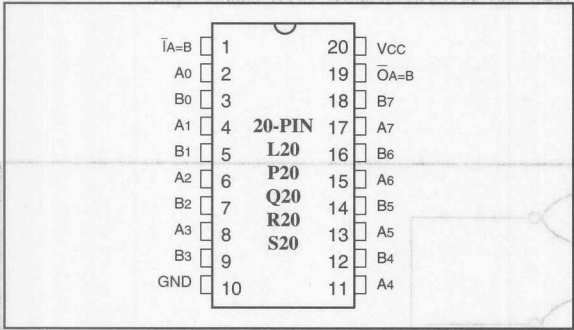
Logic Block Diagram



Product Pin Description

Pin Name	Description
$\bar{I}A=B$	Expansion or Enable Input (Active LOW)
$\bar{O}A=B$	Identity Output (Active LOW)
A0–A7	Word A Inputs
B0–B7	Word B Inputs
GND	Ground
Vcc	Power

Product Pin Configuration



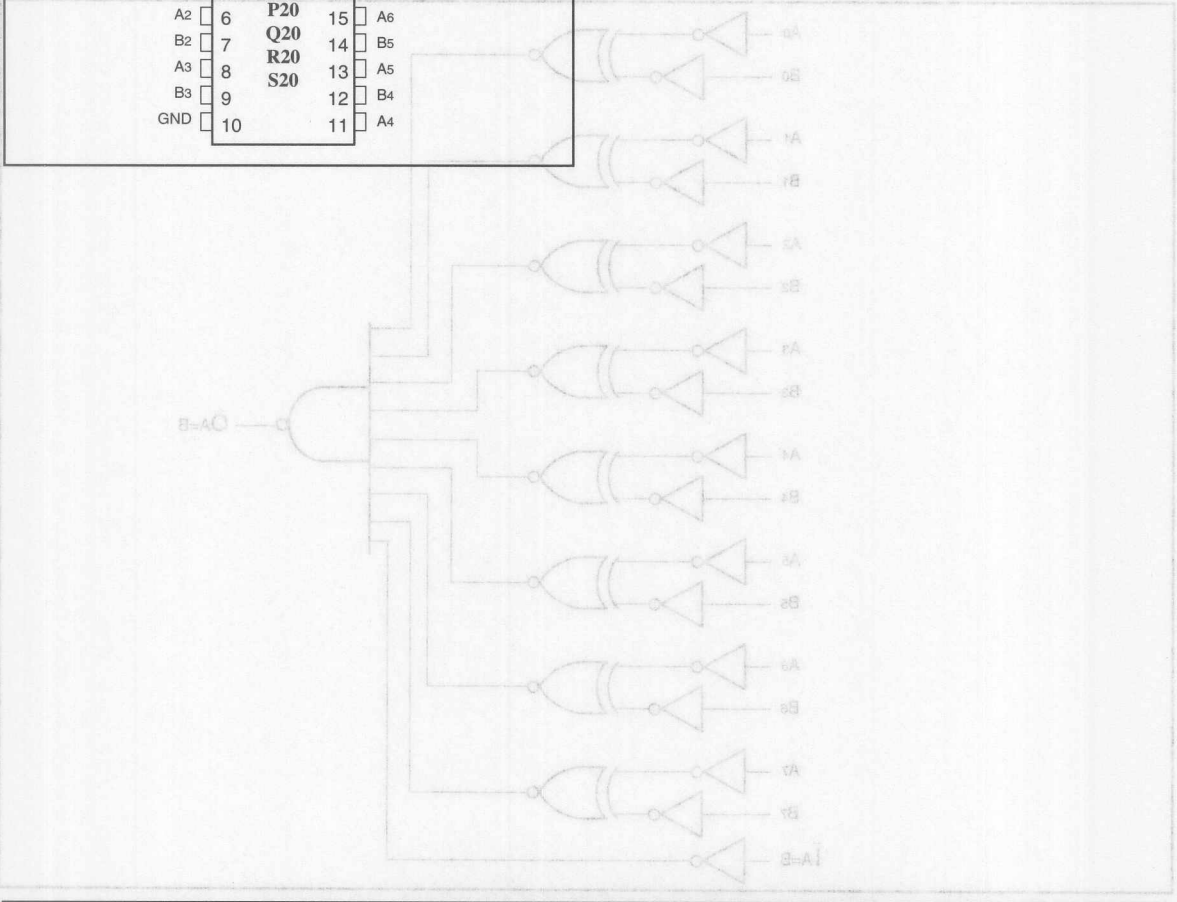
Truth Table⁽¹⁾

Inputs		Output
$\bar{I}A=B$	A, B	$\bar{O}A=B$
L	$A = B^*$	L
L	$A \neq B$	H
H	$A = B^*$	H
H	$A \neq B$	H

NOTE: 1. H = High Voltage Level

L = Low Voltage Level,

*A0 = B0, A1 = B1, A2 = B2, etc.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 48 mA		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IiH	Input HIGH Current	VCC = Max. VIN = VCC			1	µA
IiL	Input LOW Current	VCC = Max. VIN = GND			-1	µA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	-0.7	-1.2		V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
Ioff	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	µA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND V _{IN} = 3.4V V _{IN} = GND		1.7 2.0	4.0 ⁽⁵⁾ 5.0 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	521T		521AT		521BT		521CT		521DT		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay AN or BN to OA=B	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.2	1.5	5.5	1.5	4.5	1.5	4.2	ns
t _{PLH} t _{PHL}	Propagation Delay IA=B to OA=B		1.5	9.0	1.5	6.0	1.5	4.6	1.5	4.1	1.5	3.8	ns

Notes:

- See Test Circuit and Waveforms
- Minimum limits are guaranteed but not tested on Propagation Delays.



PI74FCT543T/544T
(25Ω Series) PI74FCT2543T

Fast CMOS Latched Transceivers

2

Product Features:

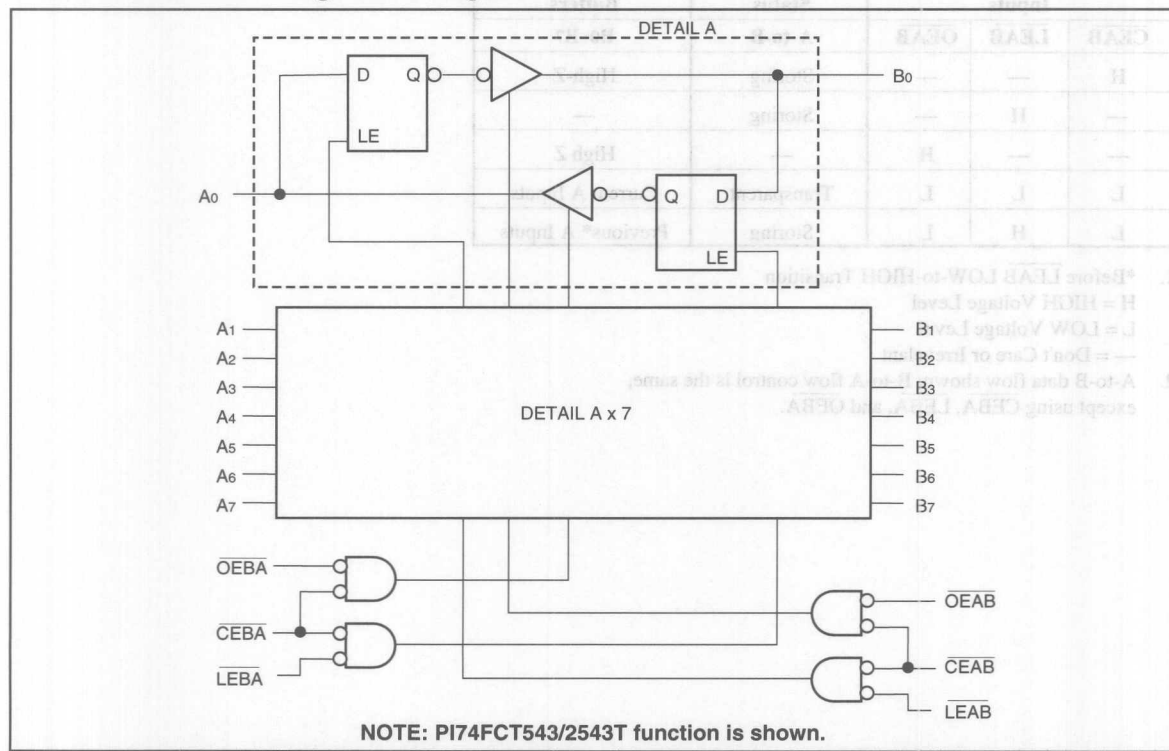
- PI74FCT543T/544/2543T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

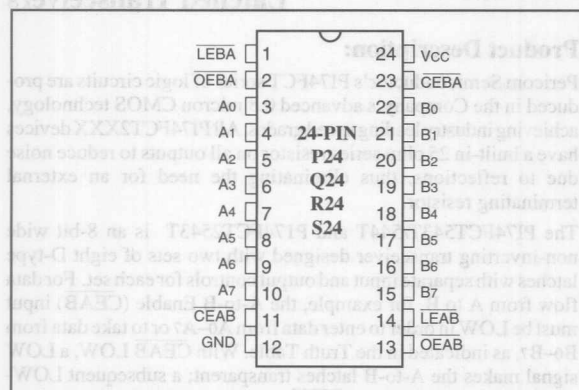
The PI74FCT543T/544T and PI74FCT2543T is an 8-bit wide non-inverting transceiver designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (CEAB) input must be LOW in order to enter data from A0-A7 or to take data from B0-B7, as indicated in the Truth Table. With CEAB LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With CEAB and OEAB both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the CEAB, LEAB, and OEAB inputs. The PI74FCT543T is a non-inverting of the PI74FCT544T.

PI74FCT543/544/2543T Logic Block Diagram



PI74FCT543/544/2543T Product Pin Configuration

Product Pin Description

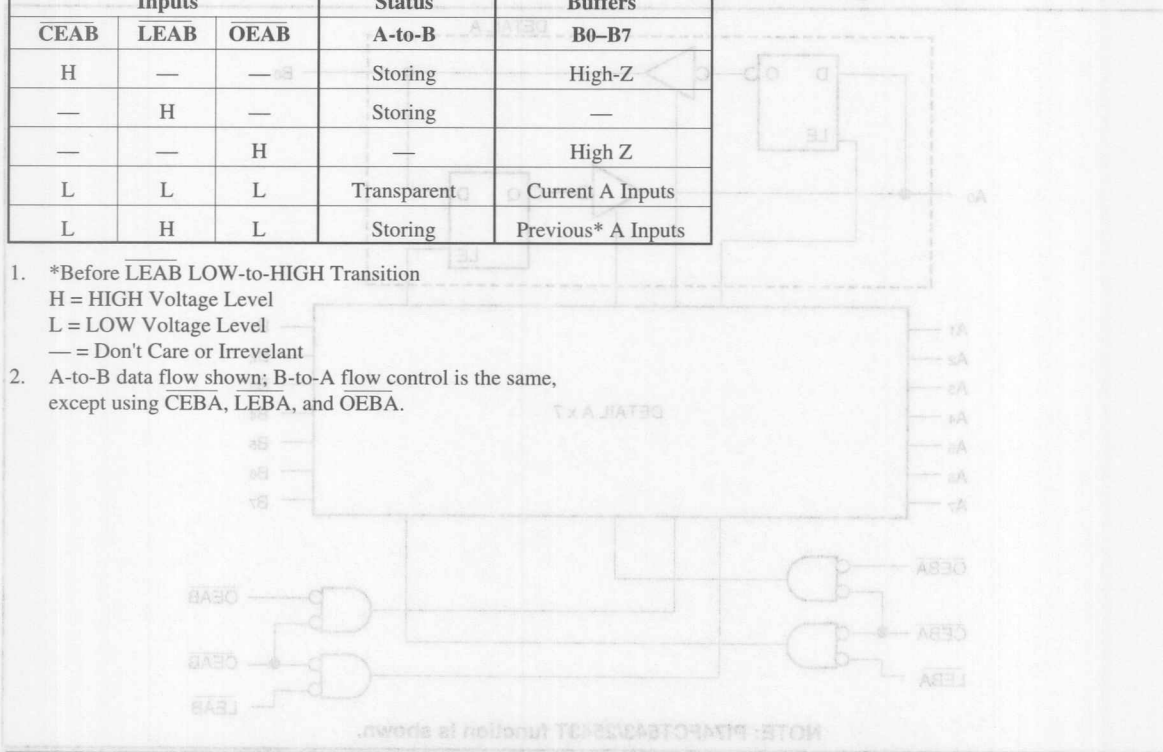


Pin Name	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CEAB	A-to-B Enable Input (Active LOW)
CEBA	B-to-A Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input (Active LOW)
LEBA	B-to-A Latch Enable Input (Active LOW)
A0-A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0-B7	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
Vcc	Power

PI74FCT543/2543T Truth Table (Non-Inverting)^(1,2)
For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
CEAB	LEAB	OEAB	A-to-B	B0-B7
H	—	—	Storing	High-Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

- *Before LEAB LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
— = Don't Care or Irrelevant
- A-to-B data flow shown; B-to-A flow control is the same, except using CEBA, LEBA, and OEBA.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.3	0.55	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 12 mA (25Ω Series)		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IIH	Input HIGH Current	(Except I/O pins) VCC = Max. VIN = VCC			1	μA
IIL	Input LOW Current	(Except I/O pins) VCC = Max. VIN = GND			-1	μA
IIH	Input HIGH Current	(I/O pins Only) VCC = Max. VIN = VCC			1	μA
IIL	Input LOW Current	(I/O pins Only) VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = MAX. VOUT = 2.7V			1	μA
IOZL	Output Current	VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	μA
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open CEAB and OEAB = GND CEBA = V _{cc} One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz (LEAB) 50% Duty Cycle CEAB and OEAB = GND CEBA = V _{cc} f _i = 5 MHz One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND V _{IN} = 3.4V V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz (LEAB) 50% Duty Cycle CEAB and OEAB = GND CEBA = V _{cc} Eight Bits Toggling f _i = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND V _{IN} = 3.4V V _{IN} = GND		7.0	12.8 ⁽⁵⁾	mA
					9.2	21.8 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

6. $I_c = I_{cc} + \Delta I_{cc} \cdot D_{HNT} + I_{ccd} (f_{CP}/2 + f_i N_i)$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT543/2543T (non-inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	543T/2543T		543AT/2543AT		543CT/2543CT		543DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay Transparent	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	ns
tPHL	Mode AN to BN or BN to AN		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	ns
tPLH	Propagation Delay		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	ns
tPHL	LEBA to AN, LEAB to BN		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	ns
tPZH	Output Enable Time		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	ns
tPZL	OEBA or OEAB to AN or BN CEBA or CEAB to AN or BN		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	ns
tPZH	Output Disable Time ⁽³⁾		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	ns
tPZL	OEBA or OEAB to AN or BN CEBA or CEAB to AN or BN	2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	ns	
tsu	Setup Time, HIGH or LOW AN or BN to LEBA or LEAB	3.0	—	2.0	—	2.0	—	1.5	—	ns	
th	Hold Time, HIGH or LOW AN or BN to LEBA or LEAB	2.0	—	2.0	—	2.0	—	1.5	—	ns	
tw	LEBA or LEAB Pulse Width LOW ⁽³⁾	5.0	—	5.0	—	5.0	—	3.0	—	ns	

2

PI74FCT544T (inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	544T		544AT		544CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Transparent Mode AN to BN or BN to AN	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	ns
tPLH tPHL	Propagation Delay LEBA to AN, LEAB to BN		2.5	12.5	2.5	8.0	2.5	7.0	ns
tPZH tPZL	Output Enable Time OEBA or OEAB to AN or BN CEBA or CEAB to AN or BN		2.0	12.0	2.0	9.0	2.0	8.0	ns
tPZH tPZL	Output Disable Time ⁽³⁾ OEBA or OEAB to AN or BN CEBA or CEAB to AN or BN		2.0	9.0	2.0	7.5	2.0	6.5	ns
tSU	Setup Time, HIGH or LOW AN or BN to LEBA or LEAB		3.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW AN or BN to LEBA or LEAB		2.0	—	2.0	—	2.0	—	ns
tW	LEBA or LEAB Pulse Width LOW ⁽³⁾		5.0	—	5.0	—	5.0	—	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.



PI74FCT623T

Fast CMOS Octal Bus Transceiver (3-State)

Product Features:

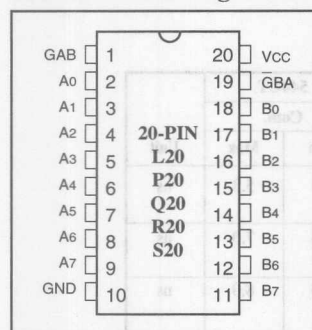
- PI74FCT623T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT623T is an 8-bit wide non-inverting octal transceiver designed with 3-state bus-driving outputs in both the send and receive directions. Designed for asynchronous two-way operation between data buses, the control function allows for maximum flexibility in timing.

Product Pin Configuration



Product Pin Description

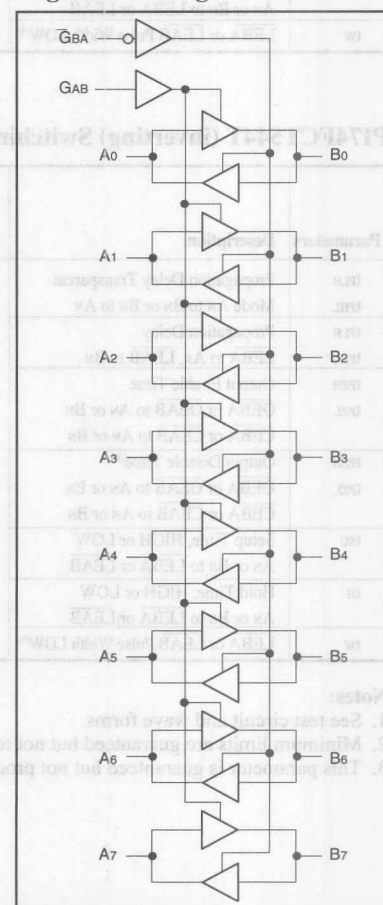
Pin Name	Description
GBA, GAB	Enable Outputs
A0-A7	A Bus Inputs or 3-State Outputs
B0-B7	B Bus Inputs or 3-State Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs		Outputs
GBA	GAB	
L	L	B Data to A Bus
H	H	A Data to B Bus
H	L	Z
L	H	B Data to A Bus A Data to B Bus

1. H = High Voltage Level
L = Low Voltage Level
Z = High Impedance (OFF) State

Logic Block Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 64 mA		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IiH	Input HIGH Current	VCC = Max.	VIN = VCC		1		μA
IiL	Input LOW Current	VCC = Max.	VIN = GND		-1		μA
IOZH	High Impedance	VCC = Max.	VOUT = 2.7V		1		μA
IOZL	Output Current		VOUT = 0.5V		-1		μA
VIK	Clamp Diode Voltage	VCC = Min., Iin = -18 mA		-0.7	-1.2		V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120		mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
VH	Input Hysteresis				200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.,	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open G _{BA} = GAB = GND, One Input Toggling, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
		G _{BA} = GAB = GND, 50% Duty Cycle One Bit toggling at f _i = 5 MHz	V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	
		G _{BA} = GAB = GND, 50% Duty Cycle Eight Bits toggling at f _i = 2.5 MHz 50% Duty Cycle	V _{IN} = 3.4V V _{IN} = GND		5.2	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_{CP}/2 + f_iN_i)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	623T		623AT		623CT		623DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay A _N to B _N	C _L = 50 pF R _L = 500Ω	1.5	7.5	1.5	5.5	1.5	4.8	1.5	3.8	ns
t _{PHL}	Propagation Delay B _N to A _N		1.5	7.5	1.5	5.5	1.5	4.8	1.5	3.8	ns
t _{PZH}	Output Enable Time G _{BA} to A _N		1.5	9.0	1.5	7.0	1.5	6.1	1.5	5.0	ns
t _{PZL}	Output Disable Time ⁽³⁾ G _{BA} to A _N		1.5	8.0	1.5	6.5	1.5	5.6	1.5	4.3	ns
t _{PZH}	Output Enable Time G _{AB} to B _N		1.5	9.0	1.5	7.0	1.5	6.1	1.5	5.0	ns
t _{PZL}	Output Disable Time ⁽³⁾ G _{AB} to B _N		1.5	8.0	1.5	6.5	1.5	5.6	1.5	4.3	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.



PI74FCT646T/648T/651T/652T
(25Ω Series PI74FCT2646T/2652T)

Fast CMOS Octal Registered Transceivers

Product Features:

- PI74FCT646T/648T/651T/652T/2646T/2652T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

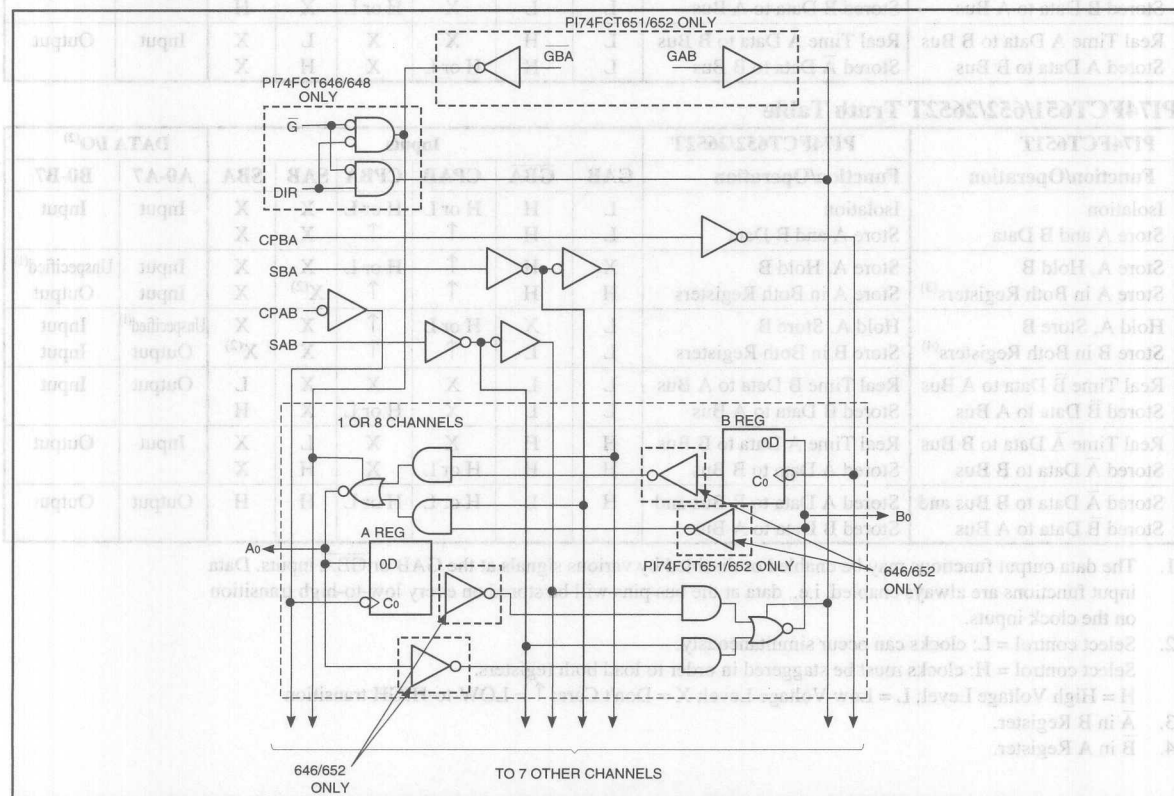
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT646T/648T/651T/652T and PI74FCT2646T/2652T are designed with a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The PI74FCT651/652T/2652T utilize GAB and GBA signals to control the transceiver functions. The PI74FCT646/2646T/648T utilize the enable control (\bar{G}) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74FCT646T is a non-inverting option of the PI74FCT648T. The PI74FCT652T is a non-inverting option of the PI74FCT651T.

Logic Block Diagram

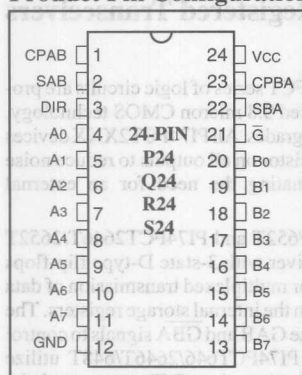




PI74FCT646/648/651/652T
(25Ω Series) PI74FCT2646T/2652T
OCTAL REGISTERED TRANSCEIVERS

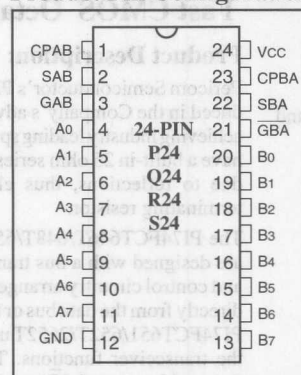
PI74FCT646/648T

Product Pin Configuration



PI74FCT651/652T

Product Pin Configuration



Product Pin Description

Pin Name	Description
A0-A7	Data Register A Inputs
B0-B7	Data Register B Outputs
B0-B7	Data Register B Inputs
B0-B7	Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, G-bar	Output Enable Inputs (646/648/2646)
GAB, GBA	Output Enable Inputs (651/652/2652)
GND	Ground
Vcc	Power

PI74FCT646/648/2646T Truth Table

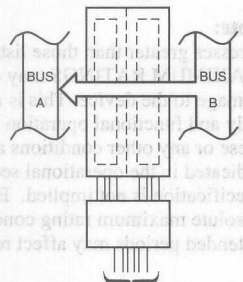
PI74FCT646/2646T	PI74FCT648T	Inputs						DATA I/O ⁽²⁾	
Function/Operation	Function/Operation	G-bar	DIR	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7
Isolation	Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	Real Time B-bar Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	Stored B-bar Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	Real Time A-bar Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	Stored A-bar Data to B Bus	L	H	H or L	X	H	X		

PI74FCT651/652/2652T Truth Table

PI74FCT651T	PI74FCT652/2652T	Inputs						DATA I/O ⁽²⁾	
Function/Operation	Function/Operation	GAB	GBA	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7
Isolation	Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾
Store A in Both Registers ⁽³⁾	Store A in Both Registers	H	H	↑	↑	X ⁽²⁾	X	Input	Output
Hold A, Store B	Hold A, Store B	L	X	H or L	↑	X	X	Unspecified ⁽¹⁾	Input
Store B in Both Registers ⁽⁴⁾	Store B in Both Registers	L	L	↑	↑	X	X ⁽²⁾	Output	Input
Real Time B Data to A Bus	Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and	Stored A Data to B Bus and	H	L	H or L	H or L	H	H	Output	Output
Stored B Data to A Bus	Stored B Data to A Bus								

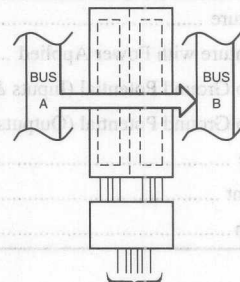
- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
 Select control = H: clocks must be staggered in order to load both registers.
 H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition
- A-bar in B Register.
- B-bar in A Register.

**REAL-TIME TRANSFER
BUS B TO A**



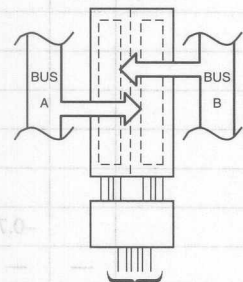
646/648/ 2646	DIR	\bar{G}	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
651/652/ 2652	GAB	GBA	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

**REAL-TIME TRANSFER
BUS A TO B**



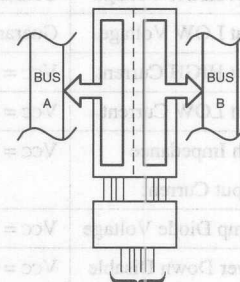
646/648/ 2646	DIR	\bar{G}	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X
651/652/ 2652	GAB	GBA	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X

**STORAGE FROM
A AND/OR B**



646/648/ 2646	DIR	\bar{G}	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
651/652/ 2652	GAB	GBA	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

**TRANSFER STORES
DATA TO A AND/OR B**



646/648 ⁽¹⁾ / 2646	DIR	\bar{G}	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
651/652/ 2652	GAB	GBA	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H

1. Note: The FCT646/2646 cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -15.0 \text{ mA}$	2.4	3.0		V
V_{OL}	Output LOW Current	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 64 \text{ mA}$		0.3	0.55	V
V_{OL}	Output LOW Current	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 12 \text{ mA (25}\Omega \text{ Series)}$		0.3	0.55	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$			-1	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$ $V_{OUT} = 2.7\text{V}$			1	μA
I_{OZL}	Output Current	$V_{OUT} = 0.5\text{V}$			-1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OFF}	Power Down Disable	$V_{CC} = \text{GND}, V_{OUT} = 4.5\text{V}$	—	—	100	μA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_{OUT} = \text{GND}$	-60	-120		mA
V_H	Input Hysteresis			200		mV

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.,	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open \bar{G} = DIR = GND or GAB = GBA = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle \bar{G} = DIR = GND or GAB = GBA = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle \bar{G} = DIR = GND or GAB = GBA = GND Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		7.0	12.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		9.2	21.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{\text{CC}} + \Delta I_{\text{CC}} D_H N_t + I_{\text{CCD}} (f_{\text{CP}}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_t = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at fi
 All currents are in milliamps and all frequencies are in megahertz.

PI74FCT646/2646T Switching Characteristics over Operating Range

PI74FCT646/648/651/652T

Parameters	Description	Conditions ⁽¹⁾	646T/2646T		646AT/2646AT		646CT		646DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
tPZH tPZL	Output Enable Time G̅, DIR to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ G̅, DIR to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tSU	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width ⁽³⁾ HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

PI74FCT648T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	648T		648AT		648CT		648DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
tPZH tPZL	Output Enable Time G̅, DIR to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ G̅, DIR to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tSU	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width ⁽³⁾ HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.

PI74FCT651T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	651T		651AT		651CT		651DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
tPHL	Bus to Bus										
tpZH	Output Enable Time	GBA, GAB to Bus	2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns
tpZL	GBA, GAB to Bus										
tpHZ	Output Disable Time ⁽³⁾	GBA, GAB to Bus	2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
tpLZ	GBA, GAB to Bus										
tPLH	Propagation Delay	Clock to Bus	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPHL	Clock to Bus										
tPLH	Propagation Delay	SBA or SAB to Bus	2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tPHL	SBA or SAB to Bus										
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width ⁽³⁾ HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

2

PI74FCT652/2652T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	652T/2652T		652AT/2652AT		652CT		652DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
tpZH	Output Enable Time		2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns
tpZL	GBA, GAB to Bus										
tpHZ	Output Disable Time ⁽³⁾		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
tpLZ	GBA, GAB to Bus										
tPLH	Propagation Delay		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
tPHL	Clock to Bus										
tPLH	Propagation Delay		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
tPHL	SBA or SAB to Bus										
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width ⁽³⁾ HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.



PI74FCT821T/823T/825T
(25Ω Series) PI74FCT2821T/2823T

Fast CMOS Bus Interface Registers

Product Features:

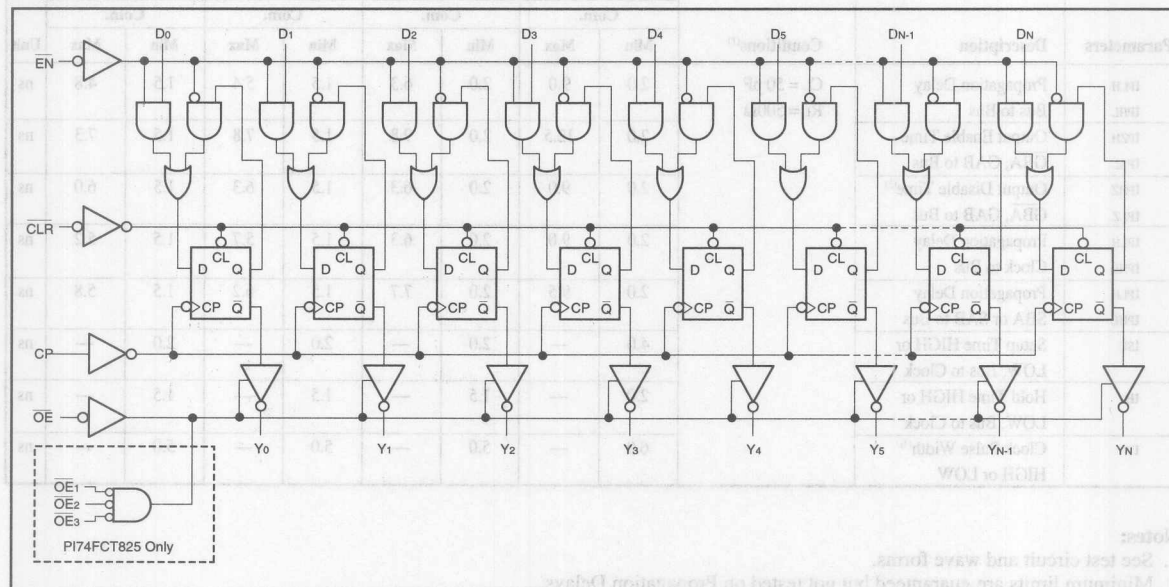
- PI74FCT821T/823T/825T/2821T/2823T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

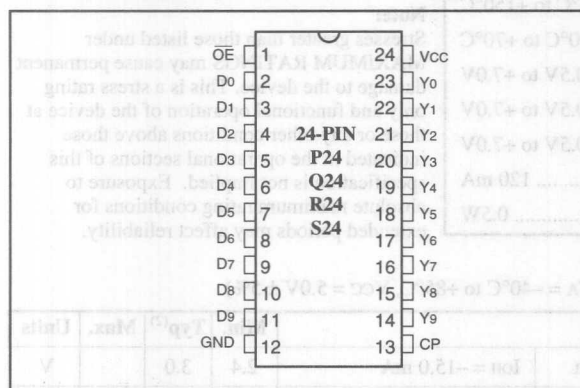
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT821T/2821T is a 10-bit wide register designed with ten D-type flip-flops with a buffered common clock and buffered 3-state outputs. The PI74FCT823/2823T is a 9-bit wide register designed with Clock Enable and Clear. The PI74FCT825T is an 8-bit wide register with all PI74FCT823T controls plus multiple enables. When output enable (OE) is LOW, the outputs are enabled. When OE is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

Logic Block Diagram



PI74FCT821/2821T Product Pin Configuration

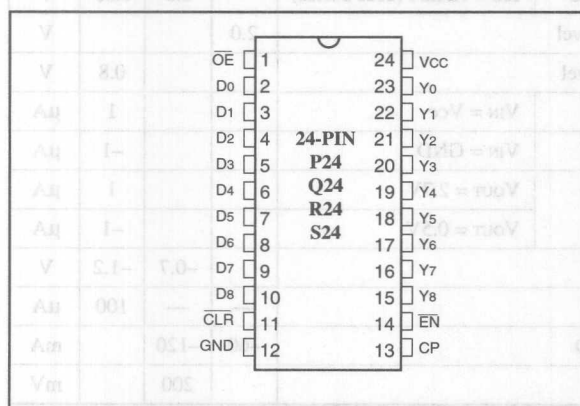


Product Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
DN	Data Inputs
YN	3-State Outputs
\overline{CLR}	Clear Input (Active LOW) (823/825/2823 Only)
\overline{EN}	Clock Enable Input (Active LOW)
GND	Ground
Vcc	Power

2

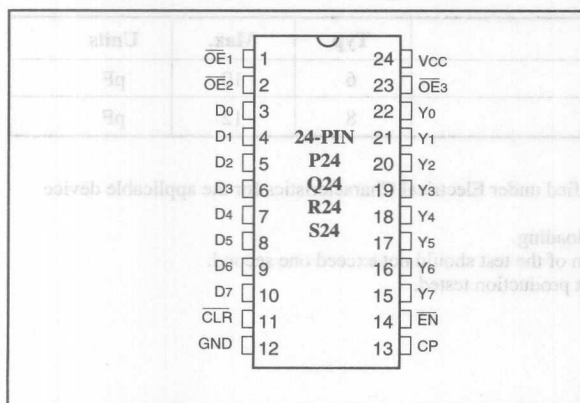
PI74FCT823/2823T Product Pin Configuration



PI74FCT821/823/825/2821/2823T Truth Table⁽¹⁾

Function	Inputs					Outputs	Internal
	\overline{CLR}	\overline{EN}	\overline{OE}	CP	DN	YN	QN
High-Z	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
Clear	L	X	H	X	X	Z	L
	L	X	L	X	X	L	L
Hold	H	H	H	X	X	Z	NC
	H	H	L	X	X	NC	NC
Load	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
	H	L	L	↑	L	L	L
	H	L	L	↑	H	H	H

PI74FCT825T Product Pin Configuration



1. H = High Voltage Level

L = Low Voltage Level

X = Don't Care

Z = High Impedance

NC = No Change

↑ = LOW-to-HIGH transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48 mA		0.3	0.50	V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA (25Ω Series)		0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current		V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V		—	—	100	μA
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-60	-120		mA
V _H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE = EN = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = EN = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.2	6.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = EN = GND Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.2	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccD} (f_{CP}/2 + f_i N_i)$$

I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT821/2821T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	821A/T/2821A/T		821B/T/2821B/T		821C/T/2821C/T		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay CP to Y _N (\overline{OE} = LOW)	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
t _{SU}	Setup Time HIGH or LOW, D _N to CP	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	ns
t _H	Hold Time HIGH or LOW, D _N to CP		2.0	—	1.5	—	1.5	—	ns
t _{SU}	Setup Time HIGH or LOW, \overline{EN} to CP		4.0	—	3.0	—	3.0	—	ns
t _H	Hold Time HIGH or LOW, \overline{EN} to CP		2.0	—	0	—	0	—	ns
t _{PHL}	Propagation Delay, CL _R to Y _N		1.5	14.0	1.5	9.0	1.5	8.0	ns
t _{REM}	Recovery Time, ⁽³⁾ CL _R to CP		6.0	—	6.0	—	6.0	—	ns
t _W	Clock Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.0	—	6.0	—	ns
t _W	CL _R Pulse Width ⁽³⁾ LOW		6.0	—	6.0	—	6.0	—	ns
t _{PEH} t _{PZL}	Output Enable Time \overline{OE} to Y _N	C _L = 50 pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ \overline{OE} to Y _N	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT823/2823T Switching Characteristics over Operating Range

2

Parameters	Description	Conditions ⁽¹⁾	823AT/2823AT		823BT/2823BT		823CT/2823CT		Unit
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay CP to YN (OE = LOW)	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
tsu	Setup Time HIGH or LOW, DN to CP	CL = 50 pF RL = 500Ω	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, DN to CP	—	2.0	—	1.5	—	1.5	—	ns
tsu	Setup Time HIGH or LOW, EN to CP	—	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, EN to CP	—	2.0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to YN	—	1.5	13.0	1.5	9.0	1.5	8.0	ns
tREM	Recovery Time, ⁽¹⁾ CLR to CP	—	6.0	—	6.0	—	6.0	—	ns
tw	Clock Pulse Width ⁽³⁾ HIGH or LOW	—	7.0	—	5.0	—	6.0	—	ns
tw	CLR Pulse Width ⁽³⁾ LOW	—	6.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time OE to YN	CL = 50 pF RL = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OE to YN	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT825T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	825AT		825BT		825CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay CP to YN (OE = LOW)	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
tsu	Setup Time HIGH or LOW, DN to CP	CL = 50 pF RL = 500Ω	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, DN to CP	—	2.0	—	1.5	—	1.5	—	ns
tsu	Setup Time HIGH or LOW, EN to CP	—	4.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW, EN to CP	—	2.0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to YN	—	1.5	13.0	1.5	9.0	1.5	8.0	ns
tREM	Recovery Time, CLR to CP	—	6.0	—	6.0	—	6.0	—	ns
tw	Clock Pulse Width HIGH or LOW	—	7.0	—	5.0	—	6.0	—	ns
tw	CLR Pulse Width ⁽³⁾ LOW	—	6.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time OE to YN	CL = 50 pF RL = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OE to YN	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.



PI74FCT827T/828T
(25Ω Series) PI74FCT2827T

Fast CMOS
10-Bit Buffers

2

Product Features:

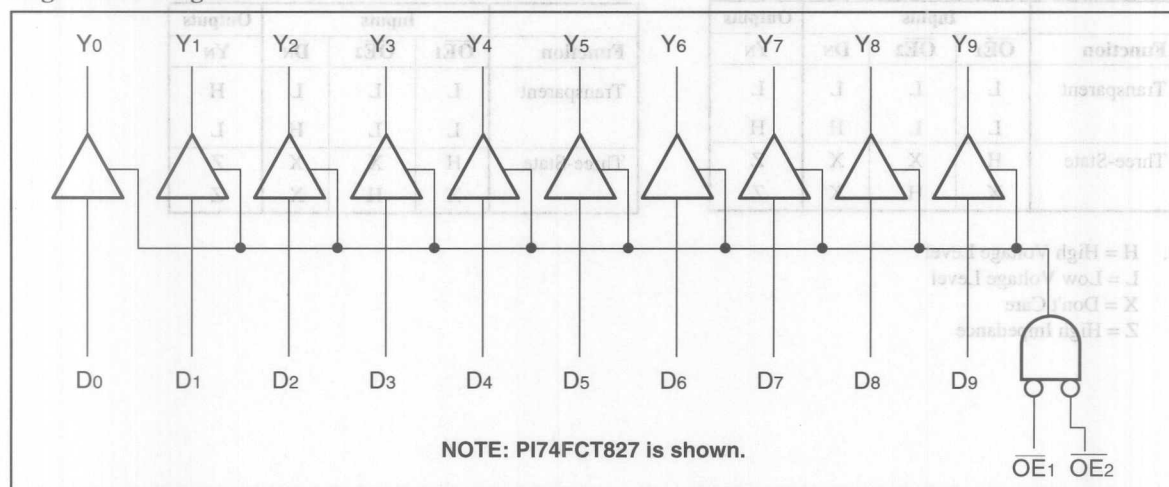
- PI74FCT827/828T/2827T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

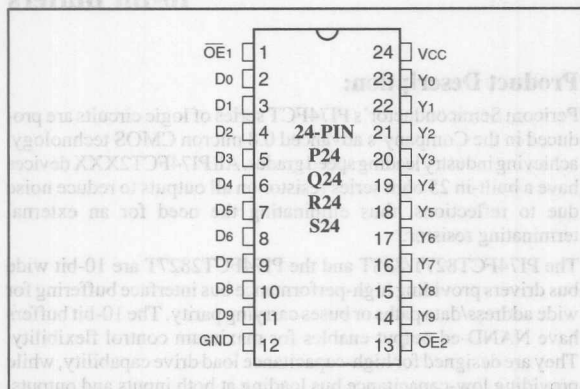
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT827T/828T and the PI74FCT2827T are 10-bit wide bus drivers providing high-performance bus interface buffering for wide address/data paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility. They are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. The PI74FCT827T/2827T is a non-inverting of the PI74FCT828T.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
OE _N	Output Enable Input (Active LOW)
D0-D9	10-bit Data Inputs
Y0-Y9	10-bit Data Outputs
GND	Ground
Vcc	Power

PI74FCT827/2827T Truth Table (Non-Inverting)⁽¹⁾

Function	Inputs			Outputs
	OE ₁	OE ₂	D _N	Y _N
Transparent	L	L	L	L
	L	L	H	H
Three-State	H	X	X	Z
	X	H	X	Z

PI74FCT828T Truth Table (Inverting)⁽¹⁾

Function	Inputs			Outputs
	OE ₁	OE ₂	D _N	Y _N
Transparent	L	L	L	H
	L	L	H	L
Three-State	H	X	X	Z
	X	H	X	Z

1. H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 48 mA		0.3	0.50	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 12 mA (25Ω Series)		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IIH	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max. VOUT = 2.7V			1	μA
IOZL	Output Current	VOUT = 0.5V			-1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	μA
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the appropriate device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE1 = OE2 = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE1 = OE2 = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{cc}		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = GND				
			V _{IN} = 3.4V		2.0	5.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE1 = OE2 = GND fi = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V _{IN} = GND				
			V _{IN} = V _{cc}		3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V		5.2	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_t + I_{ccD} (f_{CP}/2 + f_i N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_t = Number of TTL Inputs at D_H

I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT827T (non-inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	827AT/2827AT		827BT/2827BT		827CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay DN to YN	C _L = 50 pF R _L = 500Ω	1.5	6.5	1.5	5.0	1.5	4.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	ns
t _{PZH} t _{PZL}	Output Enable Time O _{EN} to YN	C _L = 50 pF R _L = 500Ω	1.5	9.5	1.5	8.0	1.5	7.0	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ O _{EN} to YN	C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	8.5	1.5	6.0	1.5	5.7	ns
		C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

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PI74FCT828T (inverting) Switching Characteristics over Operating Range

			828AT		828BT		828CT		
			Com.		Com.		Com.		
Parameters	Description	Conditions ⁽¹⁾	Min	Max	Min	Max	Min	Max	Unit
t _{PLH}	Propagation Delay DN to YN	C _L = 50 pF	1.5	6.5	1.5	5.5	1.5	4.4	ns
t _{PHL}		C _L = 500Ω							
		C _L = 300 pF ⁽³⁾	1.5	15.0	1.5	13.0	1.5	10.0	ns
		R _L = 500Ω							
t _{PZH}	Output Enable Time O _{EN} to YN	C _L = 50 pF	1.5	9.5	1.5	8.0	1.5	7.0	ns
t _{PZL}		R _L = 500Ω							
		C _L = 300 pF ⁽³⁾	1.5	23.0	1.5	15.0	1.5	14.0	ns
		R _L = 500Ω							
t _{PHZ}	Output Disable Time ⁽³⁾ O _{EN} to YN	C _L = 5 pF ⁽³⁾	1.5	8.5	1.5	6.0	1.5	5.7	ns
t _{PLZ}		R _L = 500Ω							
		C _L = 50 pF	1.5	10.0	1.5	7.0	1.5	6.0	ns
		R _L = 500Ω							

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.



PI74FCT841T/843T/845T (25Ω Series) PI74FCT2841T

Fast CMOS Bus Interface Latches

Product Features:

- PI74FCT841/843/845/2841T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

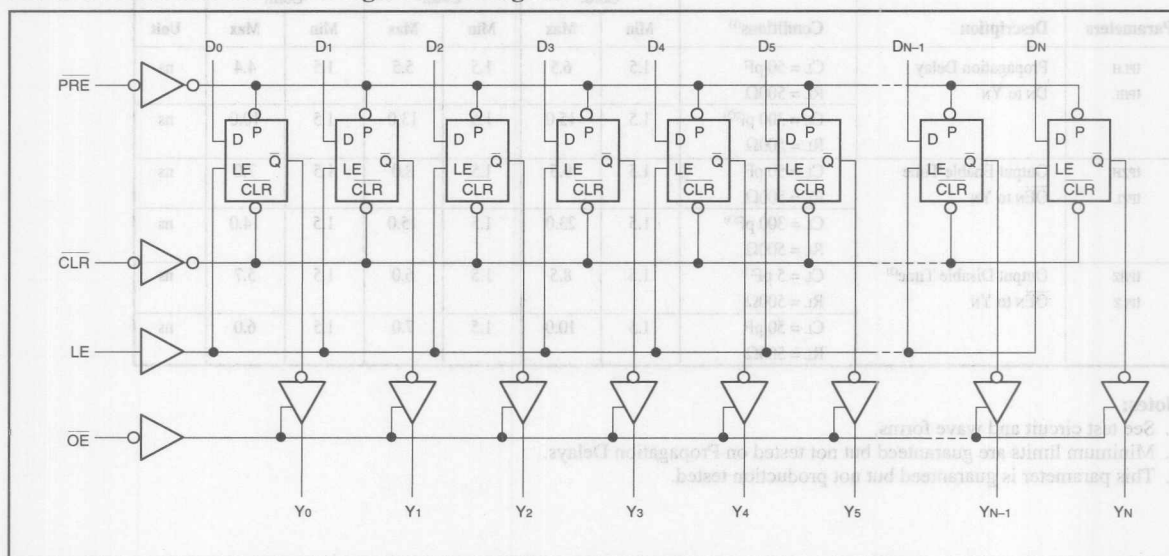
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT841T/843T/845T and PI74FCT2841T series are buffered interface latches. These transparent latches designed with 3-state outputs and are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When \overline{OE} is HIGH, the bus output is in the high impedance state.

The PI74FCT841/2841T is a 10-bit latch, the PI74FCT843T is a 9-bit latch, and the PI74FCT845T is an 8-bit latch.

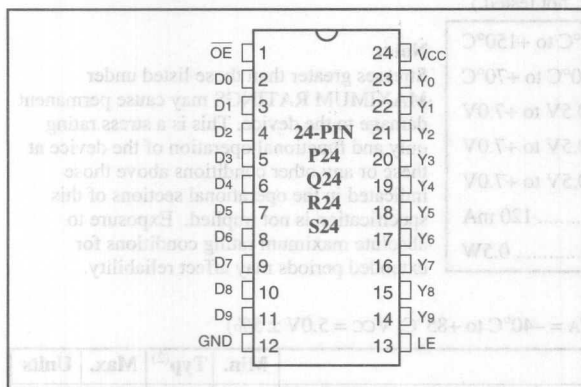
PI74FCT841/843/845/2842T Logic Block Diagram





PI74FCT841T/843T/845T
(25Ω Series) PI74FCT2841T
BUS INTERFACE LATCHES

PI74FCT841/2841T 10-Bit Latch
Product Configuration

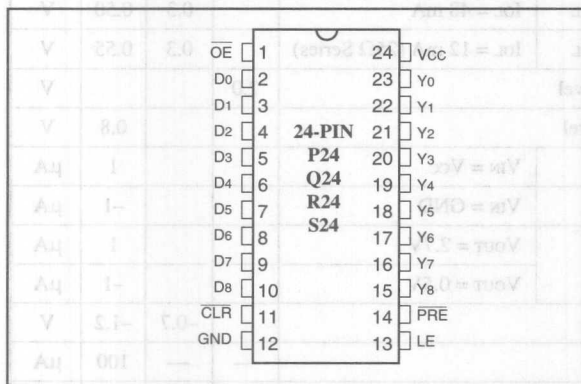


Product Pin Description

Pin Name	Description
YN	3-State Latch Outputs
DN	Latch Data Inputs
LE	Latch Enable Input
OE	Output Enable Control
CLR	Clear Latch
PRE	Preset Latch High, Preset Overrides CLR
GND	Ground
Vcc	Power

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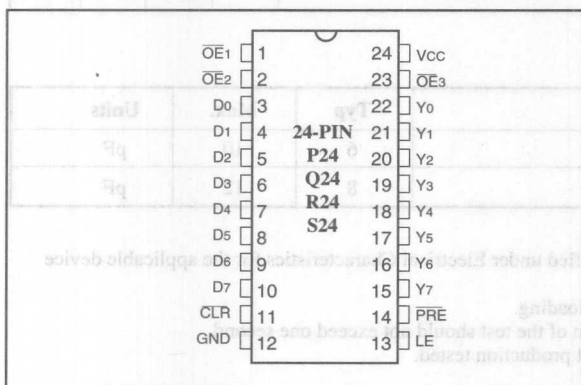
PI74FCT843T 9-Bit Latch Product Configuration



Truth Table⁽¹⁾

Function	Inputs					Outputs	Internal
	CLR	PRE	OE	LE	DN	YN	QN
High-Z	H	H	H	X	X	Z	X
	H	H	H	H	L	Z	L
	H	H	H	H	H	Z	H
Latched (High Z)	H	H	H	L	X	Z	NC
Transparent	H	H	L	H	L	L	L
	H	H	L	H	H	H	H
Latched	H	H	L	L	X	NC	NC
Preset	H	L	L	X	X	H	H
Clear	L	H	L	X	X	L	L
Preset	L	L	L	X	X	H	H
Latched (High Z)	L	H	H	L	X	Z	L
Latched (High Z)	H	L	H	L	X	Z	H

PI74FCT845T 8-Bit Latch Product Configuration



1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change
Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48 mA		0.3	0.50	V
V _{OL}	Output LOW Current	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA (25Ω Series)		0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current		V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V		—	—	100	μA
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-60	-120		mA
V _H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = GND; LE = V _{CC} One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND; LE = V _{CC} fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND; LE = V _{CC} Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.2	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT841/2841T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	841AT/2841AT		841BT/2841BT		841CT/2841CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay DN to YN (LE = HIGH)	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
tsu	Setup Time Data to LE	CL = 50 pF RL = 500Ω	2.5	—	2.5	—	2.5	—	ns
th	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
tPLH tPHL	Propagation Delay LE to YN	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	—	16.0	—	15.5	—	15.0	ns
tw	LE Pulse Width ⁽³⁾ (HIGH)	CL = 50 pF RL = 500Ω	4.0	—	4.0	—	4.0	—	ns
tpZH tpZL	Output Enable Time OE to YN	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ OE to YN	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns
		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT843T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT843AT		FCT843BT		FCT843CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay DN to YN (LE = HIGH)	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
tSU	Setup Time Data to LE	CL = 50 pF RL = 500Ω	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time Data to LE	—	2.5	—	2.5	—	2.5	—	ns
tPLH tPHL	Propagation Delay LE to YN	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
tPLH	Propagation Delay PRE to YN	CL = 50 pF RL = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
tREM	Recovery Time PRE to YN	—	1.5	11.0	1.5	10.0	1.5	9.0	ns
tPLH	Propagation Delay CLR to YN	—	1.5	11.0	1.5	10.0	1.5	9.0	ns
tREM	Recovery Time ⁽³⁾ CLR to YN	—	1.5	13.0	1.5	10.0	1.5	9.0	ns
tw	LE Pulse Width ⁽³⁾ (HIGH)	—	4.0	—	4.0	—	4.0	—	ns
tw	PRE Pulse Width ⁽³⁾ (LOW)	—	5.0	—	4.0	—	4.0	—	ns
tw	CLR Pulse Width ⁽³⁾ (LOW)	—	4.0	—	4.0	—	4.0	—	ns
tPZH tPZL	Output Enable Time OE to YN	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OE to YN	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT845T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT845AT		FCT845BT		FCT845CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
tPHL	DN to YN (LE = HIGH)		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0
tsu	Setup Time Data to LE	CL = 50 pF RL = 500Ω	2.5	—	2.5	—	2.5	—	ns
th	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
tPHL	LE to YN		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0
tPLH	Propagation Delay PRE to YN	CL = 50 pF RL = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
tREM	Recovery Time ⁽³⁾ PRE to YN		1.5	11.0	1.5	10.0	1.5	9.0	ns
tPLH	Propagation Delay CLR to YN		1.5	11.0	1.5	10.0	1.5	9.0	ns
tREM	Recovery Time ⁽³⁾ CLR to YN		1.5	13.0	1.5	10.0	1.5	9.0	ns
tw	LE Pulse Width ⁽³⁾ (HIGH)	—	4.0	—	4.0	—	4.0	—	ns
tw	PRE Pulse Width ⁽³⁾ (LOW)	—	5.0	—	4.0	—	4.0	—	ns
tw	CLR Pulse Width ⁽³⁾ (LOW)	—	4.0	—	4.0	—	4.0	—	ns
tpZH	Output Enable Time	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
tpZL	OE to YN		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0
tpHZ	Output Disable Time ⁽³⁾	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
tpLZ	OE to YN		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

Product Features:

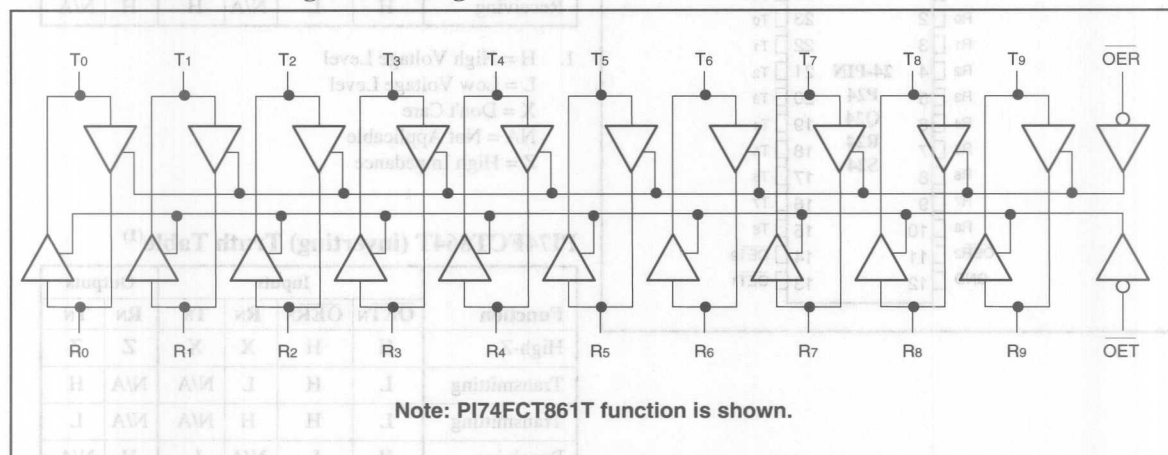
- PI74FCT861/863T/864T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

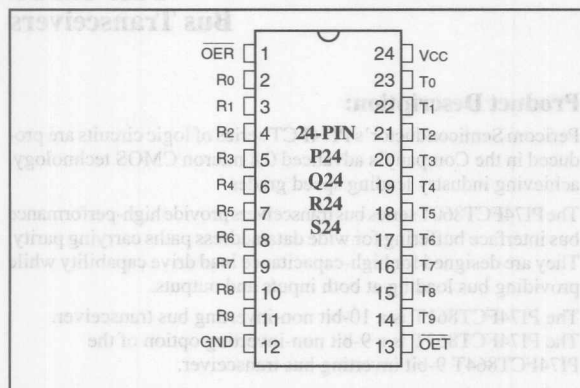
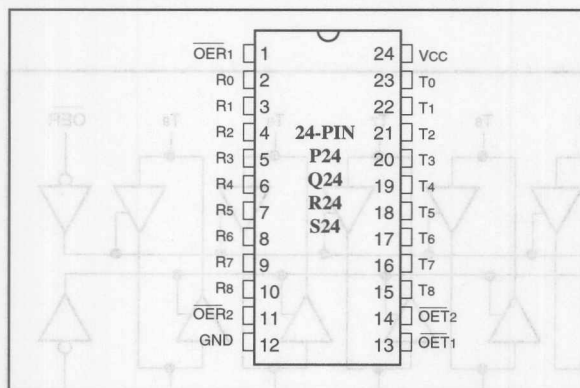
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT860T series bus transceivers provide high-performance bus interface buffering for wide data/address paths carrying parity. They are designed for high-capacitance load drive capability while providing bus loading at both inputs and outputs.

The PI74FCT861T is a 10-bit non-inverting bus transceiver. The PI74FCT863T is a 9-bit non-inverting option of the PI74FCT864T 9-bit inverting bus transceiver.

PI74FCT861/863/864T Logic Block Diagram


PI74FCT861T 10-Bit Product Configuration

PI74FCT863/864T 9-Bit Product Configuration

Product Pin Description

Pin Name	Description
RN	Receive Inputs/Outputs
TN	Transmit Inputs/Outputs
OERN	Output Enable Receive Mode
OETN	Output Enable Transmit Mode
GND	Ground
Vcc	Power

PI74FCT861/863T (non-inverting) Truth Table⁽¹⁾

Function	Inputs				Outputs	
	OETN	OERN	RN	TN	RN	TN
High-Z	H	H	X	X	Z	Z
Transmitting	L	H	L	N/A	N/A	L
Transmitting	L	H	H	N/A	N/A	H
Receiving	H	L	N/A	L	L	N/A
Receiving	H	L	N/A	H	H	N/A

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NA = Not Applicable
Z = High Impedance

PI74FCT864T (inverting) Truth Table⁽¹⁾

Function	Inputs				Outputs	
	OETN	OERN	RN	TN	RN	TN
High-Z	H	H	X	X	Z	Z
Transmitting	L	H	L	N/A	N/A	H
Transmitting	L	H	H	N/A	N/A	L
Receiving	H	L	N/A	L	H	N/A
Receiving	H	L	N/A	H	L	N/A

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NA = Not Applicable
Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 48 mA		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IIH	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max. VOUT = 2.7V			1	μA
IOZL	Output Current	VOUT = 0.5V			-1	μA
II	Input HIGH Current	VCC = Max., VIN = VCC (Max.)			20	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120		mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V	—	—	100	μA
VH	Input Hysteresis			200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10 ⁽⁵⁾	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = GND; LE = V _{CC} One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND; LE = V _{CC} fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OE = GND; LE = V _{CC} Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		5.2	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5. V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

$$I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_c = I_{\text{CC}} + \Delta I_{\text{CC}} D_H N_t + I_{\text{CCD}} (f_{\text{CP}}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_t = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT861T (non-inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	861AT		861BT		861CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay RN to TN or TN to RN	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	6.0	1.5	5.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	13.0	1.5	11.5	ns
tPZH tPZL	Output Enable Time OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.8	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	13.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.0	1.5	5.0	ns
		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

2
PI74FCT863T (non-inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	863AT		863BT		863CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay RN to TN or TN to RN	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	6.0	1.5	5.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	13.0	1.5	11.5	ns
tPZH tPZL	Output Enable Time OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.8	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	13.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.0	1.5	5.0	ns
		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT864T (inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	864AT		864BT		864CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay RN to TN or TN to RN	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	6.0	1.5	5.5	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	13.0	1.5	11.5	ns
tPZH tPZL	Output Enable Time OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.8	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	13.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.0	1.5	5.0	ns
		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

Parameters	Description	Conditions ⁽¹⁾	864AT		864BT		864CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay RN to TN or TN to RN	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	6.0	1.5	5.5	ns
tPHL		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	13.0	1.5	11.5	ns
tPZH	Output Enable Time OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.8	ns
tPZL		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	13.0	ns
tPHZ	Output Disable Time ⁽³⁾ OET to TN or OER to RN	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.0	1.5	5.0	ns
tPLZ		CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

High-Speed Inverted Hex Driver

2

Product Features:

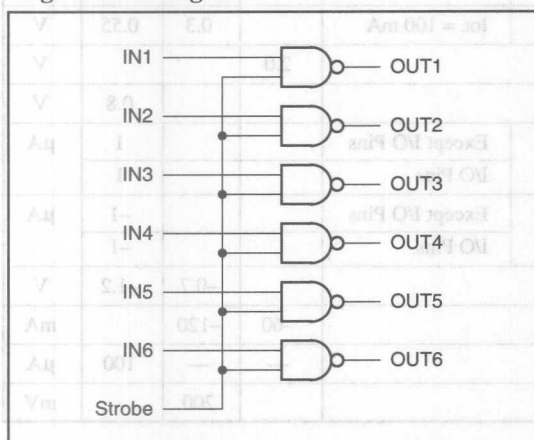
- High Drive Capability =
 $I_{OL} = 100 \mu A$
 $I_{OH} = -32 \mu A$ with capacitive loads up to 150 pF
- TTL input and output levels
- Extremely low static power
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Industrial operating temperature range: $-40^{\circ}C$ to $+85^{\circ}C$
- Packages available:
 - 16-pin 300 mil wide plastic DIP (P16)
 - 20-pin plastic PLCC (J20)

Product Description:

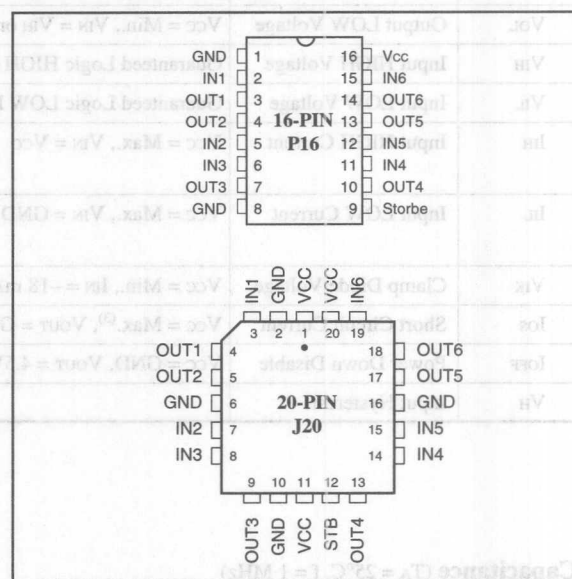
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT890T is a very high-speed, high-drive inverting hex driver capable of providing high-current drive into large capacitive loads. The device can be used as an inverting clock or DRAM driver, as well as high-speed buffer.

Logic Block Diagram



Product Pin Configurations



Truth Table⁽¹⁾

Inputs		Outputs
STB	IN	OUT
L	X	H
H	L	H
H	H	L

Note:

1. H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care

Product Pin Description

Pin Name	Description
IN0-IN6	Data Inputs
OUT0-OUT6	Data Outputs
Strobe	Strobe Input
GND	Ground
Vcc	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -32.0 mA	2.4	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 mA		0.3	0.55	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}	Except I/O Pins			1	μA
			I/O Pins			1	
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND	Except I/O Pins			-1	μA
			I/O Pins			-1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-60	-120		mA
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V		—	—	100	μA
V _H	Input Hysteresis				200		mV

Capacitance ($T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OEA or OEB = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OEA or OEB = GND f _I = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		2.0	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.5	6.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle OEA or OEB = GND Eight Bits Toggling f _I = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		4.3	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.5	16.8 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	890T		Unit
			Min	Max	
t _{PLH}	Propagation Delay, Data	C _L = 150 pF	3.0	9.0	ns
t _{PHL}	& Strobe to Low-to-High	R _L = 500Ω			

Notes:

- See test circuit and wave forms.
- Input pulse is supplied by a generator with the following characteristics: PRR = 1 MHz, Z_{OUT} = 50, and t_r & t_f < 2.0 ns
- C_L includes probe and jig capacitance.

I _C	Total Power Supply Current ⁽⁴⁾	V _{CC} = Max., Output Open f _{IN} = 10 MHz 50% Duty Cycle OE _A or OE _B = GND t _{IN} = 3 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	2.0	4.0 ⁽⁵⁾
			V _{IN} = 3.4V V _{IN} = GND	2.2	6.0 ⁽⁵⁾
			V _{IN} = V _{CC} V _{IN} = GND	4.3	7.8 ⁽⁵⁾
			V _{IN} = 3.4V V _{IN} = GND	6.2	10.8 ⁽⁵⁾

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.0V, +25°C ambient.
- For TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the test formula. These limits are guaranteed but not tested.
- I_C = I_{CC} + I_{ALOC} + I_{OE} + I_{OE2} + I_{OE3} + I_{OE4}
- I_{CC} = Quiescent Current
- I_{ALOC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
- I_{OE} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
- I_{OE2} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
- I_{OE3} = Input Frequency
- I_{OE4} = Number of inputs at I_{OE}

All currents are in milliamperes and all frequencies are in megahertz.

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DOUBLE DENSITY STANDARD 5V FCT LOGIC PRODUCTS

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PI74FCT162841T	20-Bit Transparent Latch with Balanced Output Drives	3.84
PI74FCT162952T	16-Bit Non-inverting Registered Transceiver with Balanced Output Drives	3.90



PI74FCT16240T PI74FCT162240T

Fast CMOS 16-Bit Buffer/Line Drivers

Product Features:

Common Features:

- PI74FCT16240T and PI74FCT162240T are high-speed, low power devices with high current drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

PI74FCT16240T Features:

- High output drive: $I_{OH} = -32mA$; $I_{OL} = 64mA$
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162240T Features:

- Balanced output drivers: $\pm 24mA$
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

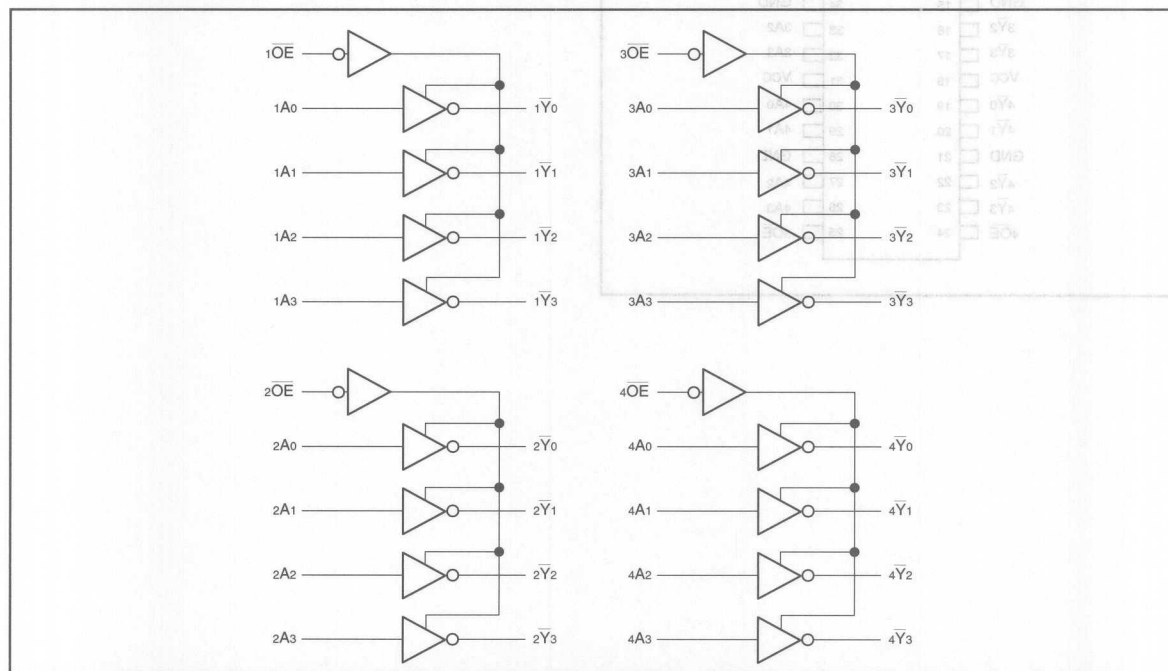
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The PI74FCT16240T and PI74FCT162240T are inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. These devices are designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The PI74FCT16240T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162240T has $\pm 24mA$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Description

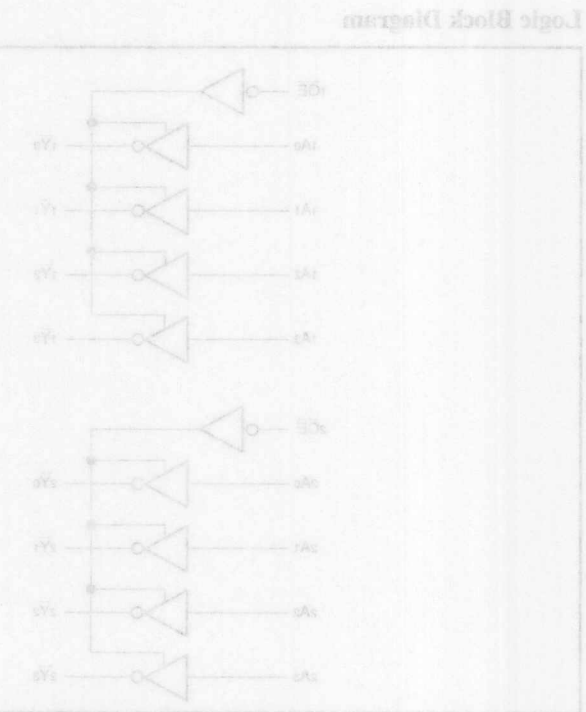
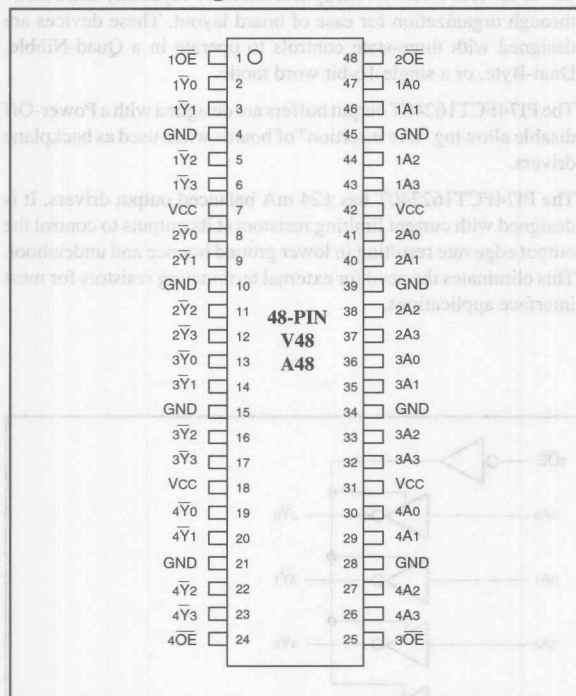
Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	H
L	H	L
H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max. V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max. V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{CC} = Max. V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16240T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5	V
			I _{OH} = -15.0 mA	2.4	3.5	
			I _{OH} = -32.0 mA	2.0	3.0	
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA	0.2	0.55	V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162240T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA	0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4 V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		60	100	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		0.7	2.5 ⁽⁵⁾	mA
			V _{IN} = 3.4 V V _{IN} = GND		0.9	3.3 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND		2.5	5.5 ⁽⁵⁾	
			V _{IN} = 3.4 V V _{IN} = GND		6.5	17.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0 V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamperes and all frequencies are in megahertz.

PI74FCT16240T Switching Characteristics over Operating Range

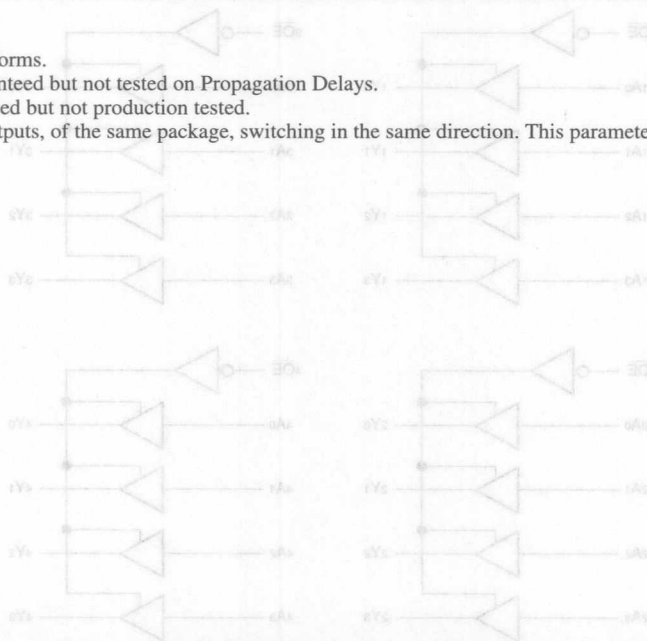
PI74FCT16240T Switching Characteristics over Operating Range												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	16240T		16240AT		16240CT		16240DT		16240ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	1.5	3.6	1.5	3.2	ns
tPHL	xAX to xYx												
tpZH	Output Enable Time	xOE to xAX or xYx	1.5	10.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns
tpZL	xOE to xAX or xYx												
tpHZ	Output Disable Time ⁽³⁾	xOE to xAX or xYx	1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.0	1.5	3.6	ns
tpLZ	xOE to xAX or xYx												
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162240T Switching Characteristics over Operating Range

PI74FCT162240T Switching Characteristics over Operating Range												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	162240T		162240AT		162240CT		162240DT		162240ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	1.5	3.6	1.5	3.2	ns
tPHL	xAX to xYx												
tpZH	Output Enable Time	xOE to xAX or xYx	1.5	10.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns
tpZL	xOE to xAX or xYx												
tpHZ	Output Disable Time ⁽³⁾	xOE to xAX or xYx	1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.0	1.5	3.6	ns
tpLZ	xOE to xAX or xYx												
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.





PI74FCT16244T
PI74FCT162244T

**Fast CMOS 16-Bit
Buffer/Line Drivers**

Product Features:

Common Features:

- PI74FCT16244T and PI74FCT162244T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

PI74FCT16244T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162244T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

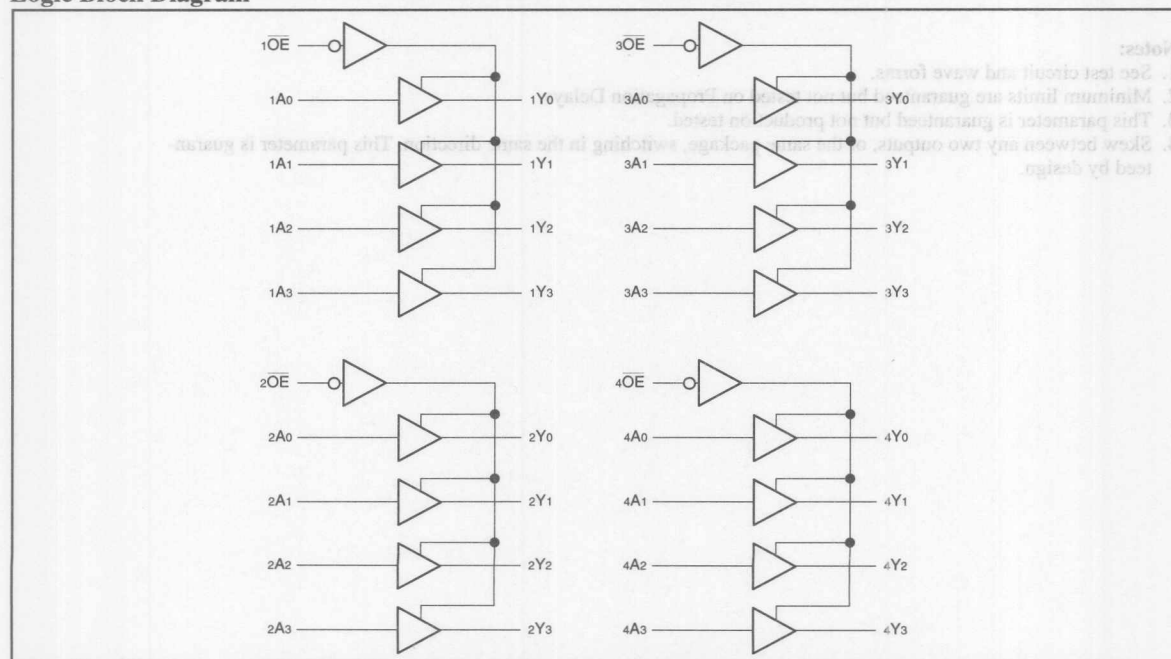
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16244T and PI74FCT162244T are non-inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. These devices are designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The PI74FCT16244T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162244T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	L
L	H	H
H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

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Product Pin Configuration

Pin		Pin		Pin		Pin	
1	OE	2	Y0	3	Y1	4	GND
5	Y2	6	Y3	7	VCC	8	Y0
9	Y1	10	GND	11	Y2	12	Y3
13	VCC	14	Y0	15	GND	16	Y1
17	Y2	18	Y3	19	VCC	20	Y0
21	GND	22	Y1	23	Y2	24	Y3
25	OE	26	Y0	27	Y1	28	GND
29	Y2	30	Y3	31	VCC	32	Y0
33	GND	34	Y1	35	Y2	36	Y3
37	VCC	38	Y0	39	GND	40	Y1
41	Y2	42	Y3	43	VCC	44	Y0
45	GND	46	Y1	47	Y2	48	Y3
49	OE	50	Y0	51	Y1	52	GND
53	Y2	54	Y3	55	VCC	56	Y0
57	GND	58	Y1	59	Y2	60	Y3
61	VCC	62	Y0	63	GND	64	Y1
65	Y2	66	Y3	67	VCC	68	Y0
69	GND	70	Y1	71	Y2	72	Y3
73	OE	74	Y0	75	Y1	76	GND
77	Y2	78	Y3	79	VCC	80	Y0
81	GND	82	Y1	83	Y2	84	Y3
85	VCC	86	Y0	87	GND	88	Y1
89	Y2	90	Y3	91	VCC	92	Y0
93	GND	94	Y1	95	Y2	96	Y3
97	OE	98	Y0	99	Y1	100	GND
101	Y2	102	Y3	103	VCC	104	Y0
105	GND	106	Y1	107	Y2	108	Y3
109	VCC	110	Y0	111	GND	112	Y1
113	Y2	114	Y3	115	VCC	116	Y0
117	GND	118	Y1	119	Y2	120	Y3
121	OE	122	Y0	123	Y1	124	GND
125	Y2	126	Y3	127	VCC	128	Y0
129	GND	130	Y1	131	Y2	132	Y3
133	VCC	134	Y0	135	GND	136	Y1
137	Y2	138	Y3	139	VCC	140	Y0
141	GND	142	Y1	143	Y2	144	Y3
145	OE	146	Y0	147	Y1	148	GND
149	Y2	150	Y3	151	VCC	152	Y0
153	GND	154	Y1	155	Y2	156	Y3
157	VCC	158	Y0	159	GND	160	Y1
161	Y2	162	Y3	163	VCC	164	Y0
165	GND	166	Y1	167	Y2	168	Y3
169	OE	170	Y0	171	Y1	172	GND
173	Y2	174	Y3	175	VCC	176	Y0
177	GND	178	Y1	179	Y2	180	Y3
181	VCC	182	Y0	183	GND	184	Y1
185	Y2	186	Y3	187	VCC	188	Y0
189	GND	190	Y1	191	Y2	192	Y3
193	OE	194	Y0	195	Y1	196	GND
197	Y2	198	Y3	199	VCC	200	Y0
201	GND	202	Y1	203	Y2	204	Y3
205	VCC	206	Y0	207	GND	208	Y1
209	Y2	210	Y3	211	VCC	212	Y0
213	GND	214	Y1	215	Y2	216	Y3
217	OE	218	Y0	219	Y1	220	GND
221	Y2	222	Y3	223	VCC	224	Y0
225	GND	226	Y1	227	Y2	228	Y3
229	VCC	230	Y0	231	GND	232	Y1
233	Y2	234	Y3	235	VCC	236	Y0
237	GND	238	Y1	239	Y2	240	Y3
241	OE	242	Y0	243	Y1	244	GND
245	Y2	246	Y3	247	VCC	248	Y0
249	GND	250	Y1	251	Y2	252	Y3
253	VCC	254	Y0	255	GND	256	Y1
257	Y2	258	Y3	259	VCC	260	Y0
261	GND	262	Y1	263	Y2	264	Y3
265	OE	266	Y0	267	Y1	268	GND
269	Y2	270	Y3	271	VCC	272	Y0
273	GND	274	Y1	275	Y2	276	Y3
277	VCC	278	Y0	279	GND	280	Y1
281	Y2	282	Y3	283	VCC	284	Y0
285	GND	286	Y1	287	Y2	288	Y3
289	OE	290	Y0	291	Y1	292	GND
293	Y2	294	Y3	295	VCC	296	Y0
297	GND	298	Y1	299	Y2	300	Y3
301	VCC	302	Y0	303	GND	304	Y1
305	Y2	306	Y3	307	VCC	308	Y0
309	GND	310	Y1	311	Y2	312	Y3
313	OE	314	Y0	315	Y1	316	GND
317	Y2	318	Y3	319	VCC	320	Y0
321	GND	322	Y1	323	Y2	324	Y3
325	VCC	326	Y0	327	GND	328	Y1
329	Y2	330	Y3	331	VCC	332	Y0
333	GND	334	Y1	335	Y2	336	Y3
337	OE	338	Y0	339	Y1	340	GND
341	Y2	342	Y3	343	VCC	344	Y0
345	GND	346	Y1	347	Y2	348	Y3
349	VCC	350	Y0	351	GND	352	Y1
353	Y2	354	Y3	355	VCC	356	Y0
357	GND	358	Y1	359	Y2	360	Y3
361	OE	362	Y0	363	Y1	364	GND
365	Y2	366	Y3	367	VCC	368	Y0
369	GND	370	Y1	371	Y2	372	Y3
373	VCC	374	Y0	375	GND	376	Y1
377	Y2	378	Y3	379	VCC	380	Y0
381	GND	382	Y1	383	Y2	384	Y3
385	OE	386	Y0	387	Y1	388	GND
389	Y2	390	Y3	391	VCC	392	Y0
393	GND	394	Y1	395	Y2	396	Y3
397	VCC	398	Y0	399	GND	400	Y1
401	Y2	402	Y3	403	VCC	404	Y0
405	GND	406	Y1	407	Y2	408	Y3
409	OE	410	Y0	411	Y1	412	GND
413	Y2	414	Y3	415	VCC	416	Y0
417	GND	418	Y1	419	Y2	420	Y3
421	VCC	422	Y0	423	GND	424	Y1
425	Y2	426	Y3	427	VCC	428	Y0
429	GND	430	Y1	431	Y2	432	Y3
433	OE	434	Y0	435	Y1	436	GND
437	Y2	438	Y3	439	VCC	440	Y0
441	GND	442	Y1	443	Y2	444	Y3
445	VCC	446	Y0	447	GND	448	Y1
449	Y2	450	Y3	451	VCC	452	Y0
453	GND	454	Y1	455	Y2	456	Y3
457	OE	458	Y0	459	Y1	460	GND
461	Y2	462	Y3	463	VCC	464	Y0
465	GND	466	Y1	467	Y2	468	Y3
469	VCC	470	Y0	471	GND	472	Y1
473	Y2	474	Y3	475	VCC	476	Y0
477	GND	478	Y1	479	Y2	480	Y3
481	OE	482	Y0	483	Y1	484	GND
485	Y2	486	Y3	487	VCC	488	Y0
489	GND	490	Y1	491	Y2	492	Y3
493	VCC	494	Y0	495	GND	496	Y1
497	Y2	498	Y3	499	VCC	500	Y0
501	GND	502	Y1	503	Y2	504	Y3
505	OE	506	Y0	507	Y1	508	GND
509	Y2	510	Y3	511	VCC	512	Y0
513	GND	514	Y1	515	Y2	516	Y3
517	VCC	518	Y0	519	GND	520	Y1
521	Y2	522	Y3	523	VCC	524	Y0
525	GND	526	Y1	527	Y2	528	Y3
529	OE	530	Y0	531	Y1	532	GND
533	Y2	534	Y3	535	VCC	536	Y0
537	GND	538	Y1	539	Y2	540	Y3
541	VCC	542	Y0	543	GND	544	Y1
545	Y2	546	Y3	547	VCC	548	Y0
549	GND	550	Y1	551	Y2	552	Y3
553	OE	554	Y0	555	Y1	556	GND
557	Y2	558	Y3	559	VCC	560	Y0
561	GND	562	Y1	563	Y2	564	Y3
565	VCC	566	Y0	567	GND	568	Y1
569	Y2	570	Y3	571	VCC	572	Y0
573	GND	574	Y1	575	Y2	576	Y3
577	OE	578	Y0	579	Y1	580	GND
581	Y2	582	Y3	583	VCC	584	Y0
585	GND	586	Y1	587	Y2	588	Y3
589	VCC	590	Y0	591	GND	592	Y1
593	Y2	594	Y3	595	VCC	596	Y0
597	GND	598	Y1	599	Y2	600	Y3

Parameter	Description	Test Conditions	Typ	Max	Units
C _{in}	Input Capacitance	V _{in} = 0V	1.5	6	pF
C _{out}	Output Capacitance	V _{out} = 0V	2.5	8	pF

- Notes:
- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
 - Typical values are at V_{cc} = 5.0V, +25°C ambient and maximum loading.
 - Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
 - This parameter is determined by device characterization but is not production tested.

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$, $V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$			-1	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$, $V_{OUT} = 2.7\text{V}$			1	μA
I_{OZL}	Output Current	$V_{CC} = \text{Max.}$, $V_{OUT} = 0.5\text{V}$			-1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}$, $V_{OUT} = \text{GND}$	-80	-140	-200	mA
I_O	Output Drive Current	$V_{CC} = \text{Max.}^{(3)}$, $V_{OUT} = 2.5\text{V}$	-50		-180	mA
V_H	Input Hysteresis			100		mV

PI74FCT16244T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -3.0\text{ mA}$	2.5	3.5		V
		$I_{OH} = -15.0\text{ mA}$	2.4	3.5		
		$I_{OH} = -32.0\text{ mA}$	2.0	3.0		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OL} = 64\text{ mA}$		0.2	0.55	V
I_{OFF}	Power Down Disable	$V_{CC} = 0\text{V}$, V_{IN} or $V_{OUT} \leq 4.5\text{V}$	—	—	± 100	μA

PI74FCT162244T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -24.0\text{ mA}$	2.4	3.3		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OL} = 24\text{ mA}$		0.3	0.55	V
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$	60	115	150	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$	-60	-115	-150	mA

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	5.5	8	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		60	100	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND	V _{IN} = V _{cc} V _{IN} = GND		0.7	2.5 ⁽⁵⁾	mA
		One Bit Toggling	V _{IN} = 3.4V V _{IN} = GND		0.9	3.3 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND	V _{IN} = V _{cc} V _{IN} = GND		2.5	5.5 ⁽⁵⁾	
		16 Bits Toggling	V _{IN} = 3.4V V _{IN} = GND		6.5	17.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{cp}/2 + f_i N_i)$$

$$I_{cc} = \text{Quiescent Current}$$

$$\Delta I_{cc} = \text{Power Supply Current for a TTL High Input (V}_{IN} = 3.4V)$$

$$D_H = \text{Duty Cycle for TTL Inputs High}$$

$$N_T = \text{Number of TTL Inputs at } D_H$$

$$I_{ccd} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$$

$$f_{cp} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$$

$$f_i = \text{Input Frequency}$$

$$N_i = \text{Number of Inputs at } f_i$$

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16244T Switching Characteristics over Operating Range

PI74FCT16244T Switching Characteristics over Operating Range												Preliminary		
			16244T		16244AT		16244CT		16244DT		16244ET			
			Com.		Com.		Com.		Com.		Com.			
Parameters	Description	Conditions ⁽¹⁾	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.8	1.5	3.2	ns	
tPHL	xAx to xYx													
tPZH	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns	
tPZL	xOE to xAx or xYx													
tPHZ	Output Disable Time ⁽³⁾		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	1.5	3.6	ns	
tPLZ	xOE to xAx or xYx													
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns	

PI74FCT162244T Switching Characteristics over Operating Range

P174FCT162244T Switching Characteristics over Operating Range											Preliminary		
Parameters	Description	Conditions ⁽¹⁾	162244T		162244AT		162244CT		162244DT		162244ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.8	1.5	3.2	ns
tPHL	xAx to xYx												
tPZH	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns
tPZL	xOE to xAx or xYx												
tPHZ	Output Disable Time ⁽³⁾		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	1.5	3.6	ns
tPLZ	xOE to xAx or xYx												
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74FCT16245T
PI74FCT162245T

Fast CMOS 16-Bit Bidirectional Transceivers

Product Features:

Common Features:

- PI74FCT16245T and PI74FCT162245T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

PI74FCT16245T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162245T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

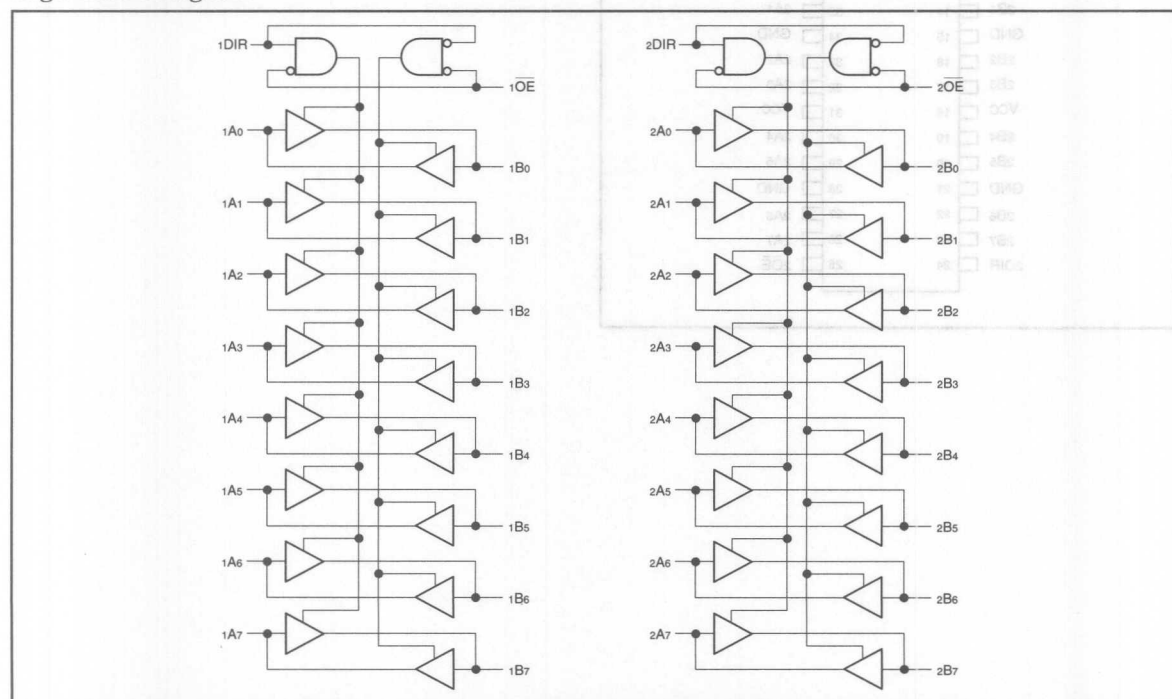
The PI74FCT16245T and PI74FCT162245T are 16-bit bidirectional transceivers designed for asynchronous two-way communication between data buses. The direction control input pin (xDIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The PI74FCT16245T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162245T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

3

Logic Block Diagram



Product Pin Description

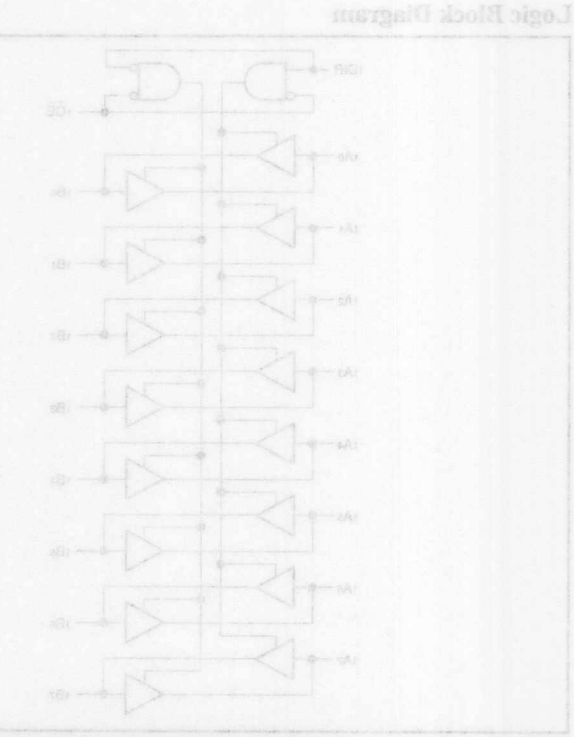
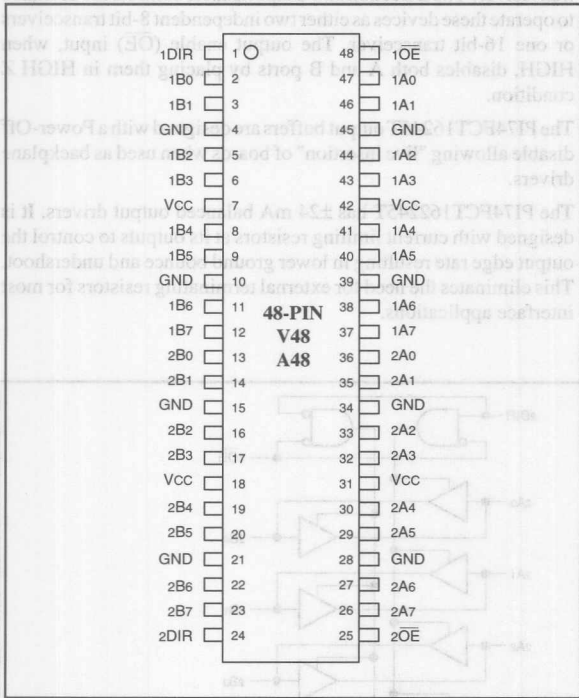
Pin Name	Description
xOE	Output Enable Inputs (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max., V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16245T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5	V
			I _{OH} = -15.0 mA	2.4	3.5	
			I _{OH} = -32.0 mA	2.0	3.0	
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA	0.2	0.55	V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162245T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA	0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = xDIR = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		60	100	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = xDIR = GND One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		0.7	2.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		0.9	3.3 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = xDIR = GND 16 Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND		2.5	5.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.5	17.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16245T Switching Characteristics over Operating Range

PI74FCT16245T Switching Characteristics over Operating Range												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	16245T		16245AT		16245CT		16245DT		16245ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	1.5	3.2	ns
tPHL													
tPZH	Output Enable Time xOE to A or B		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.4	ns
tPZL													
tPHZ	Output Disable Time ⁽³⁾ xOE to A or B		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
tPLZ													
tPZH	Output Enable Time xDIR to A or B ⁽³⁾		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.8	ns
tPZL													
tPHZ	Output Disable Time xDIR to A or B ⁽³⁾		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
tPLZ													
tSK(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162245T Switching Characteristics over Operating Range

PI74FCT162245T Switching Characteristics over Operating Range												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	162245T		162245AT		162245CT		162245DT		162245ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	1.5	3.2	ns
t _{PHL}	A to B, B to A												
t _{PZH}	Output Enable Time	xOE to A or B	1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.4	ns
t _{PZL}	xOE to A or B												
t _{PHZ}	Output Disable Time ⁽³⁾	xOE to A or B	1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
t _{PLZ}	xOE to A or B												
t _{PZH}	Output Enable Time	xDIR to A or B ⁽³⁾	1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.8	ns
t _{PZL}	xDIR to A or B ⁽³⁾												
t _{PHZ}	Output Disable Time	xDIR to A or B ⁽³⁾	1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
t _{PLZ}	xDIR to A or B ⁽³⁾												
t _{SK(o)}	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

01/15/95

Product Pin Description

Pin Name	Description
xOE	Output Enable Inputs (Active LOW)
xLE	Latch Enable Inputs (Active HIGH)
xDx	Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾			Outputs ⁽¹⁾
xDx	xOE	xLE	xOx
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

3

Product Pin Configuration

Pin	Symbol	Function	Pin	Symbol	Function
1	OE	Output Enable (Active LOW)	48	LE	Latch Enable (Active HIGH)
2	100	Input 0	47	1D0	Output 0
3	101	Input 1	46	1D1	Output 1
4	GND	Ground	45	GND	Ground
5	102	Input 2	44	1D2	Output 2
6	103	Input 3	43	1D3	Output 3
7	VCC	Power	42	VCC	Power
8	104	Input 4	41	1D4	Output 4
9	105	Input 5	40	1D5	Output 5
10	GND	Ground	39	GND	Ground
11	106	Input 6	38	1D6	Output 6
12	107	Input 7	37	1D7	Output 7
13	200	Input 8	36	2D0	Output 8
14	101	Input 9	35	2D1	Output 9
15	GND	Ground	34	GND	Ground
16	202	Input 10	33	2D2	Output 10
17	203	Input 11	32	2D3	Output 11
18	VCC	Power	31	VCC	Power
19	204	Input 12	30	2D4	Output 12
20	205	Input 13	29	2D5	Output 13
21	GND	Ground	28	GND	Ground
22	206	Input 14	27	2D6	Output 14
23	207	Input 15	26	2D7	Output 15
24	2OE	Output Enable (Active LOW)	25	2LE	Latch Enable (Active HIGH)

Parameter	Description	Test Conditions	Typ	Max.	Units
Q _{in}	Input Capacitance	V _{in} = 0V	4.5	6	pF
Q _{out}	Output Capacitance	V _{out} = 0V	5.5	8	pF

1. For conditions show as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{cc} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	VCC = Max. V _{IN} = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max. V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	VCC = Max. V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	VCC = Max. V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16373T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5		
			I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		—	—	±100	μA

PI74FCT162373T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = −24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		−60	−115	−150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND, xLE = V _{CC} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		60	100	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND, xLE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		0.7	2.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		0.9	3.3 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND, xLE = V _{CC} 16 Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND		2.5	5.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.5	17.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_I + I_{CCD} (f_{CP}/2 + f_i N_I)$$

I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_I = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_I = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16373T Switching Characteristics over Operating Range

												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	16373T		16373AT		16373CT		16373DT		16373ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay xDx to xOx	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
tPHL													
tPLH	Propagation Delay xLE to xOx		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	3.7	ns
tPHL													
tpZH	Output Enable Time xOE to xOx		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
tpZL													
tpHZ	Output Disable Time ⁽³⁾ xOE to xOx		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
tplZ													
tsu	Setup Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
th	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.0	—	1.0	—	ns
tw	xLE Pulse Width HIGH ⁽³⁾	6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns	
tsk(o)	Output Skew ⁽⁴⁾	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns	

PI74FCT162373T Switching Characteristics over Operating Range

Preliminary												Unit	
Parameters	Description	Conditions ⁽¹⁾	162373T		162373AT		162373CT		162373DT		162373ET		
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min		Max
tPLH	Propagation Delay xDx to xOx	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
tPLH	Propagation Delay xLE to xOx		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	3.7	ns
tpZH	Output Enable Time xOE to xOx		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
tpHZ	Output Disable Time ⁽³⁾ xOE to xOx		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
tsu	Setup Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
th	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.0	—	1.0	—	ns
tw	xLE Pulse Width HIGH ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74FCT16374T
PI74FCT162374T

Fast CMOS 16-Bit Registers (3-State)

Product Features:

Common Features:

- PI74FCT16374T and PI74FCT162374T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

PI74FCT16374T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162374T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

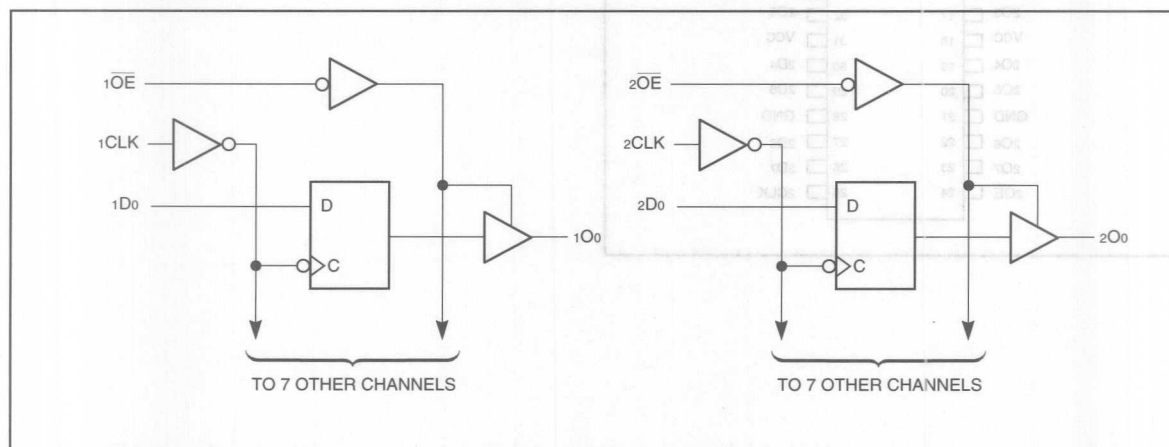
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16374T and PI74FCT162374T are 16-bit octal registers designed with 16 D-type flip-flops with a buffered common clock and 3-state outputs. The Output Enable (\overline{xOE}) and clock ($xCLK$) controls are organized to operate as two 8-bit registers or one 16-bit register. When \overline{OE} is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The PI74FCT16374T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162374T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

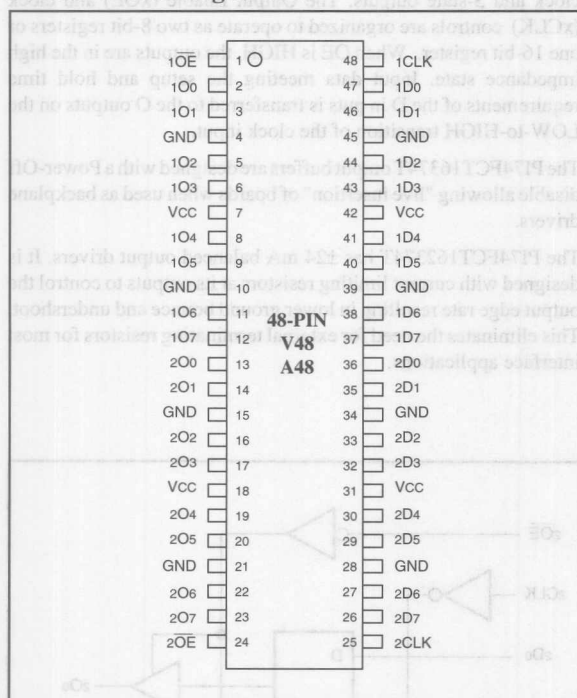
Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xCLK	Clock Inputs
xDx	Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

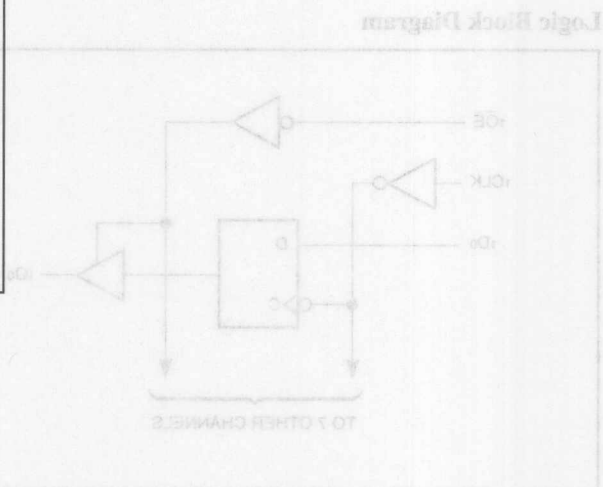
Product Pin Configuration



Truth Table⁽¹⁾

Function	Inputs			Outputs
	xDx	xCLK	xOE	xOx
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

- H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance
 ↑ = LOW-to-HIGH transition



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max., V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16374T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5	V
			I _{OH} = -15.0 mA	2.4	3.5	
			I _{OH} = -32.0 mA	2.0	3.0	
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA		0.2	0.55 V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162374T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA		0.3	0.55 V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		60	100	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle xOE = GND fi = 5 MHz 50% Duty Cycle One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		0.7	2.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.2	4.0 ⁽⁵⁾	
			V _{IN} = V _{cc} V _{IN} = GND		3.1	6.5 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = 3.4V V _{IN} = GND		7.6	20.0 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

$$I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_c = I_{\text{cc}} + \Delta I_{\text{cc}} D_H N_T + I_{\text{ccD}} (f_{\text{CP}}/2 + f_i N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16374T Switching Characteristics over Operating Range

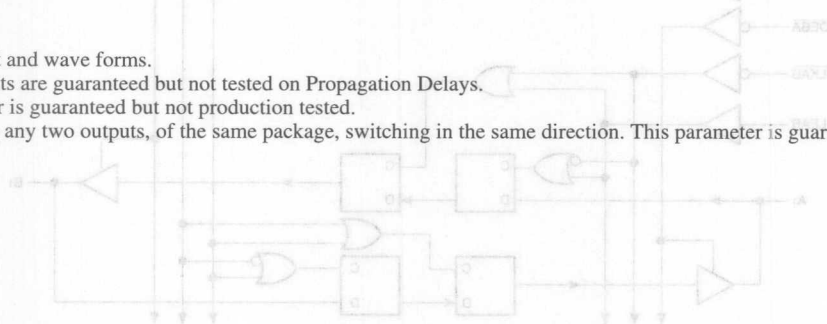
P174FCT16374T Switching Characteristics over Operating Range												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	16374T		16374AT		16374CT		16374DT		16374ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	2.0	4.2	1.5	3.7	ns
tPHL	xCLKx to xOx												
tpZH	Output Enable Time	xOE to xOx	1.5	12.5	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
tpZL	xOE to xOx												
tpHZ	Output Disable Time ⁽³⁾	xOE to xOx	1.5	8.0	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
tpLZ	xOE to xOx												
tsu	Setup Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	1.5	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	xCLK Pulse Width HIGH or LOW ⁽³⁾		7.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

3
PI74FCT162374T Switching Characteristics over Operating Range

P174FCT162374T Switching Characteristics over Operating Range												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	162374T		162374AT		162374CT		162374DT		162374ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xCLKx to xOx	CL = 50 pF RL = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	2.0	4.2	1.5	3.7	ns
tpZH tpZL	Output Enable Time xOE to xOx		1.5	12.5	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ xOE to xOx		1.5	8.0	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
tsu	Setup Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	1.5	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	xCLK Pulse Width HIGH or LOW ⁽³⁾		7.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.





PI74FCT16500T PI74FCT162500T

Fast CMOS 18-Bit Registered Transceivers

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16500T and PI74FCT162500T are 18-bit registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and OEBA, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using OEBA, LEBA and CLKBA. These high-speed, low power devices offer a flow-through organization for ease of board layout.

The PI74FCT16500T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162500T has ± 24 mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Product Features:

Common Features:5

- PI74FCT16500T and PI74FCT162500T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

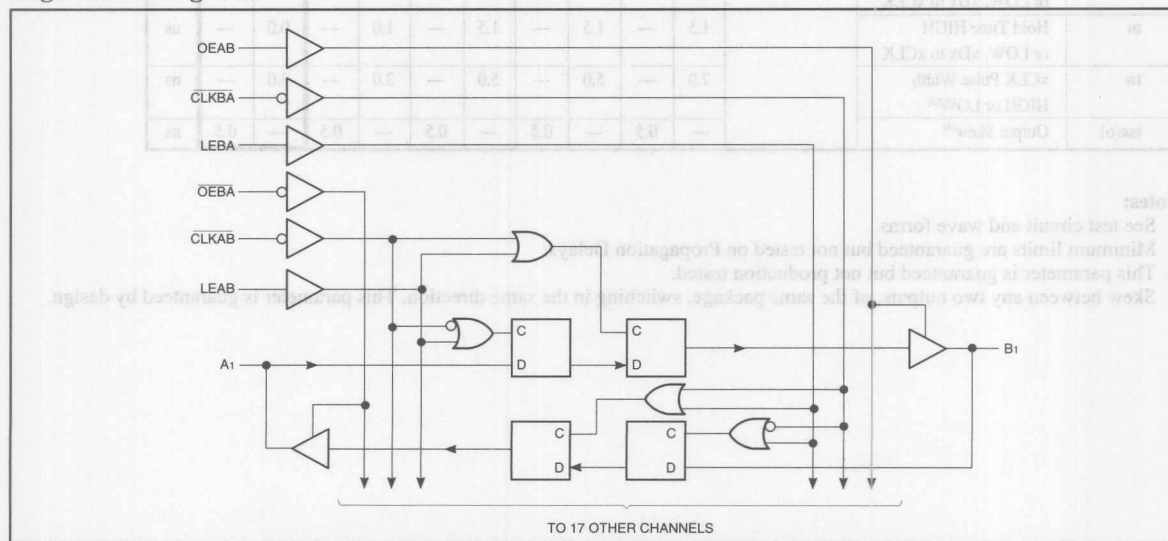
PI74FCT16500T Features:

- High output drive: $I_{OH} = -32$ mA; $I_{OL} = 64$ mA
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162500T Features:

- Balanced output drivers: ± 24 mA
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Logic Block Diagram



Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input (Active LOW)
CLKBA	B-to-A Clock Input (Active LOW)
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
Vcc	Power

Truth Table^(1,4)

Inputs			Outputs	
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ⁽²⁾
H	L	L	X	B ⁽³⁾

3
NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
4. H = High Voltage Level
L = Low Voltage Level
Z = High Impedance
↓ = HIGH-to-LOW Transition

Product Pin Configuration

OEAB	1	56	GND
LEAB	2	55	CLKAB
A0	3	54	B0
GND	4	53	GND
A1	5	52	B1
A2	6	51	B2
VCC	7	50	VCC
A3	8	49	B3
A4	9	48	B4
A5	10	47	B5
GND	11	46	GND
A6	12	45	B6
A7	13	44	B7
A8	14	43	B8
A9	15	42	B9
A10	16	41	B10
A11	17	40	B11
GND	18	39	GND
A12	19	38	B12
A13	20	37	B13
A14	21	36	B14
VCC	22	35	VCC
A15	23	34	B15
A16	24	33	B16
GND	25	32	GND
A17	26	31	B17
OEBA	27	30	CLKBA
LEBA	28	29	GND

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$			-1	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$ $V_{OUT} = 2.7\text{V}$			1	μA
I_{OZL}	Output Current	$V_{CC} = \text{Max.}$ $V_{OUT} = 0.5\text{V}$			-1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_{OUT} = \text{GND}$	-80	-140	-200	mA
I_O	Output Drive Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_{OUT} = 2.5\text{V}$	-50		-180	mA
V_H	Input Hysteresis			100		mV

PI74FCT16500T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}				V
		$I_{OH} = -3.0\text{ mA}$	2.5	3.5		
		$I_{OH} = -15.0\text{ mA}$	2.4	3.5		
		$I_{OH} = -32.0\text{ mA}$	2.0	3.0		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}		0.2	0.55	V
I_{OFF}	Power Down Disable	$V_{CC} = 0\text{V}$, V_{IN} or $V_{OUT} \leq 4.5\text{V}$	—	—	± 100	μA

PI74FCT162500T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}				V
		$I_{OH} = -24.0\text{ mA}$	2.4	3.3		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}		0.3	0.55	V
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾	60	115	150	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾	-60	-115	-150	mA

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OEAB = OEBA = V _{CC} or GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (CLKAB) 50% Duty Cycle OEAB = OEBA = V _{CC} LEAB = GND One Bit Toggling f _I = 5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.8	2.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	4.2 ⁽⁵⁾	
		V _{CC} = Max., Output Open f _{CP} = 10 MHz (CLKAB) 50% Duty Cycle OEAB = OEBA = V _{CC} LEAB = GND Eighteen Bits Toggling f _I = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	7.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		8.6	21.85 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_C = Total Power Supply Current

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_{HNT} = Duty Cycle for TTL Inputs High

N_I = Number of TTL Inputs at High

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at High

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16500T Switching Characteristics over Operating Range

Preliminary											
Parameters	Description	Conditions ⁽¹⁾	16500AT		16500CT		16500DT		16500ET		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{MAX}	CLKAB or CLKBA frequency	C _L = 50 pF	—	150	—	150	—	150	—	150	MHz
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Ax to Bx	R _L = 500 Ω	1.5	5.1	1.5	4.6	1.5	4.1	—	3.8	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	—	4.2	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	—	4.2	ns
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6.0	1.5	5.6	1.5	5.0	—	4.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	5.2	1.5	4.8	—	4.0	ns
t _{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		3.0	—	3.0	—	3.0	—	2.4	—	ns
t _H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	ns
t _{SU}	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock HIGH	3.0	—	3.0	—	3.0	—	2.0	—	ns
		Clock LOW	1.5	—	1.5	—	1.5	—	1.5	—	ns
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	0.5	—	ns
t _W	LEAB or LEBA Pulse Width HIGH ⁽³⁾		3.0	—	3.0	—	3.0	—	3.0	—	ns
t _W	CLKAB or CLKBA Pulse Width HIGH ⁽³⁾ or LOW		3.0	—	3.0	—	3.0	—	3.0	—	ns
t _{SK(O)}	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

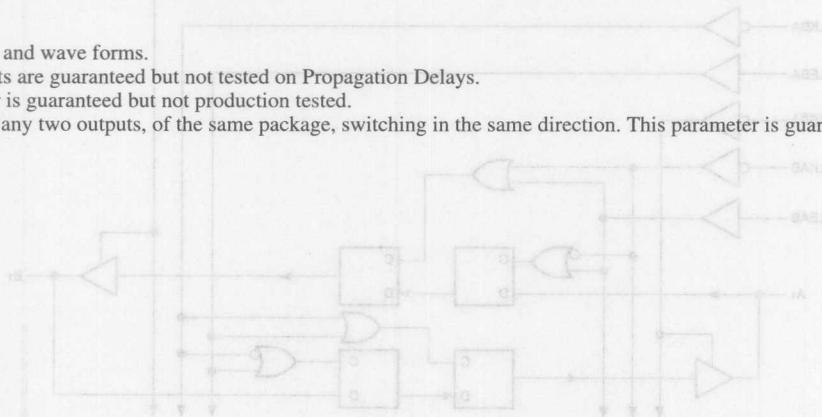
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162500T Switching Characteristics over Operating Range

162500AT/162500CT/162500DT Switching Characteristics over Operating Range										Preliminary		
Parameters	Description	Conditions ⁽¹⁾	162500AT		162500CT		162500DT		162500ET		Unit	
			Com.		Com.		Com.		Com.			
			Min	Max	Min	Max	Min	Max	Min	Max		
t _{MAX}	CLKAB or CLKBA frequency	C _L = 50 pF	—	150	—	150	—	150	—	150	MHz	
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Ax to Bx	R _L = 500 Ω	1.5	5.1	1.5	4.6	1.5	4.1	—	3.8	ns	
t _{PLH} t _{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	—	4.2	ns	
t _{PLH} t _{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	—	4.2	ns	
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6.0	1.5	5.6	1.5	5.0	—	4.8	ns	
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	5.2	1.5	4.8	—	4.0	ns	
t _{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		3.0	—	3.0	—	3.0	—	2.4	—	ns	
t _H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	ns	
t _{SU}	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock HIGH	3.0	—	3.0	—	3.0	—	2.0	—	ns	
		Clock LOW	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	0.5	—	ns	
t _W	LEAB or LEBA Pulse Width HIGH ⁽³⁾		3.0	—	3.0	—	3.0	—	3.0	—	ns	
t _W	CLKAB or CLKBA Pulse Width HIGH ⁽³⁾ or LOW		3.0	—	3.0	—	3.0	—	3.0	—	ns	
t _{SK(o)}	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.





PI74FCT16501T
PI74FCT162501T

Fast CMOS 18-Bit Registered Transceivers

Product Features:

Common Features:

- PI74FCT16501T and PI74FCT162501T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

PI74FCT16501T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162501T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

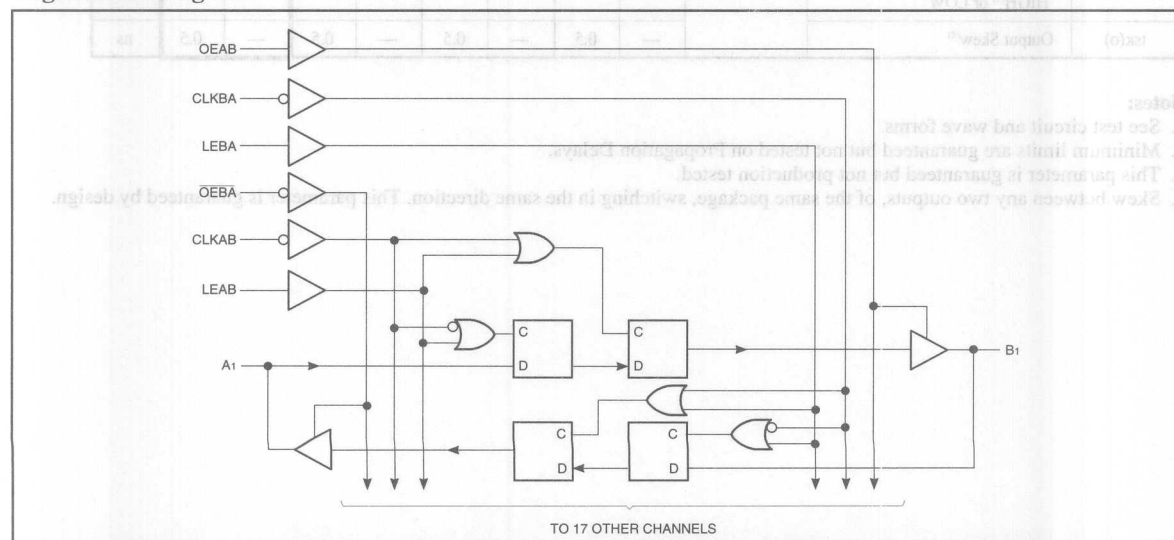
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16501T and PI74FCT162501T are 18-bit registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and OEBA, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using OEBA, LEBA and CLKBA. These high-speed, low power devices offer a flow-through organization for ease of board layout.

The PI74FCT16501T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162501T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
Vcc	Power

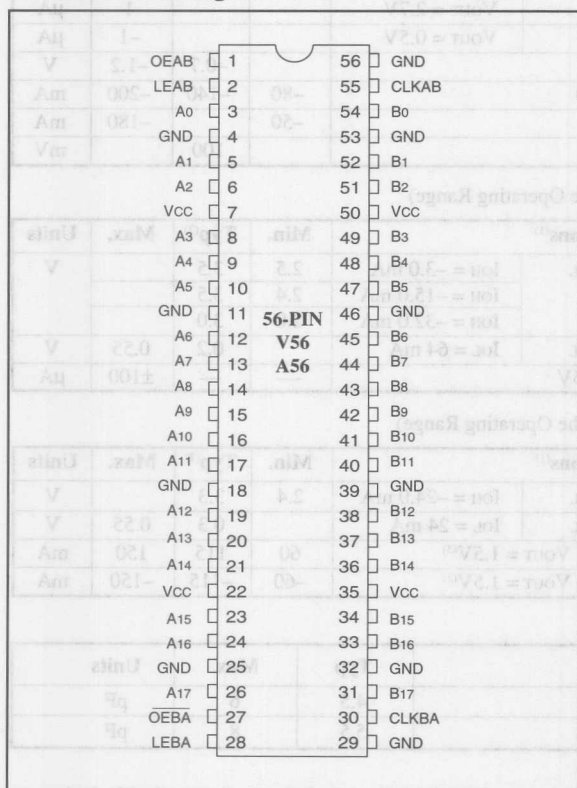
Truth Table^(1,4)

Inputs			Outputs	
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ⁽²⁾
H	L	L	X	B ⁽³⁾

NOTES:

1. A-toB data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
4. H = High Voltage Level
L = Low Voltage Level
Z = High Impedance
↓ = HIGH-to-LOW Transition

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$, $V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$			-1	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$, $V_{OUT} = 2.7\text{V}$			1	μA
I_{OZL}	Output Current	$V_{CC} = \text{Max.}$, $V_{OUT} = 0.5\text{V}$			-1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}$, $V_{OUT} = \text{GND}$	-80	-140	-200	mA
I_O	Output Drive Current	$V_{CC} = \text{Max.}^{(3)}$, $V_{OUT} = 2.5\text{V}$	-50		-180	mA
V_H	Input Hysteresis			100		mV

PI74FCT16501T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -3.0\text{ mA}$	2.5	3.5		V
		$I_{OH} = -15.0\text{ mA}$	2.4	3.5		
		$I_{OH} = -32.0\text{ mA}$	2.0	3.0		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OL} = 64\text{ mA}$		0.2	0.55	V
I_{OFF}	Power Down Disable	$V_{CC} = 0\text{V}$, V_{IN} or $V_{OUT} \leq 4.5\text{V}$	—	—	± 100	μA

PI74FCT162501T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -24.0\text{ mA}$	2.4	3.3		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OL} = 24\text{ mA}$		0.3	0.55	V
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$	60	115	150	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$	-60	-115	-150	mA

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OEAB = OEBA = V _{CC} or GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (CLKAB) 50% Duty Cycle OEAB = OEBA = V _{CC} LEAB = GND One Bit Toggling f _I = 5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.8	2.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	4.2 ⁽⁵⁾	
		V _{CC} = Max., Output Open f _{CP} = 10 MHz (CLKAB) 50% Duty Cycle OEAB = OEBA = V _{CC} LEAB = GND Eighteen Bits Toggling f _I = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	7.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		8.6	21.85 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_I N_I)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_I = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16501T Switching Characteristics over Operating Range

16501ET										Preliminary	
Parameters	Description	Conditions ⁽¹⁾	16501AT		16501CT		16501DT		16501ET		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tMAX	CLKAB or CLKBA frequency	C _L = 50 pF	—	150	—	150	—	150	—	150	MHz
tPLH tPHL	Propagation Delay Ax to Bx or Ax to Bx	R _L = 500 Ω	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns
tPLH tPHL	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
tPLH tPHL	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
tPZH tPZL	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns
tSU	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		3.0	—	3.0	—	3.0	—	2.4	—	ns
tH	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	ns
tSU	Setup Time HIGH or LOW	Clock HIGH	3.0	—	3.0	—	3.0	—	2.0	—	ns
	Ax to LEAB, Bx to LEBA	Clock LOW	1.5	—	1.5	—	1.5	—	1.5	—	ns
tH	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	0.5	—	ns
tW	LEAB or LEBA Pulse Width HIGH ⁽³⁾		3.0	—	3.0	—	3.0	—	3.0	—	ns
tW	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽³⁾		3.0	—	3.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

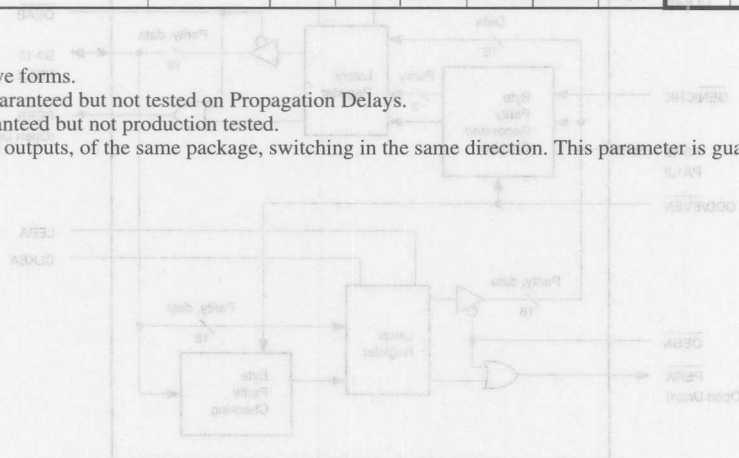
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162501T Switching Characteristics over Operating Range

74FCT162501T Switching Characteristics over Operating Range											Preliminary	
Parameters	Description	Conditions ⁽¹⁾	162501AT		162501CT		162501DT		162501ET		Unit	
			Com.		Com.		Com.		Com.			
			Min	Max	Min	Max	Min	Max	Min	Max		
t _{MAX}	CLKAB or CLKBA frequency	C _L = 50 pF	—	150	—	150	—	150	—	150	MHz	
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Ax to Bx	R _L = 500 Ω	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns	
t _{PLH} t _{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns	
t _{PLH} t _{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns	
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns	
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns	
t _{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		3.0	—	3.0	—	3.0	—	2.4	—	ns	
t _H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	ns	
t _{SU}	Setup Time Clock HIGH		3.0	—	3.0	—	3.0	—	2.0	—	ns	
	HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	0.5	—	ns	
t _w	LEAB or LEBA Pulse Width HIGH ⁽³⁾		3.0	—	3.0	—	3.0	—	3.0	—	ns	
t _w	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽³⁾		3.0	—	3.0	—	3.0	—	3.0	—	ns	
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.





PI74FCT16511T
PI74FCT162511T

Product Features:

Common Features:

- PI74FCT16511 and PI74FCT162511 are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Typical tsk(o) (Output Skew) < 250 ps, clocked mode
- Extended range of $-40^{\circ}C$ to $+85^{\circ}C$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide TSSOP (A56)
 - 56-pin 300 mil wide SSOP (V56)

PI74FCT16511T Features:

- High output drive: $I_{OH} = -32$ mA; $I_{OL} = 64$ mA
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}C$

PI74FCT162511T Features:

- High output drive: $I_{OL}/I_{OH} = 24$ mA
- Open drain parity error allows wire-OR
- Typical VOLP (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}C$
- Balanced output drivers: ± 24 mA
- Series current limiting resistors

Fast CMOS 16-Bit Registered/Latched Transceiver With Parity

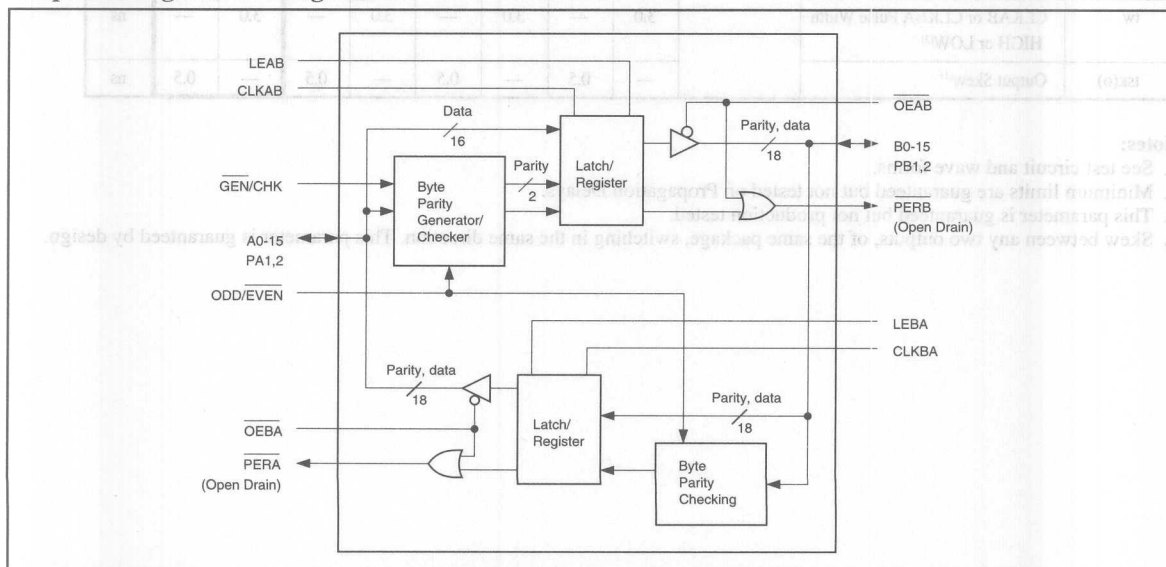
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

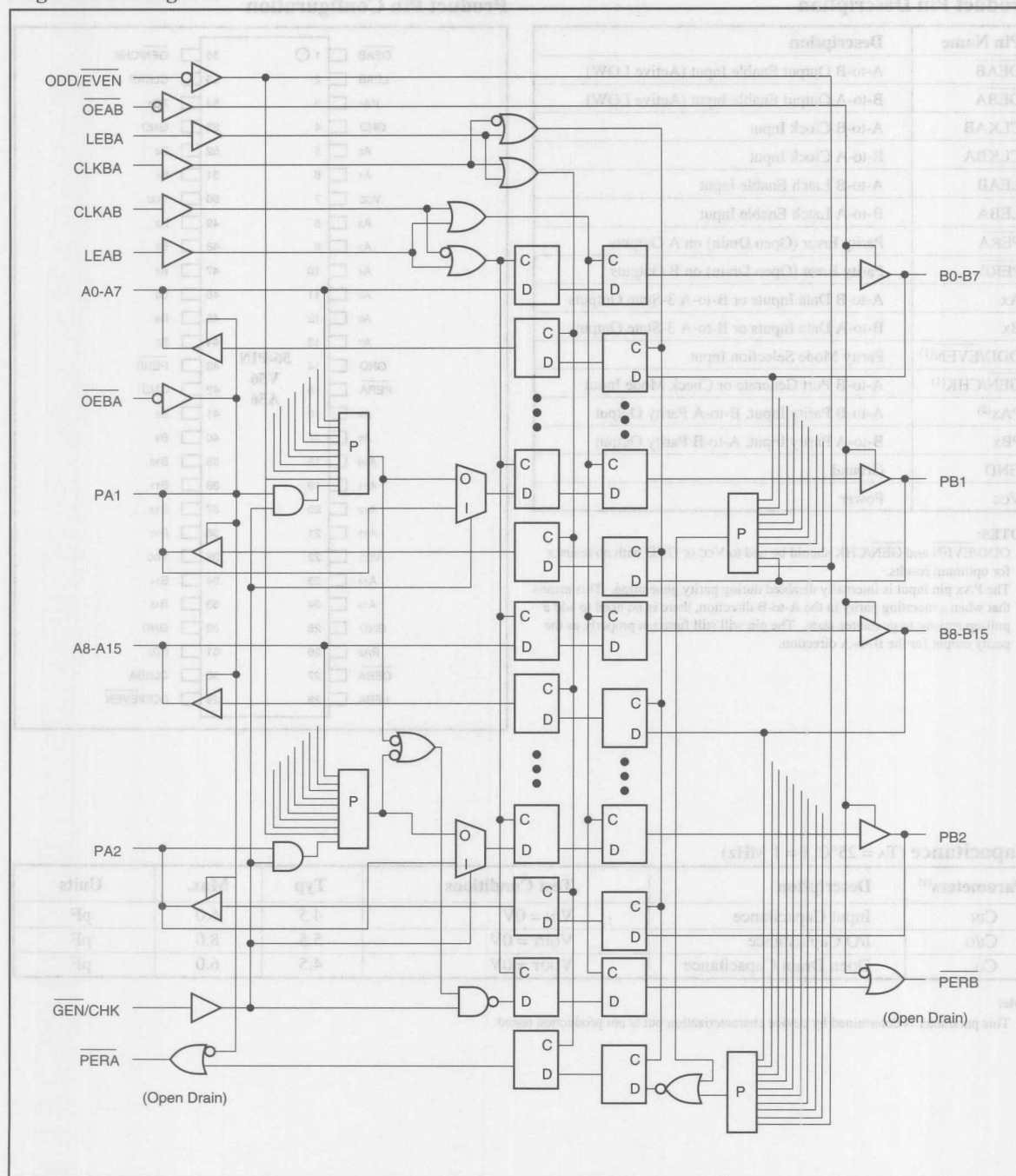
The PI74FCT16511T and PI74FCT162511T are high-speed, low-power 16-bit registered/latched transceiver with parity which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched or clocked modes. It has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. One error flag for each direction (A-to-B or B-to-A) exists to indicate an error for either byte in either direction. The parity error flags which are open drain outputs, can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. To disable the error flag during combinational transitions, a designer can disable the parity error flag by the OE_{xx} control pins.

The operation in A-to-B direction is controlled by LEAB, CLKAB and OEAB control pins, and the operation in B-to-A direction is controlled by LEBA, CLKBA and OEBA control pins. GEN/CHK is used to select the operation of A-to-B direction, while B-to-A direction is always in checking mode. The ODD/EVEN select is common between the two directions. Independent operation can be achieved between the two directions by using the corresponding control lines except for the ODD/EVEN control.

Simplified Logic Block Diagram



Logic Block Diagram



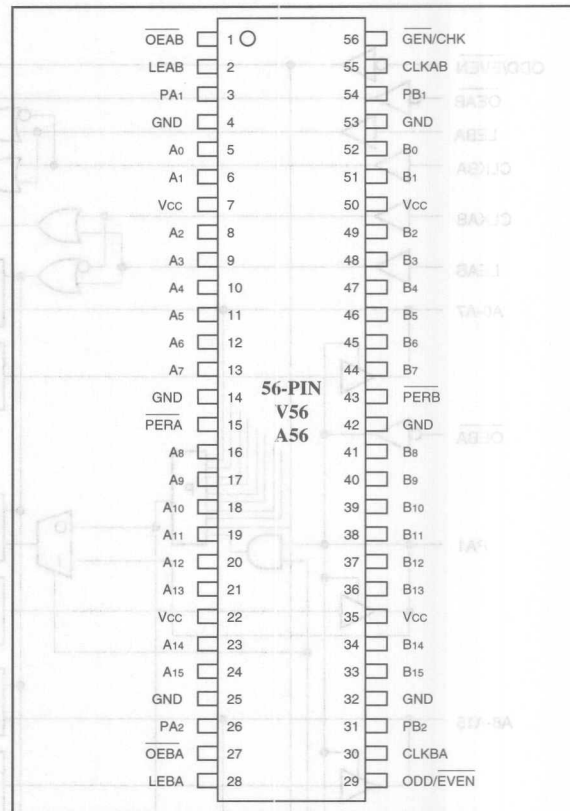
Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
PERA	Parity Error (Open Drain) on A Outputs
PERB	Parity Error (Open Drain) on B Outputs
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or B-to-A 3-State Outputs
ODD/EVEN ⁽¹⁾	Parity Mode Selection Input
GEN/CHK ⁽¹⁾	A-to-B Port Generate or Check Mode Input
PAX ⁽²⁾	A-to-B Parity Input, B-to-A Parity Output
PBx	B-to-A Parity Input, A-to-B Parity Output
GND	Ground
Vcc	Power

NOTES:

1. ODD/EVEN and GEN/CHK should be tied to Vcc or GND with no resistor for optimum results.
2. The PAX pin input is internally disabled during parity generation. This means that when generating parity in the A-to-B direction, there is no need to add a pull-up resistor to guarantee state. The pin will still function properly as the parity output for the B-to-A direction.

Product Pin Configuration



Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	5.5	8.0	pF
C _O	Open Drain Capacitance	V _{OUT} = 0V	4.5	6.0	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Truth Table^(1,2)

Inputs				Output Buffers
OEAB	LEAB	CLKAB	Ax	Bx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B ⁽³⁾
L	L	H	X	B ⁽⁴⁾

NOTES:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
Z = High Impedance
↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A flow control is the same, except using OEBA, LEBA, and CLKBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, assuming CLKAB was HIGH before LEAB went LOW.

3

Truth Table (Parity Generation) (1, 2, 3, 4, 5)

A0 - A7, Total Number of Inputs that are high	ODD/EVEN	PB1
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:

1. Conditions shown are for $\overline{\text{GEN}}/\text{CHK} = \text{L}$, $\overline{\text{OEAB}} = \text{L}$, $\overline{\text{OEBA}} = \text{H}$.
2. A-to-B parity generation is shown. B-to-A can check parity while A-to-B is performing generation. B-to-A will not generate parity.
3. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
4. Conditions shown are for the byte A0-A7. The byte A8-A15 is similar but will output the parity on PB2.
5. The error flag PERB will remain in a high state during parity generation.

Truth Table (Parity Checking) (1, 2, 3, 4)

A0 - A7 and PA1 ⁽⁵⁾ , Total Number of Inputs that are high	ODD/EVEN	PERB
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H ⁽⁶⁾
0, 2, 4, 6 or 8	L	H ⁽⁶⁾
0, 2, 4, 6 or 8	H	L

NOTES:

1. Conditions shown are for $\overline{\text{GEN}}/\text{CHK} = \text{H}$, $\overline{\text{OEAB}} = \text{L}$, $\overline{\text{OEBA}} = \text{H}$.
2. A-to-B parity checking is shown. B-to-A parity checking is same but uses $\overline{\text{OEBA}} = \text{L}$, $\overline{\text{OEAB}} = \text{H}$ and errors will be indicated on PERA.
3. In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors. (PB1 = PA1)
4. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
5. Conditions shown are for the byte A0-A7 and PA1. The byte A8-A15 and PA2 is same.
6. The parity error flag PERB is a combined flag for both bytes A0-A7 and A8-A15. If a parity error occurs on either byte PERB will go low.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	(Input pins) VCC = Max. V _{IN} = VCC			1	μA
		(I/O pins)			-1	
I _{IL}	Input LOW Current	(Input pins) VCC = Max. V _{IN} = GND			1	μA
		(I/O pins)			-1	
IOZH	High Impedance	VCC = Max. V _{OUT} = 2.7V			1	μA
IOZL	Output Current	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current (I/O pins)	VCC = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-225	mA
I _O	Output Drive Current (I/O pins)	VCC = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
I _{OFF}	Output Leakage Current (Open Drain)	VCC = Max., V _{OUT} = 4.5V			±100	μA
V _H	Input Hysteresis			100		mV

PI74FCT16511T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -3.0 mA	2.5	3.5		V
		I _{OH} = -15.0 mA	2.4	3.5		
		I _{OH} = -32.0 mA	2.0	3.0		
VOL	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	VCC = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162511T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -24.0 mA	2.4	3.3		V
VOL	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
ICCL, ICCH, ICCZ	Quiescent Power Supply Current	VCC = Max.		0.1	10	μA
ΔICC	Supply Current per Input @ TTL HIGH	VCC = Max.		0.5	1.5	mA
ICCD	Supply Current per Input per MHz ⁽⁴⁾	VCC = Max., Outputs Open OEAB = GND OEBA = VCC One Bit Toggling 50% Duty Cycle	VIN = VCC VIN = GND	75	120	μA/MHz
IC	Total Power Supply Current ⁽⁶⁾	VCC = Max., Outputs Open fCP = 10 MHz (CLKAB) 50% Duty Cycle LEAB = OEAB = GND OEBA = VCC fI = 5 MHz One Bit Toggling	VIN = VCC VIN = GND	0.8	2.7 ⁽⁵⁾	mA
			VIN = 3.4V VIN = GND	1.3	4.2 ⁽⁵⁾	
		VCC = Max., Outputs Open fCP = 10 MHz (CLKAB) 50% Duty Cycle LEAB = OEAB = GND OEBA = VCC fI = 2.5 MHz 18 Bits Toggling	VIN = VCC VIN = GND	3.8	7.5 ⁽⁵⁾	
			VIN = 3.4V VIN = GND	8.6	21.85 ⁽⁵⁾	

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Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
- IC = IQUIESCENT + IINPUTS + IDYNAMIC
IC = ICC + ΔICC DHNT + ICCD (fCP/2 + fINi)
ICC = Quiescent Current
ΔICC = Power Supply Current for a TTL High Input (VIN = 3.4V)
DH = Duty Cycle for TTL Inputs High
Nt = Number of TTL Inputs at DH
ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
fCP = Clock Frequency for Register Devices (Zero for Non-Register Devices)
fI = Input Frequency
Ni = Number of Inputs at fi
All currents are in milliamps and all frequencies are in megahertz.

16511T/162511T Switching Characteristics over Operating Range (Propagation Delays)

Parameters	Description	Conditions ⁽¹⁾	16511/162511T		16511/162511AT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	5.7	ns
tPHL	PAX to PBx						
tPLH	Propagation Delay		1.5	6.5	1.5	5.0	ns
tPHL	Ax to Bx or Bx to Ax, PBx to PAX						
tPLH	Propagation Delay		1.5	9.0	1.5	7.5	ns
tPHL	Ax to PBx						
tPLH ⁽³⁾	Propagation Delay		1.5	10.5	1.5	9.0	ns
tPHL	Ax to PERB, PAX to PERB		1.5	9.5	1.5	8.0	ns
tPLH ⁽³⁾	Propagation Delay		1.5	10.5	1.5	9.0	ns
tPHL	Bx to PERA, PBx to PERA		1.5	9.5	1.5	8.0	ns
tPLH	Propagation Delay		1.5	6.0	1.5	5.6	ns
tPHL	LEBA to Ax and PAX LEAB to Bx and PBx						
tPLH ⁽³⁾	Propagation Delay		1.5	7.5	1.5	7.0	ns
tPHL	LEBA to PERA, LEAB to PERB		1.5	6.5	1.5	6.0	ns
tPLH	Propagation Delay		1.5	6.0	1.5	5.6	ns
tPHL	CLKBA to Ax and PAX CLKAB to Bx and PBx						
tPLH ⁽³⁾	Propagation Delay		1.5	7.5	1.5	7.0	ns
tPHL	CLKBA to PERA CLKAB to PERB		1.5	6.5	1.5	6.0	ns
tFZH	Output Enable Time		1.5	7.0	1.5	6.0	ns
tFZL	OEBA to Ax and PAX OEAB to Bx and PBx						
tPHZ	Output Disable Time ⁽⁴⁾		1.5	7.0	1.5	5.6	ns
tPLZ	OEBA to Ax and PAX OEAB to Bx and PBx						
tPLZ ⁽³⁾	Parity ERROR Enable		1.5	6.0	1.5	6.0	ns
tFZL	OEBA to PERA, OEAB to PERB		1.5	6.0	1.5	6.0	ns
tPLH	ODD/EVEN to PERB		1.5	10.0	1.5	10.0	ns
tPHL			1.5	10.0	1.5	10.0	ns
tPLH	ODD/EVEN to PBx		1.5	10.0	1.5	10.0	ns
tPHL							

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. On Open Drain Outputs tPLH is measured up to $V_{OUT} = V_{OL} + 0.3V$.
4. This parameter is guaranteed but not production tested.

PI74FCT16511T/162511T Switching Characteristics over Operating Range (Setup Times)

Parameters	Description	Conditions ^(1,3)	16511/162511T		16511/162511AT		Unit				
			Com.		Com.						
			Min	Max	Min	Max					
tsu	Setup Time HIGH or LOW Ax to CLKAB	GEN/CHK LOW	PBx valid	CL = 50 pF RL = 500Ω	6.5	—	4	—	ns		
			PBx not valid		3	—	3	—	ns		
		GEN/CHK HIGH	PERB valid		6.5	—	4	—	ns		
			PERB not valid		3	—	3	—	ns		
tsu	Setup Time PAX to CLKAB	GEN/CHK HIGH	PERB valid		6.5	—	4	—	ns		
tsu	Setup Time Bx to CLKBA PBx to CLKBA	PERA valid	PERB not valid		3	—	3	—	ns		
			PERA not valid	6.5	—	4	—	ns			
		PERA not valid	3	—	3	—	ns				
tsu	Setup Time Ax to LEAB	CLKAB LOW	PBx valid		6.5	—	3.5	—	ns		
		GEN/CHK LOW	PBx not valid		3	—	3	—	ns		
		CLKAB LOW	PERB valid		6.5	—	3.5	—	ns		
		GEN/CHK HIGH	PERB not valid		3	—	3	—	ns		
		CLKAB HIGH	PBx valid		6.5	—	3.5	—	ns		
		GEN/CHK LOW	PBx not valid		3	—	3	—	ns		
		CLKAB HIGH	PERB valid		6.5	—	3.5	—	ns		
		GEN/CHK HIGH	PERB not valid		3	—	3	—	ns		
		tsu	Setup Time PAX to LEAB	CLKAB LOW	PERB valid		6.5	—	3.5	—	ns
				GEN/CHK HIGH	PERB not valid		3	—	3	—	ns
CLKAB HIGH	PERB valid				6.5	—	3.5	—	ns		
GEN/CHK HIGH	PERB not valid				3	—	3	—	ns		
tsu	Setup Time Bx to LEBA PBx to LEBA	CLKBA LOW	PERA valid		6.5	—	3.5	—	ns		
		PERA not valid		3	—	3	—	ns			
		CLKAB HIGH	PERA valid		6.5	—	3.5	—	ns		
		PERA not valid		3	—	3	—	ns			

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PI74FCT16511T/162511T Switching Characteristics over Operating Range (Hold Times)

Parameters	Description	Conditions ⁽¹⁾	16511/162511T		16511/162511AT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
th	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	CL = 50 pF RL = 500Ω	1	—	1	—	ns
th	Hold Time HIGH or LOW PAX to LEAB		1	—	1	—	ns
th	Hold Time HIGH or LOW PBx to LEBA		1	—	1	—	ns
th	Hold Time Ax to CLKAB, PAX to CLKAB		1	—	1	—	ns
th	Hold Time Bx to CLKBA, PBx to CLKBA		1	—	1	—	ns
tw	LEAB or LEBA Pulse Width HIGH ⁽²⁾		3	—	3	—	ns
tw	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽²⁾		3	—	3	—	ns

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not production tested.
- "Not valid" means the setup time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A-to-B or B-to-A port respective to the indicated direction.



PI74FCT16540T PI74FCT162540T

Fast CMOS 16-Bit Buffer/Line Drivers

Product Features:

Common Features:

- PI74FCT16500T and PI74FCT162500T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

PI74FCT16540T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162540T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

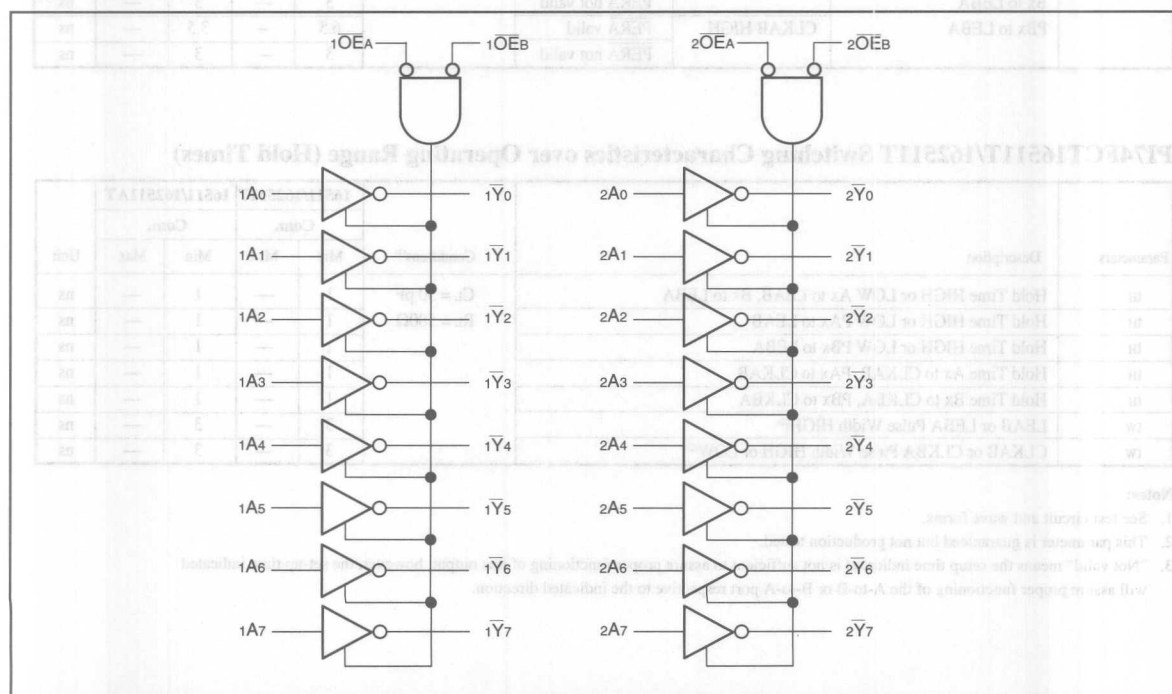
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16540T and PI74FCT162540T are inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. These devices are designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The PI74FCT16540T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162540T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs (Active LOW)
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	H
L	H	L
H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

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Product Pin Configuration

Pin		Pin	
1	10Ea	48	10Eb
2	1Y0	47	1A0
3	1Y1	46	1A1
4	GND	45	GND
5	1Y2	44	1A2
6	1Y3	43	1A3
7	Vcc	42	Vcc
8	1Y4	41	1A4
9	1Y5	40	1A5
10	GND	39	GND
11	1Y6	38	1A6
12	1Y7	37	1A7
13	2Y0	36	2A0
14	2Y1	35	2A1
15	GND	34	GND
16	2Y2	33	2A2
17	2Y3	32	2A3
18	Vcc	31	Vcc
19	2Y4	30	2A4
20	2Y5	29	2A5
21	GND	28	GND
22	2Y6	27	2A6
23	2Y7	26	2A7
24	20Ea	25	20Eb

Parameter	Description	Test Conditions	Typ	Max	Units
C _{in}	Input Capacitance	V _{in} = 0V	4.2	6	pF
C _{out}	Output Capacitance	V _{out} = 0V	2.2	8	pF

- Notes:
- For conditions show as Max. or Min., use appropriate values specified under Electrical Characteristics for the applicable device type.
 - Typical values are at V_{cc} = 5.0V, +35°C ambient and maximum loading.
 - Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
 - This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	VCC = Max., V _{IN} = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max., V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	VCC = Max., V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	VCC = Max., V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16540T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} , I _{OH} = -3.0 mA	2.5	3.5		V
		I _{OH} = -15.0 mA	2.4	3.5		
		I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} , I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	VCC = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162540T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} , I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} , I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		60	100	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		0.6	1.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		0.9	2.3 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} V _{IN} = GND		2.4	4.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.4	16.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- $I_c = I_{cc} + \Delta I_{cc} D_H N_t + I_{ccd} (f_{cp}/2 + f_i N_i)$
 I_{cc} = Quiescent Current
 ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_t = Number of TTL Inputs at D_H
 I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16540T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	16540T		16540AT		16540CT		16540DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	8.5	1.5	4.8	1.5	4.3	1.5	3.6	ns
tPHL	xAX to xYx										
tPZH	Output Enable Time		1.5	10.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tPZL	xOEx to xYx										
tpHZ	Output Disable Time ⁽³⁾		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.3	ns
tPLZ	xOEx to xYx										
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162540T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162540T		162540AT		162540CT		162540DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay xAX to xYx	CL = 50 pF RL = 500Ω	1.5	8.5	1.5	4.8	1.5	4.3	1.5	3.6	ns
tPHL	xAX to xYx										
tPZH	Output Enable Time xOEx to xYx		1.5	10.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
tPZL	xOEx to xYx										
tpHZ	Output Disable Time ⁽³⁾ xOEx to xYx		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.3	ns
tPLZ	xOEx to xYx										
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74FCT16541T
PI74FCT162541T

Fast CMOS 16-Bit Octal Buffer/Line Drivers

Product Features:

Common Features:

- PI74FCT16541T and PI74FCT162541T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

PI74FCT16541T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162541T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

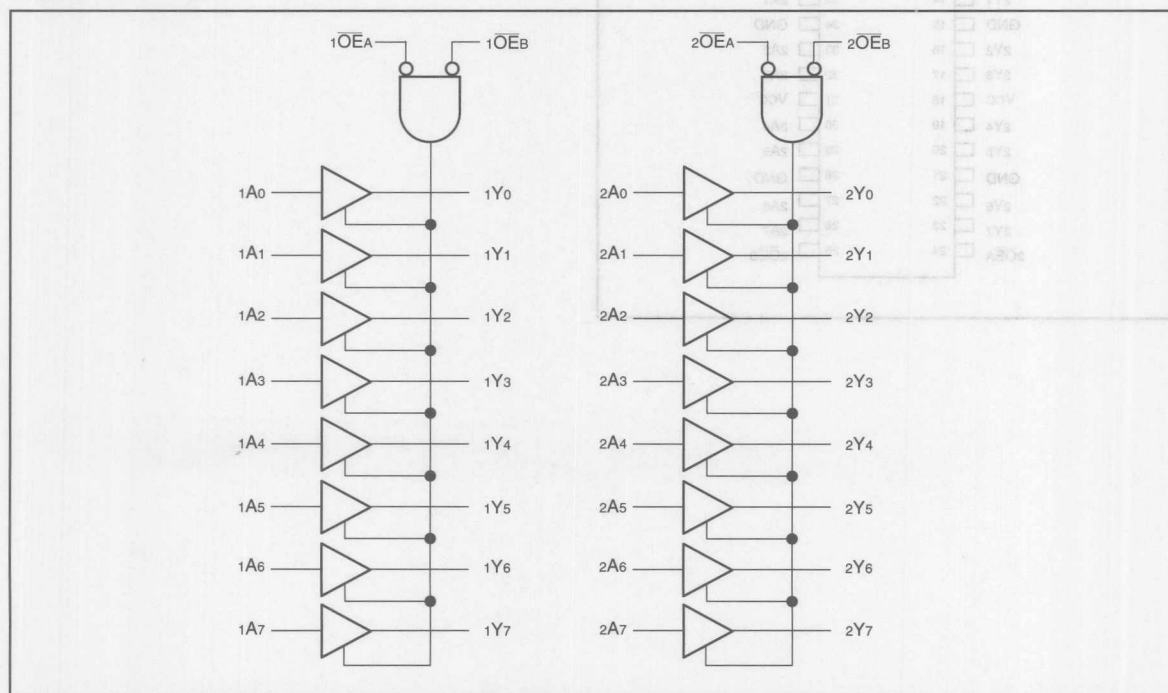
The PI74FCT16541T and PI74FCT162541T are non-inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. These devices are designed with three-state controls to operate in a Dual-Byte, or a single 16-bit word mode.

The PI74FCT16541T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162541T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

3

Logic Block Diagram



Product Pin Description

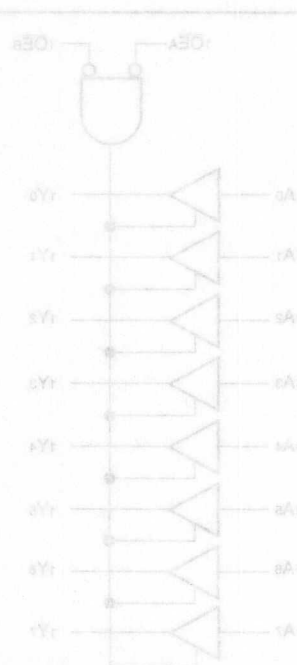
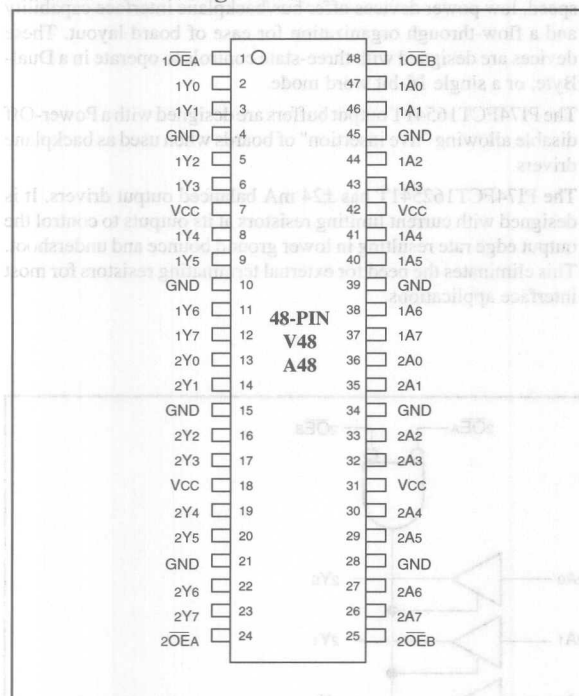
Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	H
L	H	L
H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max. V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max. V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{CC} = Max. V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16541T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -3.0 mA	2.5	3.5		V
				3.5		
			2.4	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162541T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max., V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max., V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle		60	100	μA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND		0.6	1.5 ⁽⁵⁾	mA
		One Bit Toggling	V _{IN} = 3.4V V _{IN} = GND	0.9	2.3 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND	V _{IN} = V _{cc} V _{IN} = GND	2.4	4.5 ⁽⁵⁾	
		16 Bits Toggling	V _{IN} = 3.4V V _{IN} = GND	6.4	16.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

$$I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_c = I_{\text{cc}} + \Delta I_{\text{cc}} D_H N_t + I_{\text{ccD}} (f_{\text{cp}}/2 + f_i N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_t = Number of TTL Inputs at D_H

I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16541T Switching Characteristics over Operating Range

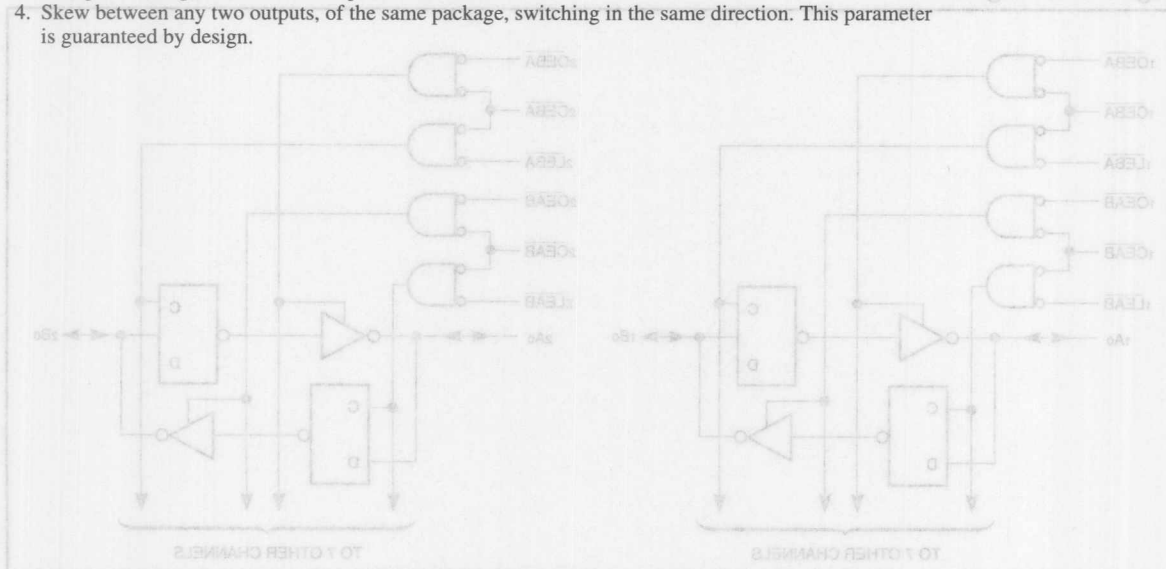
Parameters	Description	Conditions ⁽¹⁾	16541T		16541AT		16541CT		16541DT		Unit
			Com.	Com.	Com.	Com.	Com.	Com.	Com.	Com.	
1PLH 1PHL	Propagation Delay xAX to xYx	CL = 50 pF RL = 500Ω	1.5	8.5	1.5	4.8	1.5	4.3	1.5	3.6	ns
1PZH 1PZL	Output Enable Time xOEx to xYx		1.5	10.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
1PHZ 1PLZ	Output Disable Time ⁽³⁾ xOEx to xYx		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.3	ns
1SK(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162541T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162541T		162541AT		162541CT		162541DT		Unit
			Com.	Com.	Com.	Com.	Com.	Com.	Com.	Com.	
1PLH 1PHL	Propagation Delay xAX to xYx	CL = 50 pF RL = 500Ω	1.5	8.5	1.5	4.8	1.5	4.3	1.5	3.6	ns
1PZH 1PZL	Output Enable Time xOEx to xYx		1.5	10.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
1PHZ 1PLZ	Output Disable Time ⁽³⁾ xOEx to xYx		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.3	ns
1SK(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter guaranteed but not production tested
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



[illegible]

01/15/95

Product Pin Description

Pin Name	Description
xOEAB	A-to-B Output Enable Input (Active LOW)
xOEBA	B-to-A Output Enable Input (Active LOW)
xCEAB	A-to-B Enable Input (Active LOW)
xCEBA	B-to-A Enable Input (Active LOW)
xLEAB	A-to-B Latch Enable Input (Active LOW)
xLEBA	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or B-to-A 3-State Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs			Latch Status	Output Buffers
xCEAB	xLEAB	xOEAB	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES:

- *Before xLEAB LOW-to-HIGH Transistion
H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
Z = High Impedance
- A-to-B data flow shown. B-to-A flow control is the same, except using xCEBA, xLEBA, and xOEBA.

Product Pin Configuration

10EAB	1	56	10EBA
1LEAB	2	55	1LEBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A0	5	52	1B0
1A1	6	51	1B1
VCC	7	50	VCC
1A2	8	49	1B2
1A3	9	48	1B3
1A4	10	47	1B4
GND	11	46	GND
1A5	12	45	1B5
1A6	13	44	1B6
1A7	14	43	1B7
2A0	15	42	2B0
2A1	16	41	2B1
2A2	17	40	2B2
GND	18	39	GND
2A3	19	38	2B3
2A4	20	37	2B4
2A5	21	36	2B5
VCC	22	35	VCC
2A6	23	34	2B6
2A7	24	33	2B7
GND	25	32	GND
2CEAB	26	31	2CEBA
2LEAB	27	30	2LEBA
2OEAB	28	29	2OEBA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$	$V_{IN} = \text{GND}$			-1	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$	$V_{OUT} = 2.7\text{V}$			1	μA
I_{OZL}	Output Current	$V_{CC} = \text{Max.}$	$V_{OUT} = 0.5\text{V}$			-1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{ mA}$			-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}$, $V_{OUT} = \text{GND}$		-80	-140	-200	mA
I_O	Output Drive Current	$V_{CC} = \text{Max.}^{(3)}$, $V_{OUT} = 2.5\text{V}$		-50		-180	mA
V_H	Input Hysteresis				100		mV

PI74FCT16543T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3.0\text{ mA}$	2.5	3.5		V
			$I_{OH} = -15.0\text{ mA}$	2.4	3.5		
			$I_{OH} = -32.0\text{ mA}$	2.0	3.0		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 64\text{ mA}$		0.2	0.55	V
I_{OFF}	Power Down Disable	$V_{CC} = 0\text{V}$, V_{IN} or $V_{OUT} \leq 4.5\text{V}$		—	—	± 100	μA

PI74FCT162543T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -24.0\text{ mA}$	2.4	3.3		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24\text{ mA}$		0.3	0.55	V
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$		60	115	150	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-150	mA

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xCEAB & xOEAB = GND xCEBA = V _{cc} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		60	100	μA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xLEAB, xCEAB, and xOEAB = GND xCEBA = V _{cc} One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		0.7	2.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		0.9	3.3 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xLEAB, xCEAB, and xOEAB = GND xCEBA = V _{cc} 16 Bits Toggling	V _{IN} = V _{cc} V _{IN} = GND		2.5	5.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.5	17.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_t + I_{ccd} (f_{cp}/2 + f_i N_i)$$

I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_t = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16543T Switching Characteristics over Operating Range

PI74FCT16543T Switching Characteristics over Operating Range												Preliminary	
		Conditions ⁽¹⁾	16543T		16543AT		16543CT		16543DT		16543ET		Unit
Parameters	Description		Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
tPHL	Transparent Mode xAx to xBx or xBx to xAx												
tPLH	Propagation Delay		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
tPHL	xLEBA to xAx, xLEAB to xBx												
tpZH	Output Enable Time		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
tpZL	xOEBA or xOEAB to xAx or xBx												
tpHZ	Output Disable Time ⁽³⁾		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
tpLZ	xOEBA or xOEAB to xAx or xBx												
tsu	Setup Time HIGH or LOW xAx or xBx to xLEAB or xLEBA	C _L = 50 pF R _L = 500Ω	3.0	—	2.0	—	2.0	—	2.0	—	1.0	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tw	xLEAB or xLEBA Pulse Width LOW ⁽³⁾		5.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162543T Switching Characteristics over Operating Range

P174FCT162543T Switching Characteristics over Operating Range												Preliminary		
Parameters		Description	Conditions ⁽¹⁾	162543T		162543AT		162543CT		162543DT		162543ET		Unit
				Com.		Com.		Com.		Com.		Com.		
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	ns	
tPHL	Transparent Mode xAx to xBx or xBx to xAx		2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4		
tPLH	Propagation Delay		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7		
tPHL	xLEBA to xAx, xLEAB to xBx		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7		
tpZH	Output Enable Time		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8		
tpZL	xOEBA or xOEAB to xAx or xBx		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8		
tpHZ	Output Disable Time ⁽³⁾		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0		
tpLZ	xOEBA or xOEAB to xAx or xBx		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0		
tsu	Setup Time HIGH or LOW xAx or xBx to xLEAB or xLEBA	CL = 50 pF RL = 500Ω	3.0	—	2.0	—	2.0	—	2.0	—	1.0	—	ns	
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—		
tw	xLEAB or xLEBA Pulse Width LOW ⁽³⁾		5.0	—	5.0	—	5.0	—	3.0	—	3.0	—		
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5		

Notes:

- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74FCT16646T
PI74FCT162646T

Fast CMOS 16-Bit Registered Transceivers

Product Features:

Common Features:

- PI74FCT16646T and PI74FCT162646T high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

PI74FCT16646T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162646T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

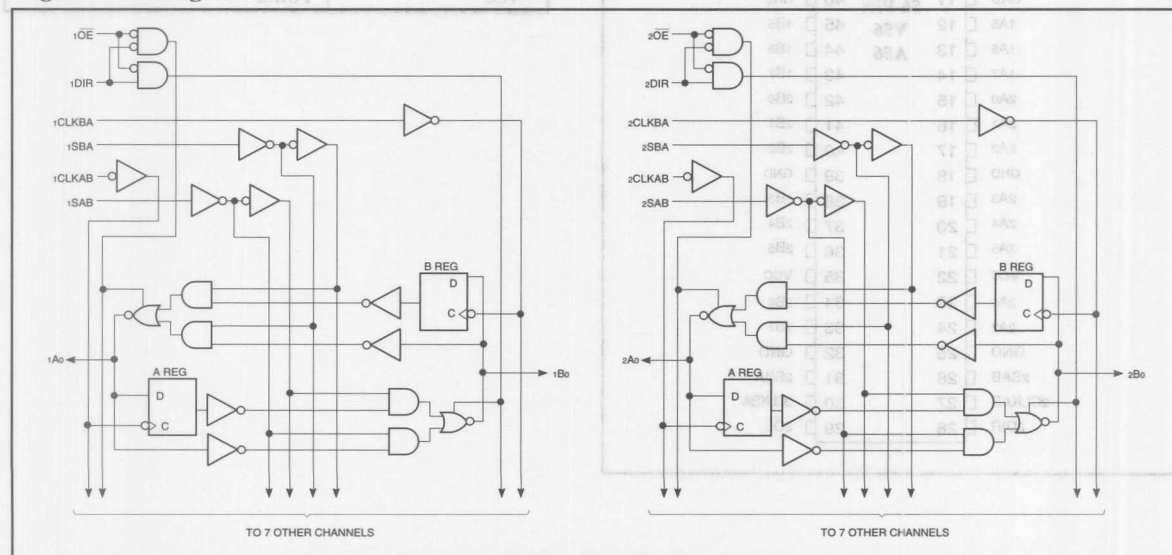
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Logic Block Diagram

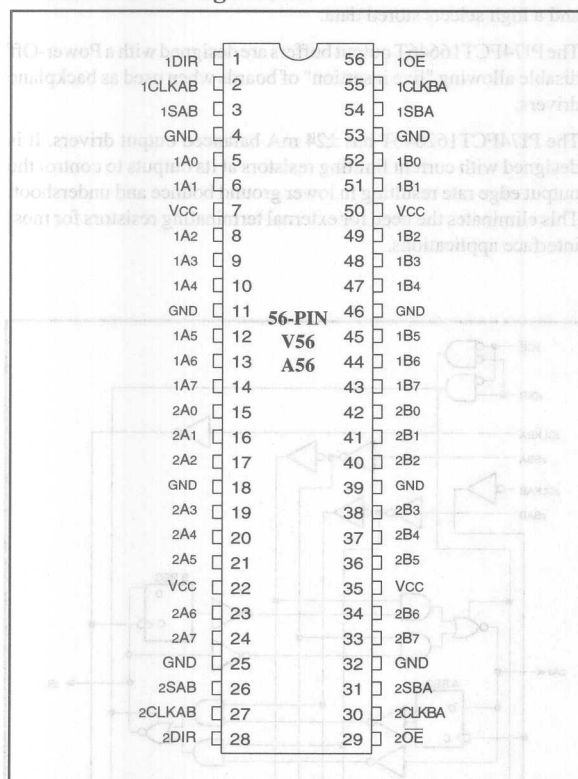


Truth Table

Function/Operation	Inputs						DATA I/O ⁽²⁾	
	x \overline{OE}	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

- The data output functions may be enabled or disabled by various signals at the x \overline{OE} or xDIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.
H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition

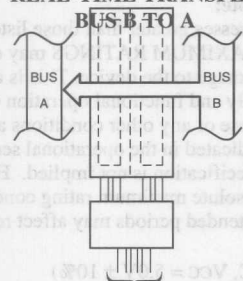
Product Pin Configuration



Product Pin Description

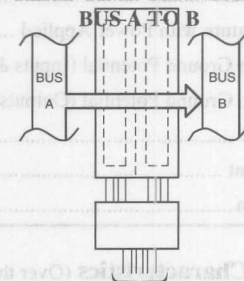
Pin Name	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
xDIR, x \overline{OE}	Output Enable Inputs
GND	Ground
Vcc	Power

REAL-TIME TRANSFER



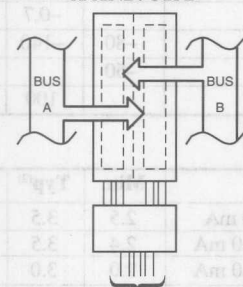
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER



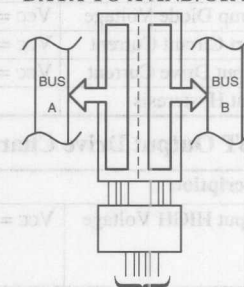
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

STORAGE FROM A AND/OR B



xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

TRANSFER STORES DATA TO A AND/OR B



xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Parameter ¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{in}	Input Capacitance	V _{in} = 0V	4.5	6	pF
C _{out}	Output Capacitance	V _{out} = 0V	3.5	8	pF

- Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical values are at V_{CC} = 3.0V, +25°C ambient and maximum loading.
 3. Not more than one output should be enabled at one time. Duration of the test should not exceed one second.
 4. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	VCC = Max.	V _{IN} = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	VCC = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	VCC = Max.	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , V _{OUT} = GND		-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max. ⁽³⁾ , V _{OUT} = 2.5V		-50		-180	mA
V _H	Input Hysteresis				100		mV

PI74FCT16646T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5		
			I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	VCC = 0V, V _{IN} or V _{OUT} ≤ 4.5V		—	—	±100	μA

PI74FCT162646T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.12	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xDIR = xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		75	120	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{cp} = 10 MHz (xCLKBA) 50% Duty Cycle xDIR = xOE = GND One Bit Toggling fi = 5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.8	2.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	4.2 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{cp} = 10 MHz (xCLKBA) 50% Duty Cycle xDIR = xOE = GND 16 Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		3.8	7.5 ⁽⁵⁾	
			V _{IN} = 3.4 V _{IN} = GND		8.3	21.0 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} \cdot D_{HN} \cdot N_t + I_{ccd} (f_{cp}/2 + f_i \cdot N_i)$
I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_t = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16646 Switching Characteristics over Operating Range

PI74FCT16646 Switching Characteristics over Operating Range											Preliminary		
Parameters	Description	Conditions ⁽¹⁾	16646T		16646AT		16646CT		16646DT		16646ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	C _L = 50 pF R _L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tPHL	Bus to Bus												
tpZH	Output Enable Time		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tpZL	xDIR or xOE to Bus												
tpHZ	Output Disable Time ⁽³⁾		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLZ	xDIR or xOE to Bus												
tPLH	Propagation Delay		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPHL	Clock to Bus												
tPLH	Propagation Delay		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tPHL	xSBA or xSAB to Bus												
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162646 Switching Characteristics over Operating Range

PI74FCT162646 Switching Characteristics over Operating Range												Preliminary	
Parameters	Description	Conditions ⁽¹⁾	162646T		162646AT		162646CT		162646DT		162646ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tPHL	Bus to Bus												
tpZH	Output Enable Time		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tpZL	xDIR or xOE to Bus												
tpHZ	Output Disable Time ⁽³⁾		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLZ	xDIR or xOE to Bus												
tPLH	Propagation Delay		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPHL	Clock to Bus												
tPLH	Propagation Delay		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tPHL	xSBA or xSAB to Bus												
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
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- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

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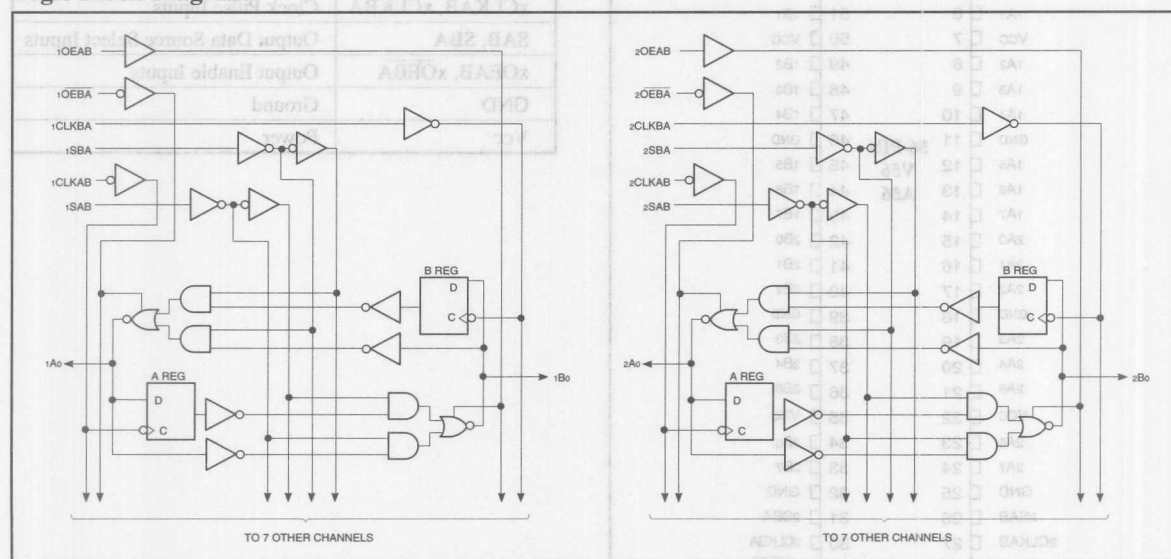
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Logic Block Diagram



Truth Table

Function/Operation	Inputs						DATA I/O ⁽²⁾	
	xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾
Store A in Both Registers	H	H	↑	↑	X ⁽²⁾	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified ⁽¹⁾	Input
Store B in Both Registers	L	L	↑	↑	X	X ⁽²⁾	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

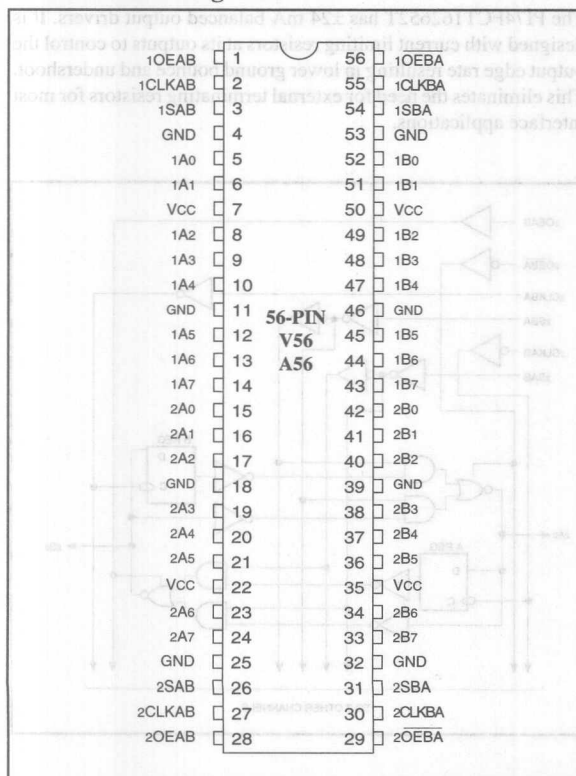
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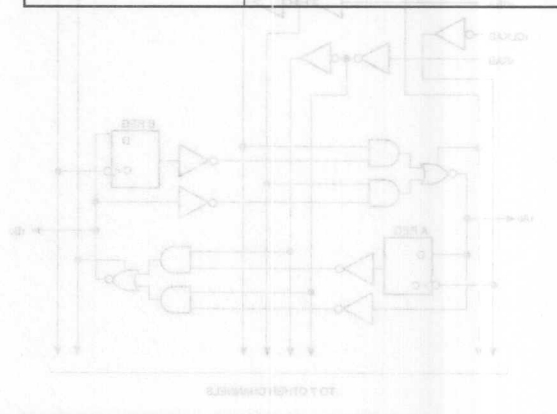
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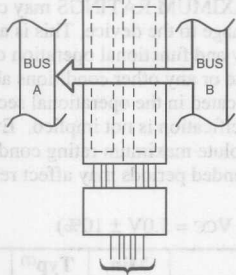
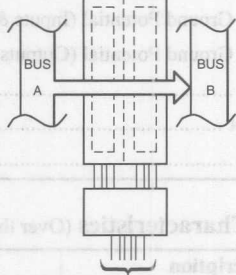
Product Pin Configuration

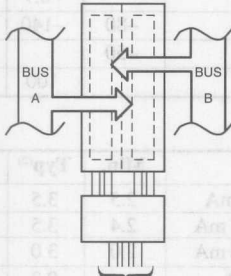
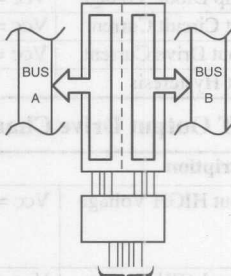


Product Pin Description

Pin Name	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
xOEAB, xOEBA	Output Enable Inputs
GND	Ground
Vcc	Power



<p>REAL-TIME TRANSFER BUS B TO A</p> 						<p>REAL-TIME TRANSFER BUS A TO B</p> 					
xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L	H	H	X	X	L	X

<p>STORAGE FROM A AND/OR B</p> 						<p>TRANSFER STORES DATA TO A AND/OR B</p> 					
xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X	H	L	H or L	H or L	H	H
L	X	X	↑	X	X	L	X	X	X	X	X
L	H	↑	↑	X	X	L	H	X	X	X	X

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max. VIN = GND			-1	μA
I _{OZH}	High Impedance	VCC = Max. VOUT = 2.7V			1	μA
I _{OZL}	Output Current	VCC = Max. VOUT = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max. ⁽³⁾ , VOUT = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16652T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., VIN = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5	V
			I _{OH} = -15.0 mA	2.4	3.5	
			I _{OH} = -32.0 mA	2.0	3.0	
V _{OL}	Output LOW Voltage	VCC = Min., VIN = V _{IH} or V _{IL}	I _{OL} = 64 mA	0.2	0.55	V
I _{OFF}	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA

PI74FCT162652T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., VIN = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3	V
V _{OL}	Output LOW Voltage	VCC = Min., VIN = V _{IH} or V _{IL}	I _{OL} = 24 mA	0.3	0.55	V
I _{ODL}	Output LOW Current	VCC = 5V, VIN = V _{IH} or V _{IL} , VOUT = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	VCC = 5V, VIN = V _{IH} or V _{IL} , VOUT = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	VIN = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	VOUT = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open xOEAB = xOEBA = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xOEAB = xOEBA = GND One Bit Toggling fi = 5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.8	2.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	4.2 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xOEAB = xOEBA = GND 16 Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	7.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		8.3	21.0 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_I + I_{CCD} (f_{CP}/2 + f_i N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_I = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_I = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16652 Switching Characteristics over Operating Range

PI74FCT16652 Switching Characteristics over Operating Range											Preliminary		
Parameters	Description	Conditions ⁽¹⁾	16652T		16652AT		16652CT		16652DT		16652ET		Unit
			Com.	Com.	Com.	Com.	Com.	Com.	Com.				
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tPHL	Bus to Bus												
tPZH	Output Enable Time		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tPZL	xOEAB or x OEBA to Bus												
tpHZ	Output Disable Time ⁽³⁾		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLZ	xOEAB or x OEBA to Bus												
tPLH	Propagation Delay		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPHL	Clock to Bus												
tPLH	Propagation Delay		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tPHL	xSBA or xSAB to Bus												
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162652 Switching Characteristics over Operating Range

PI74FCT162652 Switching Characteristics over Operating Range											Preliminary		
Parameters	Description	Conditions ⁽¹⁾	162652T		162652AT		162652CT		162652DT		162652ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tPHL	Bus to Bus												
tPZH	Output Enable Time		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tPZL	xOEAB or xOEBA to Bus												
tPHZ	Output Disable Time ⁽³⁾		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLZ	xOEAB or xOEBA to Bus												
tPLH	Propagation Delay		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPHL	Clock to Bus												
tPLH	Propagation Delay		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tPHL	xSBA or xSAB to Bus												
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74FCT16823T **PI74FCT162823T**

Fast CMOS **18-Bit Registers**

Product Features:

Common Features:

- PI74FCT16823T and PI74FCT162823T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide palstic SSOP (V56)

PI74FCT16823T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162823T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

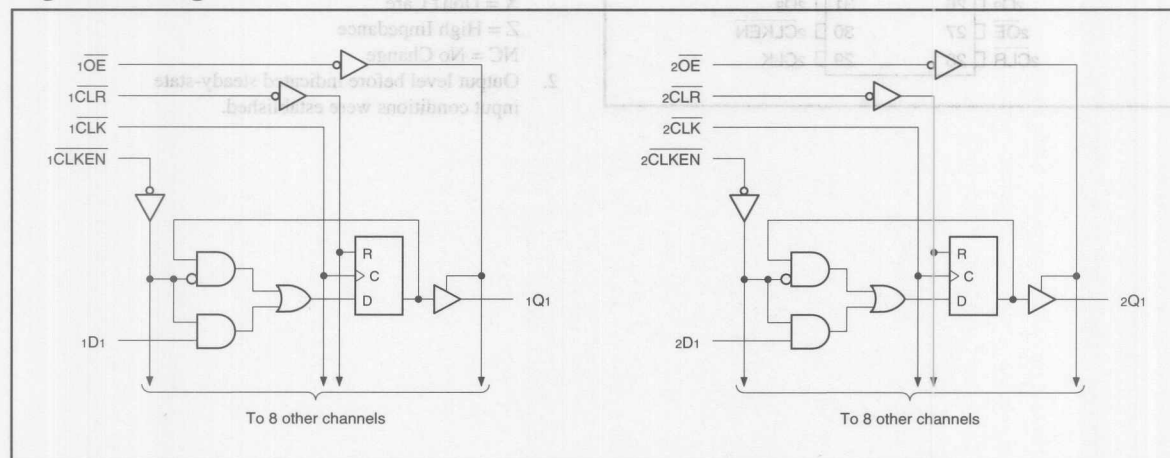
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16823T and PI74FCT162823T are 18-bit wide registers with clock enable (xCLKEN) and clear (xCLR) controls that make these devices especially suitable for parity bus interfacing in high-performance systems. The devices can be operated as two 9-bit registers or one 18-bit register using the control inputs. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The output buffers on PI74FCT16823T and PI74FCT162823T are especially designed for driving high-capacitance loads and low impedance backplanes and include a Power-Off Disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The PI74FCT162823T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Configuration

1CLR	1	56	1CLK
1OE	2	55	1CLKEN
1Q1	3	54	1D1
GND	4	53	GND
1Q2	5	52	1D2
1Q3	6	51	1D3
Vcc	7	50	Vcc
1Q4	8	49	1D4
1Q5	9	48	1D5
1Q6	10	47	1D6
GND	11	46	GND
1Q7	12	45	1D7
1Q8	13	44	1D8
1Q9	14	43	1D9
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
Vcc	22	35	Vcc
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2OE	27	30	2CLKEN
2CLR	28	29	2CLK

Product Pin Description

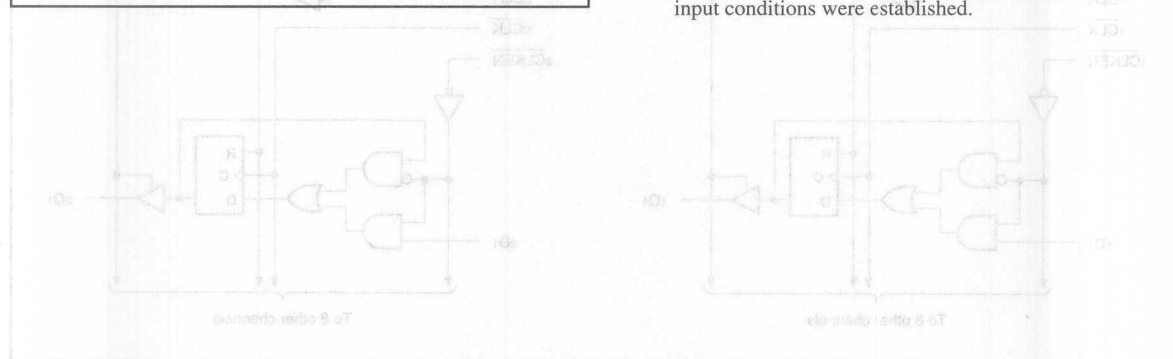
Pin Name	Description
xDx	Data Inputs
xCLK	Clock Inputs
xCLKEN	Clock Enable Inputs (Active LOW)
xCLR	Asynchronous Clear Inputs (Active LOW)
xOE	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

PI74FCT16823 Truth Table(1)

Function	Inputs					Outputs
	xOE	xCLR	xCLKEN	xCLK	xDx	xQx
High-Z	H	X	X	X	X	Z
Clear	L	L	X	X	X	L
Hold	L	H	H	X	X	Q ⁽²⁾
Load	H	H	L	↑	L	Z
	H	H	L	↑	H	Z
	L	H	L	↑	L	L
	L	H	L	↑	H	H

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change

- Output level before indicated steady-state input conditions were established.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max. VOUT = 2.7V			1	μA
IOZL	Output Current	VCC = Max. VOUT = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max. ⁽³⁾ , VOUT = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16823T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -3.0 mA	2.5	3.5		V
		IOH = -15.0 mA	2.4	3.5		
		IOH = -32.0 mA	2.0	3.0		
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.2	0.55	V
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA

PI74FCT162823T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -24.0 mA	2.4	3.3		V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL IOL = 24 mA		0.3	0.55	V
IODL	Output LOW Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V ⁽³⁾	60	115	150	mA
IODH	Output HIGH Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	VIN = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	VOUT = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max. V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max. V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = xCLKEN = GND One Input Toggling 50% Duty Cycle		75	120	μA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle xOE = xCLKEN = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND	0.8	2.7	mA
			V _{IN} = 3.4V V _{IN} = GND	1.3	4.2	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle xOE = xCLKEN = GND Eighteen Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND	4.2	8.1 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	9.2	23.1 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16823 Switching Characteristics over Operating Range

PI74FCT16823 Switching Characteristics over Operating Range										Preliminary				Unit
Parameters	Description	Conditions ⁽¹⁾	16823AT		16823BT		16823CT		16823DT		16823ET			
			Com.		Com.		Com.		Com.		Com.			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay xCLK to xQx	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns	
t _{PHL}		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns	
t _{PHL}	Propagation Delay xCLR to xQx	C _L = 50 pF R _L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns	
t _{PZH}	Output Enable Time xOE to xQx	C _L = 50 pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns	
t _{PZL}		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	9.0	1.5	9.0	ns	
t _{PHZ}	Output Disable Time ⁽³⁾ xOE to xQx	C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	1.5	3.6	ns	
t _{PLZ}		C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	3.6	ns	
t _{SU}	Setup Time HIGH or LOW, xDx to xCLK	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns	
t _H	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns	
t _{SU}	Setup Time HIGH or LOW, xCLKEN to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns	
t _H	Hold Time HIGH or LOW, xCLKEN to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns	
t _W	xCLK Pulse Width HIGH or LOW ⁽³⁾		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns	
t _W	xCLR Pulse Width LOW ⁽³⁾		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns	
t _{REM}	Recovery Time ⁽³⁾ xCLR to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns	
t _{sk(o)}	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162823 Switching Characteristics over Operating Range

P174FCT162823 Switching Characteristics over Operating Range										Preliminary				
				162823AT		162823BT		162823CT		162823DT		162823ET		Unit
				Com.		Com.		Com.		Com.		Com.		
Parameters	Description	Conditions ⁽¹⁾	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tpLH tpHL	Propagation Delay xCLK to xQx	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns	
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns	
tpHL	Propagation Delay xCLR to xQx	CL = 50 pF RL = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns	
tpZH tpZL	Output Enable Time xOE to xQx	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns	
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	9.0	1.5	9.0	ns	
tpHZ tpLZ	Output Disable Time ⁽³⁾ xOE to xQx	CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	1.5	3.6	ns	
		CL = 50 pF RL = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	3.6	ns	
tsu	Setup Time HIGH or LOW, xDx to xCLK	CL = 50 pF RL = 500Ω	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns	
th	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns	
tsu	Setup Time HIGH or LOW, xCLKEN to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns	
th	Hold Time HIGH or LOW, xCLKEN to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns	
tw	xCLK Pulse Width HIGH or LOW ⁽³⁾		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns	
tw	xCLR Pulse Width LOW ⁽³⁾		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns	
tREM	Recovery Time ⁽³⁾ xCLR to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns	
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74FCT16827T
PI74FCT162827T

Fast CMOS
20-Bit Buffers

Product Features:

Common Features:

- PI74FCT16827T and PI74FCT162827T are high-speed, low power devices with high current drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

PI74FCT16827T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162827T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

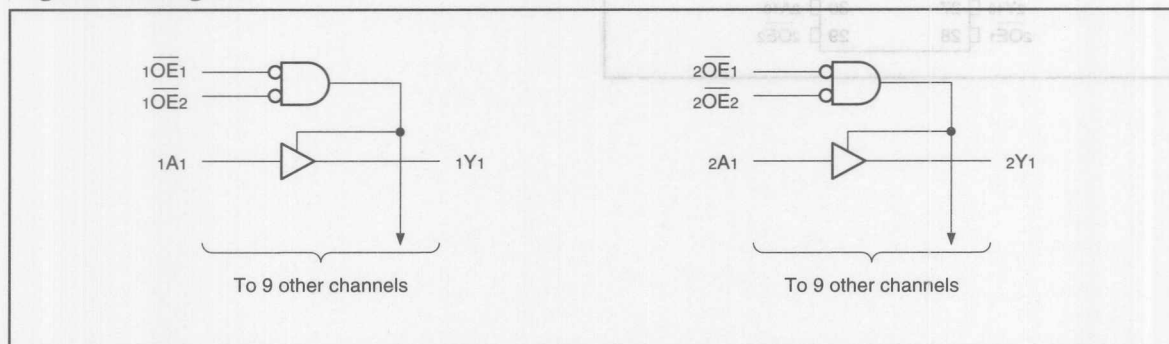
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16827T and PI74FCT162827T are 20-bit wide bus drivers designed to provide buffering and high-performance bus interfacing for wide data/address paths or busses with parity. Two pair of nanded output enable controls allow the devices to be operated as two 10-bit buffers or as one 20-bit buffer. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The output buffers on the PI74FCT16827T and PI74FCT162827T are especially designed for driving high-capacitance loads and low impedance backplanes and include a Power-Off Disable function allowing "live insertion" of boards when the devices are used as backplane drivers.

The PI74FCT162827T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Configuration

1OE1	1	56	1OE2
1Y1	2	55	1A1
1Y2	3	54	1A2
GND	4	53	GND
1Y3	5	52	1A3
1Y4	6	51	1A4
Vcc	7	50	Vcc
1Y5	8	49	1A5
1Y6	9	48	1A6
1Y7	10	47	1A7
GND	11	46	GND
1Y8	12	45	1A8
1Y9	13	44	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
GND	18	39	GND
2Y4	19	38	2A4
2Y5	20	37	2A5
2Y6	21	36	2A6
Vcc	22	35	Vcc
2Y7	23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9	26	31	2A9
2Y10	27	30	2A10
2OE1	28	29	2OE2

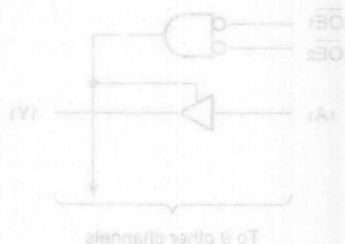
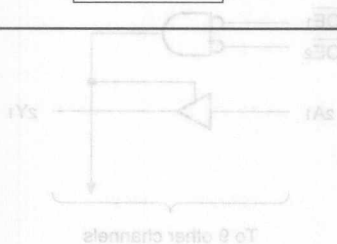
Product Pin Description

Pin Name	Description
xOE _x	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

Truth Table(1)

Inputs			Outputs
xOE ₁	xOE ₂	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max. V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max. V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{CC} = Max. V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16827T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}				
		I _{OH} = -3.0 mA	2.5	3.5		V
		I _{OH} = -15.0 mA	2.4	3.5		
		I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.2	0.55	V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162827T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}				
		I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE1 = OE2 = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{cp} = 10 MHz 50% Duty Cycle OE1 = OE2 = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{cp} = 10 MHz 50% Duty Cycle OE1 = OE2 = GND Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4 V _{IN} = GND		5.2	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_c = I_{cc} + ΔI_{cc} D_H N_t + I_{ccd} (f_{cp}/2 + fi N_i)
I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_t = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
fi = Input Frequency
N_i = Number of Inputs at fi
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16827 Switching Characteristics over Operating Range

PI74FCT16827 Switching Characteristics over Operating Range									Preliminary				
Parameters	Description	Conditions ⁽¹⁾	16827AT		16827BT		16827CT		16827DT		16827ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xAX to xYx	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.0	1.5	4.4	1.5	3.8	1.5	3.2	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	1.5	7.5	1.5	7.0	ns
tPZH tPZL	Output Enable Time xOEx to xYx	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	5.0	1.5	4.8	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	1.5	9.0	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OEN to YN	CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	9.0	1.5	6.0	1.5	5.7	1.5	4.3	1.5	4.0	ns
		CL = 50 pF RL = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	1.5	4.3	1.5	4.0	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

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PI74FCT162827 Switching Characteristics over Operating Range

PI74FCT162827 Switching Characteristics over Operating Range									Preliminary				
Parameters	Description	Conditions ⁽¹⁾	162827AT		162827BT		162827CT		162827DT		162827ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xAX to xYx	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.0	1.5	4.4	1.5	3.8	1.5	3.2	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	1.5	7.5	1.5	7.0	ns
tPZH tPZL	Output Enable Time xOEx to xYx	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	5.0	1.5	4.8	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	1.5	9.0	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ OEN to YN	CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	9.0	1.5	6.0	1.5	5.7	1.5	4.3	1.5	4.0	ns
		CL = 50 pF RL = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	1.5	4.3	1.5	4.0	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74FCT16841T PI74FCT162841T

Fast CMOS 20-Bit Transparent Latch

Product Features:

Common Features:

- PI74FCT16841T and PI74FCT162841T are high-speed, low power devices with high current drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

PI74FCT16841T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162841T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

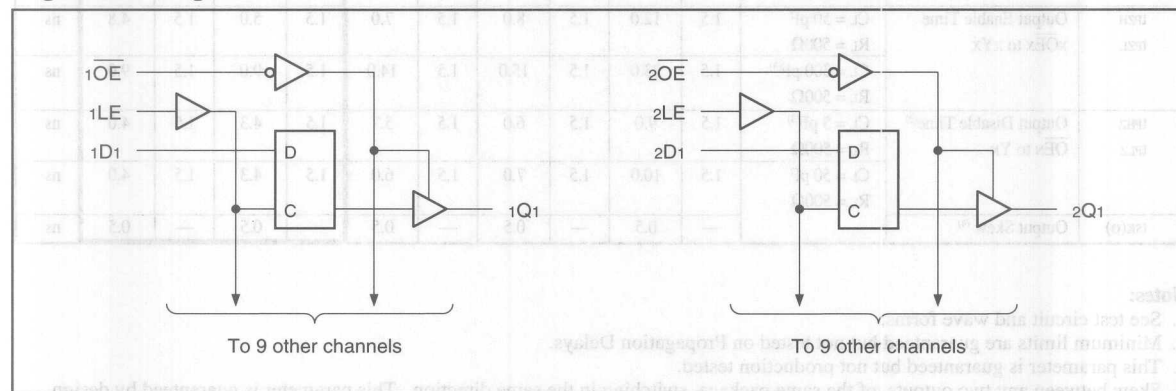
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16841T and PI74FCT162841T are 20-bit wide transparent latches designed to provide temporary storage of data and can be used as I/O ports, memory address latches, and bus drivers. The Output Enable and Latch Enable controls allow the devices to be operated as two 10-bit latches or one 20-bit latch. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The output buffers on the PI74FCT16841T and PI74FCT162841T are especially designed for driving high-capacitance loads and low impedance backplanes and include a Power-Off Disable function allowing "live insertion" of boards when the devices are used as backplane drivers.

The PI74FCT162841T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Configuration

1OE	1	56	1LE
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
Vcc	7	50	Vcc
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
Vcc	22	35	Vcc
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
2OE	28	29	2LE

Product Pin Description

Pin Name	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active LOW)
xOE	Output Enable Input (Active LOW)
xQx	3-State Outputs

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Truth Table(1)

Inputs			Outputs
xDx	xLE	xOE	xQx
H	H	L	H
L	H	L	L
X	L	L	Q ⁽²⁾
X	X	H	Z

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
- Output level before xLE HIGH-to-LOW Transition.

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IN} or V _I	2.4	2.5	2.7	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IN} or V _I	0.3	0.4	0.5	V
I _{OH}	Output HIGH Current	V _{CC} = 2V, V _{IN} = V _{IN} or V _I , V _{OUT} = 1.5V	60	115	150	mA
I _{OL}	Output LOW Current	V _{CC} = 2V, V _{IN} = V _{IN} or V _I , V _{OUT} = 1.5V	-50	-115	-150	mA

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
C _{in}	Input Capacitance	V _{IN} = 0V	4.5	5	6	pF
C _{out}	Output Capacitance	V _{OUT} = 0V	2.5	3	4	pF

- Notes:
- For conditions show as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
 - Typical values are at V_{CC} = 2.0V, +25°C ambient and maximum loading.
 - Not more than one output should be asserted at one time. Duration of the test should not exceed one second.
 - This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	VCC = Max.	V _{IN} = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	VCC = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	VCC = Max.	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , V _{OUT} = GND		-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max. ⁽³⁾ , V _{OUT} = 2.5V		-50		-180	mA
V _H	Input Hysteresis				100		mV

PI74FCT16841T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5		
			I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	VCC = 0V, V _{IN} or V _{OUT} ≤ 4.5V		—	—	±100	μA

PI74FCT162841T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE = GND; LE = V _{cc} One Input Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
		OE = GND; LE = V _{cc} fi = 5 MHz One Bit Toggling	V _{IN} = V _{cc} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.2	14.5 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND				
			V _{IN} = 3.4V V _{IN} = GND				
		OE = GND; LE = V _{cc} Eight Bits Toggling fi = 2.5 MHz 50% Duty Cycle					

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{CP}/2 + f_i N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16841 Switching Characteristics over Operating Range

PI74FCT16841 Switching Characteristics over Operating Range									Preliminary				Unit
Parameters	Description	Conditions ⁽¹⁾	16841AT		16841BT		16841CT		16841DT		16841ET		
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	C _L = 50 pF R _L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	1.5	4.2	1.5	3.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	13.0	1.5	13.0	1.5	13.0	1.5	13.0	1.5	7.5	ns
t _{PLH} t _{PHL}	Propagation Delay xLE to xQx	C _L = 50 pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	1.5	4.0	1.5	3.7	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	1.5	8.0	1.5	7.5	ns
t _{PZH} t _{PZL}	Output Enable Time xOE to xQx	C _L = 50 pF R _L = 500Ω	1.5	11.5	1.5	8.0	1.5	6.5	1.5	4.8	1.5	4.4	ns
		C _L = 300 pF ⁽⁴⁾ R _L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	1.5	9.0	1.5	9.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ xOE to xQx	C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	1.5	4.0	1.5	3.6	ns
		C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	1.5	5.4	1.5	3.6	ns
t _{SU}	Setup Time HIGH or LOW, xDx to xLE	C _L = 50 pF R _L = 500Ω	2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
t _H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
t _W	xLE Pulse Width HIGH ⁽³⁾		4.0	—	4.0	—	4.0	—	4.0	—	3.0	—	ns
t _{SK(o)}	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

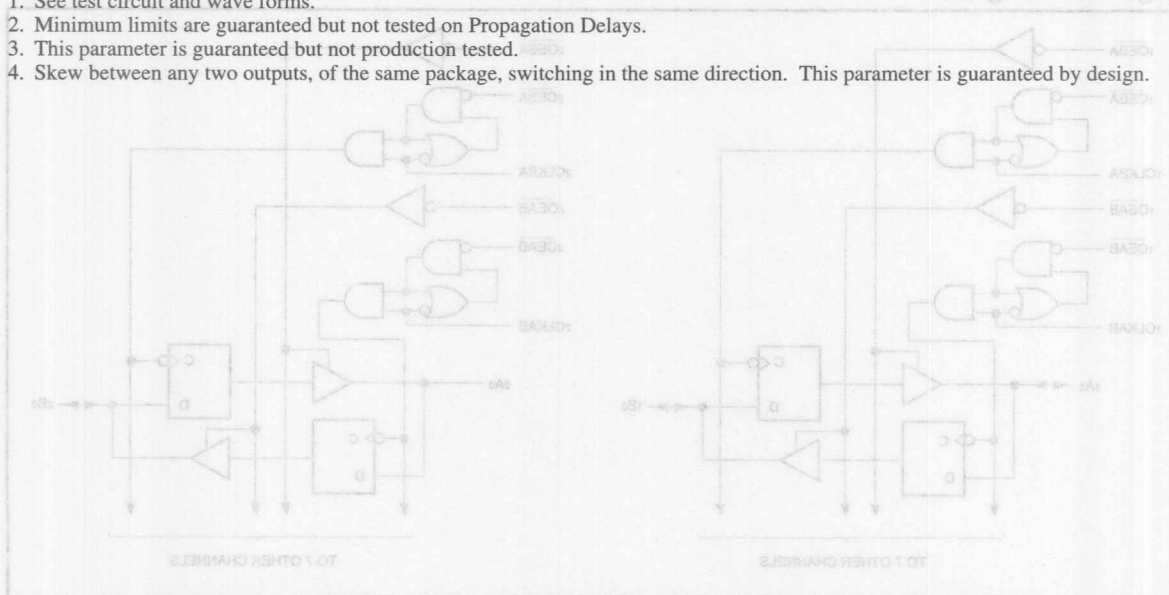
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT16841 Switching Characteristics over Operating Range

PI74FCT16841 Switching Characteristics over Operating Range									Preliminary				
Parameters	Description	Conditions ⁽¹⁾	162841AT		162841BT		162841CT		162841DT		162841ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF	1.5	9.0	1.5	6.5	1.5	5.5	1.5	4.2	1.5	3.4	ns
t _{PHL}	xDx to xQx	R _L = 500Ω											
	(LE = HIGH)	C _L = 300 pF ⁽³⁾	1.5	13.0	1.5	13.0	1.5	13.0	1.5	13.0	1.5	7.5	ns
		R _L = 500Ω											
t _{PLH}	Propagation Delay	C _L = 50 pF	1.5	12.0	1.5	8.0	1.5	6.4	1.5	4.0	1.5	3.7	ns
t _{PHL}	xLE to xQx	R _L = 500Ω											
		C _L = 300 pF ⁽³⁾	1.5	16.0	1.5	15.5	1.5	15.0	1.5	8.0	1.5	7.5	ns
		R _L = 500Ω											
t _{PZH}	Output Enable Time	C _L = 50 pF	1.5	11.5	1.5	8.0	1.5	6.5	1.5	4.8	1.5	4.4	ns
t _{PZL}	xOE to xQx	R _L = 500Ω											
		C _L = 300 pF ⁽⁴⁾	1.5	23.0	1.5	14.0	1.5	12.0	1.5	9.0	1.5	9.0	ns
		R _L = 500Ω											
t _{PHZ}	Output Disable Time ⁽³⁾	C _L = 5 pF ⁽³⁾	1.5	7.0	1.5	6.0	1.5	5.7	1.5	4.0	1.5	3.6	ns
t _{PLZ}	xOE to xQx	R _L = 500Ω											
		C _L = 50 pF	1.5	8.0	1.5	7.0	1.5	6.0	1.5	5.4	1.5	3.6	ns
		R _L = 500Ω											
t _{su}	Setup Time HIGH or LOW, xDx to xLE	C _L = 50 pF	2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
		R _L = 500Ω											
t _h	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
t _w	xLE Pulse Width HIGH ⁽³⁾		4.0	—	4.0	—	4.0	—	4.0	—	3.0	—	ns
t _{sk(o)}	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



Fast CMOS 16-Bit Registered Transceivers

Product Features:

Common Features:

- PI74FCT16952T and PI74FCT162952T are high-speed, low power devices with high current drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

PI74FCT16952T Features:

- High output drive: $I_{OH} = -32 \text{ mA}$; $I_{OL} = 64 \text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162952T Features:

- Balanced output drivers: $\pm 24 \text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

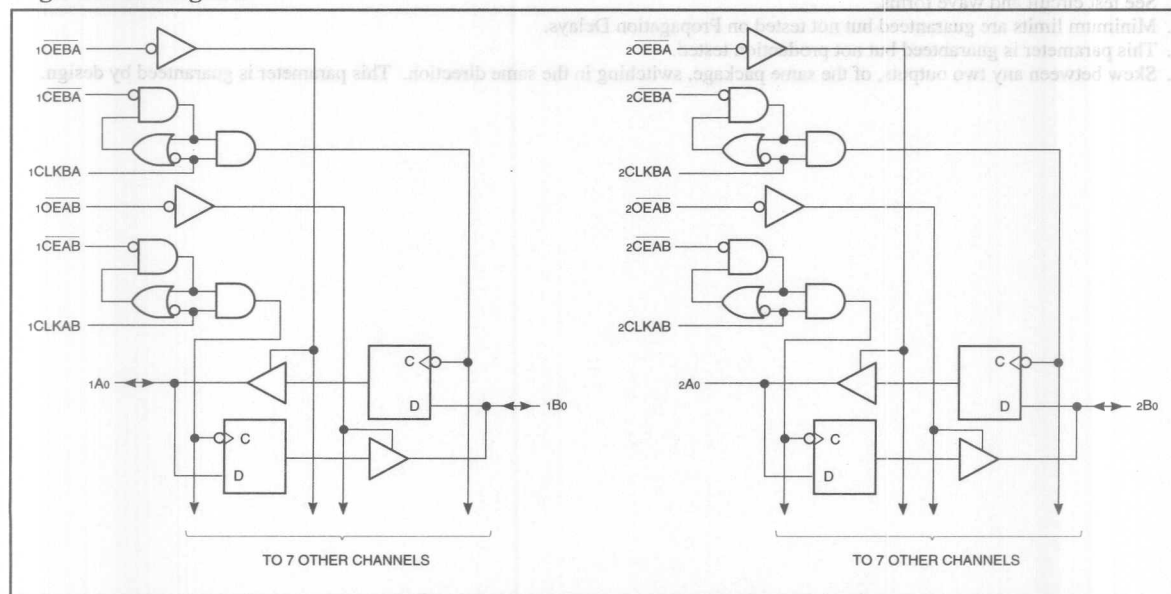
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16952T and PI74FCT162952T are 16-bit registered transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($x\overline{CEAB}$) input must be LOW in order to enter data from $x\overline{Ax}$. The data present on the A port will be clocked on the B register when $x\overline{CLKAB}$ toggles from LOW-to-HIGH. The $x\overline{OEAB}$ control performs the output enable function on the B port. Control of data from B to A is similar, but uses the $x\overline{CEBA}$, $x\overline{CLKBA}$, and $x\overline{OEBA}$ inputs. By connecting the control pins of the two independent transceivers together, a full 16-bit operation can be achieved. The output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT16952T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162952T has $\pm 24 \text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Pin Description

Pin Name	Description
xOEAB	A-to-B Output Enable Input (Active LOW)
xOEBA	B-to-A Output Enable Input (Active LOW)
xCEAB	A-to-B Clock Enable Input (Active LOW)
xCEBA	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or B-to-A 3-State Outputs
GND	Ground
Vcc	Power

Truth Table^(1,2)

Inputs				Outputs
xCEAB	xCLKAB	xOEAB	xAx	xBx
H	X	L	X	B ⁽³⁾
X	L	L	X	B ⁽³⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	High Z

3
NOTES:

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
↑ = LOW-to-HIGH Transition
Z = High Impedance
- A-to-B data flow shown. B-to-A flow control is the same, except using xCEBA, xCLKBA, and xOEBA.
- Level of B before the indicated steady-state input conditions were established.

Product Pin Configuration

10EAB	1	56	10EBA
1CLKAB	2	55	1CLKBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A0	5	52	1B0
1A1	6	51	1B1
VCC	7	50	VCC
1A2	8	49	1B2
1A3	9	48	1B3
1A4	10	47	1B4
GND	11	46	GND
1A5	12	45	1B5
1A6	13	44	1B6
1A7	14	43	1B7
2A0	15	42	2B0
2A1	16	41	2B1
2A2	17	40	2B2
GND	18	39	GND
2A3	19	38	2B3
2A4	20	37	2B4
2A5	21	36	2B5
VCC	22	35	VCC
2A6	23	34	2B6
2A7	24	33	2B7
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	VCC = Max., V _{IN} = VCC			1	μA
I _{IL}	Input LOW Current	VCC = Max., V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	VCC = Max., V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	VCC = Max., V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	VCC = Max. ⁽³⁾ , V _{OUT} = 2.5V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16952T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5	
			I _{OH} = -32.0 mA	2.0	3.0	
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	VCC = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162952T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	VCC = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open xOEAB or xOEBA = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		75	120	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 10 MHz (xCLKAB) 50% Duty Cycle xOEAB = xCEAB = GND xOEAB = V _{cc} One Bit Toggling fi = 5 MHz 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.8	1.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	3.2 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _{CP} = 10 MHz (xCLKAB) 50% Duty Cycle xOEAB = xCEAB = GND xOEBA = V _{cc} 16 Bits Toggling fi = 2.5 MHz 50% Duty cycle	V _{IN} = V _{cc} V _{IN} = GND		3.4	5.9 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		7.6	18.7 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{CP}/2 + f_i N_i)$
 I_{cc} = Quiescent Current
 ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16952T Switching Characteristics over Operating Range

PI74FCT16952T Switching Characteristics over Operating Range												Preliminary		
Parameters	Description	Conditions ⁽¹⁾	16952AT		16952BT		16952CT		16952DT		16952ET		Unit	
			Com.		Com.		Com.		Com.		Com.			
tPLH	Propagation Delay	CL = 50 pF RL = 500	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.4	1.5	3.7	ns	
tpHL	xCLKAB, xCLKBA to xBx, xAx													
tpZH	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns	
tpZL	xOEBA, xOEAB to xAx, xBx													
tpHZ	Output Disable Time ⁽³⁾		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	3.6	ns	
tPLZ	xOEBA, xOEAB to xAx, xBx													
tsu	Setup Time HIGH or LOW		2.5	—	2.5	—	2.5	—	2.0	—	1.5	—	ns	
	xAx, xBx to xCLKAB, xCLKBA													
th	Hold Time HIGH or LOW		2.0	—	2.0	—	1.5	—	1.0	—	0.0	—	ns	
	xAx, xBx to xCLKAB, xCLKBA													
tsu	Setup Time HIGH or LOW	CL = 50 pF RL = 500	3.0	—	3.0	—	3.0	—	2.0	—	2.0	—	ns	
	xCEAB, xCEBA to xCLKAB, xCLKBA													
th	Hold Time HIGH or LOW		2.0	—	2.0	—	2.0	—	1.5	—	0.0	—	ns	
	xCEAB, xCEBA to xCLKAB, xCLKBA													
tw	Pulse Width HIGH ⁽³⁾ or LOW, xCLKAB or xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns	

PI74FCT162952T Switching Characteristics over Operating Range

PI74FCT162952T Switching Characteristics over Operating Range											Preliminary		
Parameters	Description	Conditions ⁽¹⁾	162952AT		162952BT		162952CT		162952DT		162952ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.4	1.5	3.7	ns
tpHL	xCLKAB, xCLKBA to xBx, xAx												
tpZH	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
tpZL	xOEBA, xOEAB to xAx, xBx												
tpHZ	Output Disable Time ⁽³⁾		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	3.6	ns
tPLZ	xOEBA, xOEAB to xAx, xBx												
tsu	Setup Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.0	—	1.5	—	ns
th	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.0	—	0.0	—	ns
tsu	Setup Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	1.5	—	0.0	—	ns
tw	Pulse Width HIGH ⁽³⁾ or LOW, xCLKAB or xCLKBA	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	
tsk(o)	Output Skew ⁽⁴⁾	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

GENERAL INFORMATION**1****STANDARD AND 25Ω OUTPUT RESISTOR SERIES
5V FCT LOGIC PRODUCTS****2****DOUBLE DENSITY STANDARD
5V FCT LOGIC PRODUCTS****3****DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS****4****STANDARD 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****5****DOUBLE DENSITY 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****6****SPECIALTY LOGIC PRODUCTS****7****BUS SWITCH PRODUCTS****8****CLOCK DISTRIBUTION PRODUCTS****9****CLOCK GENERATOR PRODUCTS****10****NETWORKING PRODUCTS****11****APPLICATION NOTES****12****QUALITY AND RELIABILITY INFORMATION****13****PACKAGE MECHANICAL OUTLINES****14****SALES AND DISTRIBUTION LOCATIONS****15**

**DOUBLE DENSITY
3.3V FCT LOGIC PRODUCTS**

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PI74FCT163245	Fast CMOS 3.3V 16-Bit Bidirectional Transceivers	4.11
PI74FCT163373	Fast CMOS 3.3V 16-Bit Transparent Latches	4.16
PI74FCT163374	Fast CMOS 3.3V 16-Bit Registers (3-State)	4.21

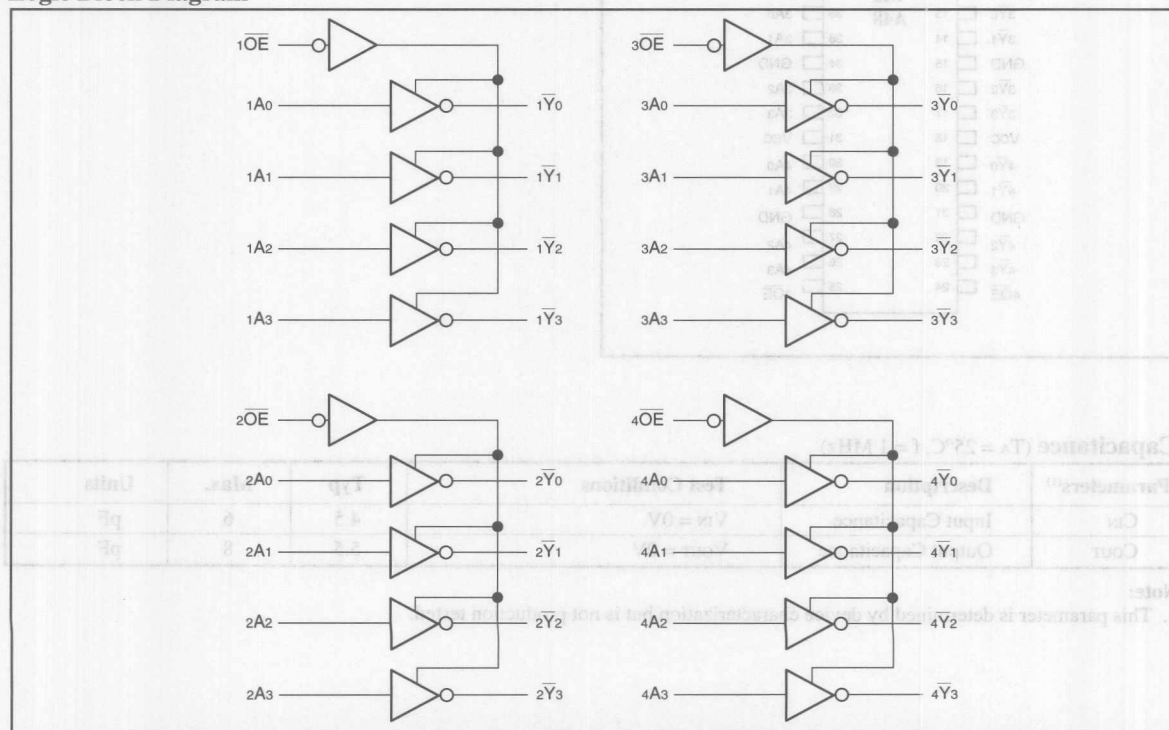
**Fast CMOS 3.3V 16-Bit
Octal Buffer/Line Driver**
Product Features:

- Advanced Low Power CMOS Operation
- Can serve as a 5V to 3V translator
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
Compatible with LVC™ class of products.
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Inputs can be driven by 3.3V or 5V devices
- Multiple center pin and distributed Vcc/GND pins minimizing switching noise
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT163240 is an inverting 16-bit buffer/line driver designed for applications driving high-capacitance loads and low impedance backplanes. This high-speed, low power device offers bus/backplane interface capability and a flow-through organization for ease of board layout. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

4
Logic Block Diagram


Product Pin Description

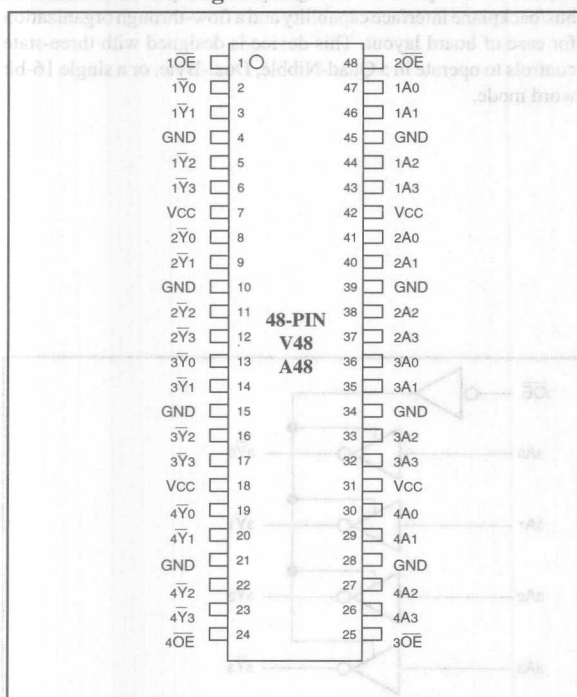
Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	H
L	H	L
H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Product Pin Configuration



Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	V _{CC} +0.5	V
V _{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max. V _{IN} = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	V _{CC} = Max. V _{IN} = V _{CC}	—	—	±1	μA
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max. V _{IN} = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	V _{CC} = Max. V _{IN} = GND	—	—	±1	μA
I _{OZH}	High Impedance Output Current	V _{CC} = Max. V _{OUT} = V _{CC}	—	—	±1	μA
I _{OZL}	(3-State Output pins)	V _{CC} = Max. V _{OUT} = GND	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA	—	-0.7	-1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} , I _{OH} = -0.1 mA	V _{CC} -0.2	—	—	V
		V _{CC} = 3.0V, I _{OH} = -3 mA	2.4	3.0	—	V
		V _{CC} = 3.0V, I _{OH} = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		V _{CC} = 3.0V, I _{OH} = -24 mA	2.0	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 0.1 mA	—	—	0.2	V
		V _{CC} = Min., I _{OL} = 16 mA	—	0.2	0.4	V
		V _{CC} = Min., I _{OL} = 24 mA	—	0.3	0.5	V
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-60	-85	-240	mA
V _H	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- $I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_c = I_{cc} + \Delta I_{cc} \text{ DH} \text{ Nt} + I_{\text{ccd}} (\text{fcp}/2 + \text{fiNi})$
 I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccZ})
 ΔI_{cc} = Power Supply Current for a TTL High Input
 DH = Duty Cycle for TTL Inputs High
 Nt = Number of TTL Inputs at DH
 I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 fcp = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 Ncp = Number of Clock Inputs at fcp
 fi = Input Frequency
 Ni = Number of Inputs at fi
 All currents are in milliamperes and all frequencies are in megahertz.

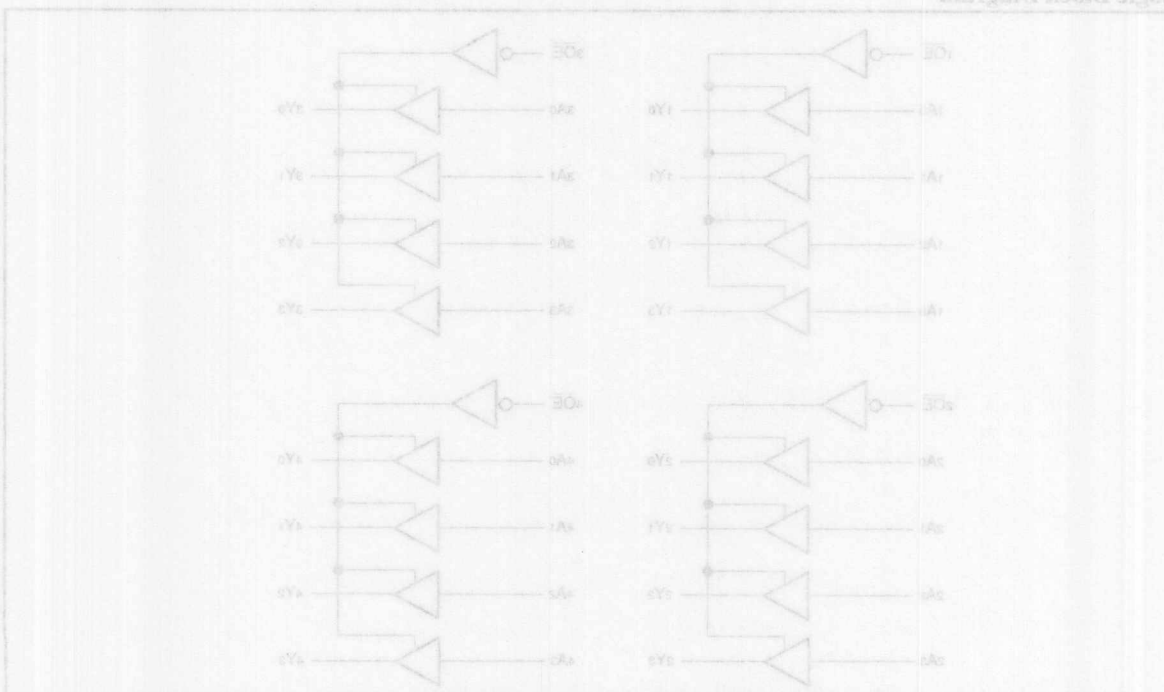
Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	FCT163240		FCT163240A		FCT163240C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	ns
TPHL	xAX to xYx								
tpZH	Output Enable Time		1.5	10.0	1.5	6.2	1.5	5.8	ns
tpZL	xOE to xYx								
tpHZ	Output Disable Time ⁽⁴⁾		1.5	9.5	1.5	5.6	1.5	5.2	ns
tPLZ	xOE to xYx								
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

4

Notes:

1. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. For $V_{CC} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



Fast CMOS 3.3V 16-Bit Buffer/Line Driver

Product Features:

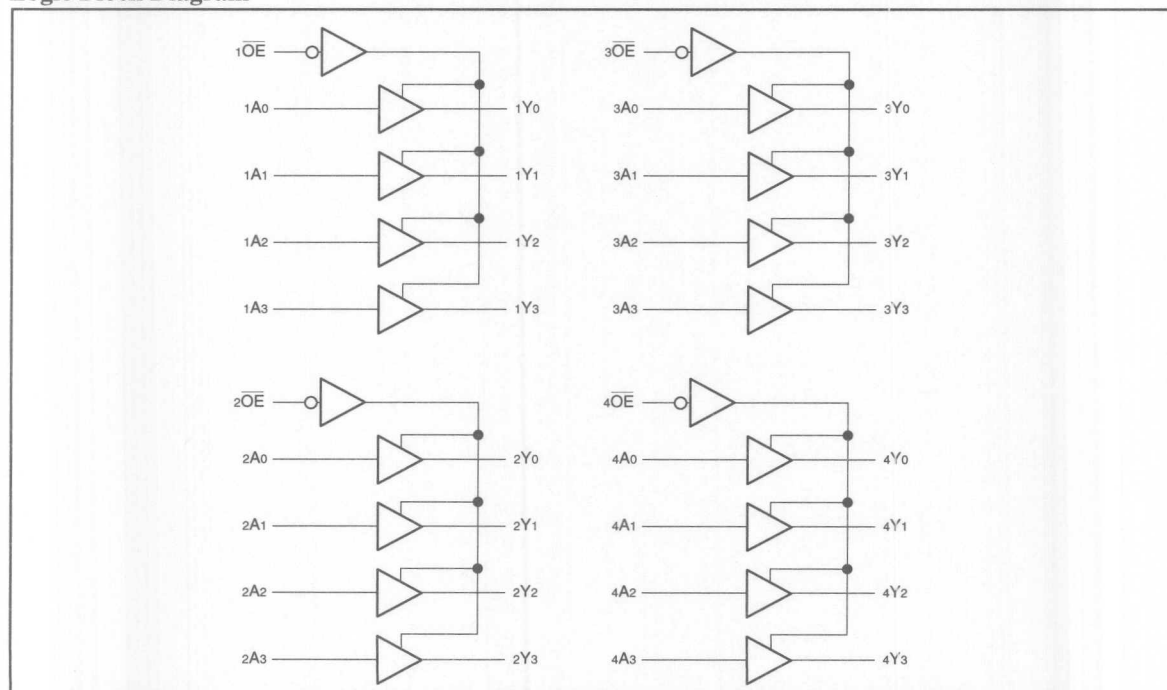
- Advanced Low Power CMOS Operation
- Can serve as a 5V to 3V translator
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
Compatible with LVC™ class of products
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Inputs can be driven by 3.3V or 5V devices
- Multiple center pin and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT163244 is a 16-bit buffer/line driver designed for applications driving high capacitive loads and low impedance backplanes. This high-speed, low power device offers bus/backplane interface capability and a flow-through organization for ease of board layout. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	L
L	H	H
H	X	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Product Pin Configuration

1OE	1	48	2OE
1Y0	2	47	1A0
1Y1	3	46	1A1
GND	4	45	GND
1Y2	5	44	1A2
1Y3	6	43	1A3
Vcc	7	42	Vcc
2Y0	8	41	2A0
2Y1	9	40	2A1
GND	10	39	GND
2Y2	11	38	2A2
2Y3	12	37	2A3
3Y0	13	36	3A0
3Y1	14	35	3A1
GND	15	34	GND
3Y2	16	33	3A2
3Y3	17	32	3A3
Vcc	18	31	Vcc
4Y0	19	30	4A0
4Y1	20	29	4A1
GND	21	28	GND
4Y2	22	27	4A2
4Y3	23	26	4A3
4OE	24	25	4OE

4
Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = VCC	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	Vcc-0.2	—	—	V
		VCC = Min., VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
Ios	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

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Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- $I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_c = I_{\text{cc}} + \Delta I_{\text{cc}} D_H N_t + I_{\text{ccd}} (f_{\text{CP}}/2 + f_i N_i)$
 $I_{\text{cc}} = \text{Quiescent Current (IcCL, IcCH and IcCZ)}$
 $\Delta I_{\text{cc}} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_t = \text{Number of TTL Inputs at } D_H$
 $I_{\text{ccd}} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{\text{CP}} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{\text{CP}} = \text{Number of Clock Inputs at } f_{\text{CP}}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	FCT163244		FCT163244A		FCT163244C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay xAX to xYx	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
tpZH tpZL	Output Enable Time xOE to xYx		1.5	8.0	1.5	6.2	1.5	5.8	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ xOE to xYx		1.5	7.0	1.5	5.6	1.5	5.2	ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. For $V_{CC} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Fast CMOS 3.3V 16-Bit Bidirectional Transceiver

Product Features:

- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
Compatible with LVCTM class of products.
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Control inputs can be driven by 3.3V or 5V devices
- Multiple center pin and distributed Vcc/GND pins minimizing switching noise
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

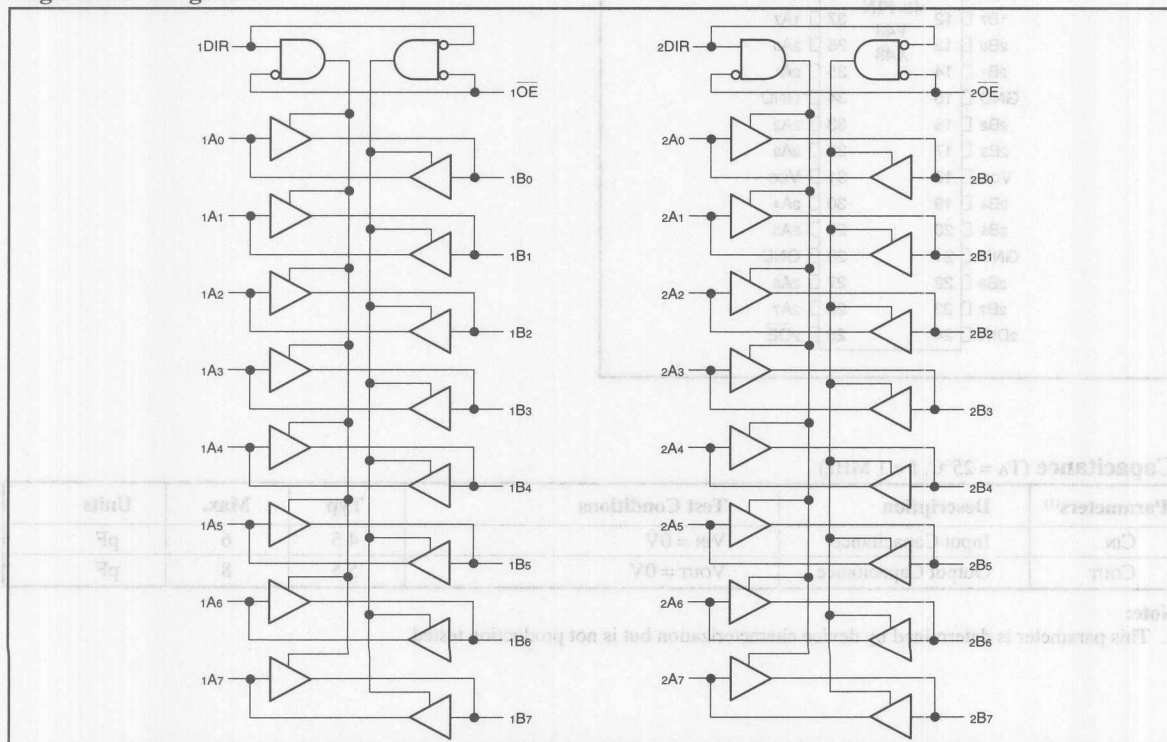
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT163245 is a 16-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The direction control input pin (xDIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable (xOE) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

4

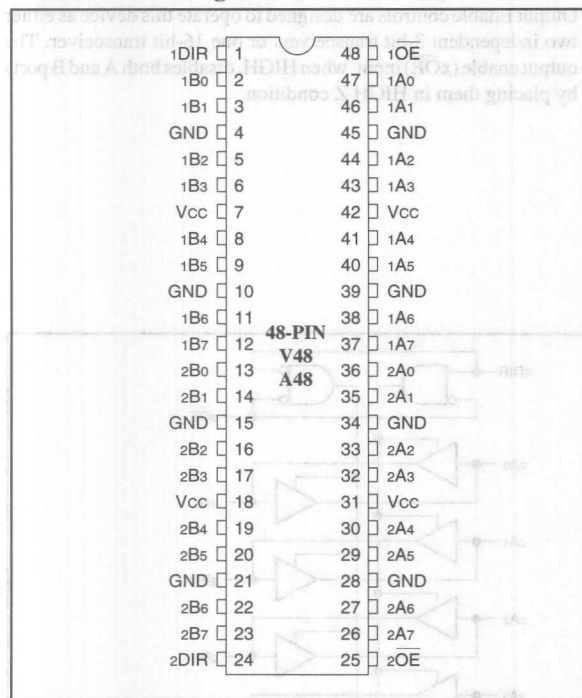
Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Inputs
xBx	Side B Outputs or 3-State Outputs
GND	Ground
Vcc	Power

Product Pin Configuration



Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

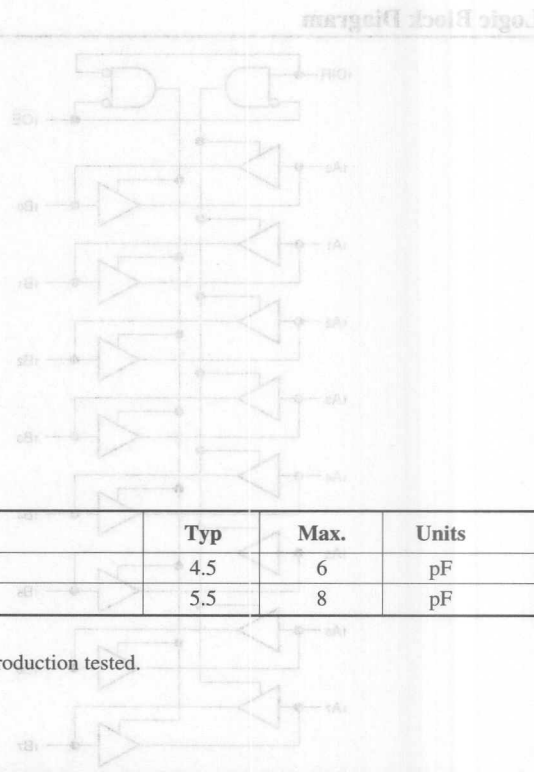
1. This parameter is determined by device characterization but is not production tested.

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	V _{CC} +0.5	V
V _{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max. V _{IN} = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	V _{CC} = Max. V _{IN} = V _{CC}	—	—	±1	μA
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max. V _{IN} = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	V _{CC} = Max. V _{IN} = GND	—	—	±1	μA
IOZH	High Impedance Output Current	V _{CC} = Max. V _{OUT} = V _{CC}	—	—	±1	μA
IOZL	(3-State Output pins)	V _{CC} = Max. V _{OUT} = GND	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. I _{OH} = -0.1 mA	V _{CC} -0.2	—	—	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -3 mA	2.4	3.0	—	V
		V _{CC} = 3.0V, I _{OH} = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -24 mA	2.0	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. I _{OL} = 0.1 mA	—	—	0.2	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 16 mA	—	0.2	0.4	V
		I _{OL} = 24 mA	—	0.3	0.5	V
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-60	-85	-240	mA
V _H	Input Hysteresis			150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccp}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = xDIR = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = xDIR = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = xDIR = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

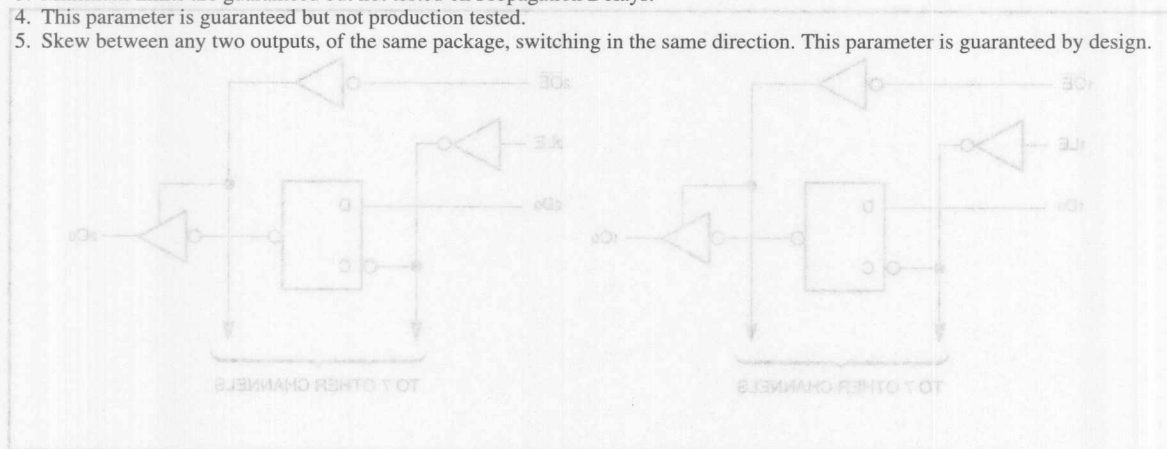
- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} \cdot DH_{NT} + I_{ccp} (f_{cp}/2 + f_i N_i)$
 I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccZ})
 ΔI_{cc} = Power Supply Current for a TTL High Input
 DH = Duty Cycle for TTL Inputs High
 NT = Number of TTL Inputs at DH
 ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{cp} = Number of Clock Inputs at f_{cp}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	FCT163245		FCT163245A		FCT163245C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay A to B, B to A	C _L = 50 pF R _L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	ns
tpZH tpZL	Output Enable Time xOE to A or B		1.5	9.5	1.5	6.2	1.5	5.8	ns
tpHZ tpLZ	Output Disable Time ⁽⁴⁾ xOE to A or B		1.5	7.5	1.5	5.0	1.5	4.8	ns
tpZH tpZL	Output Enable Time xDIR to A or B		1.5	9.5	1.5	6.2	1.5	5.8	ns
tpHZ tpLZ	Output Disable Time ⁽⁴⁾ xDIR to A or B		1.5	7.5	1.5	5.0	1.5	4.8	ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



Fast CMOS 3.3V 16-Bit Transparent Latch

Product Features:

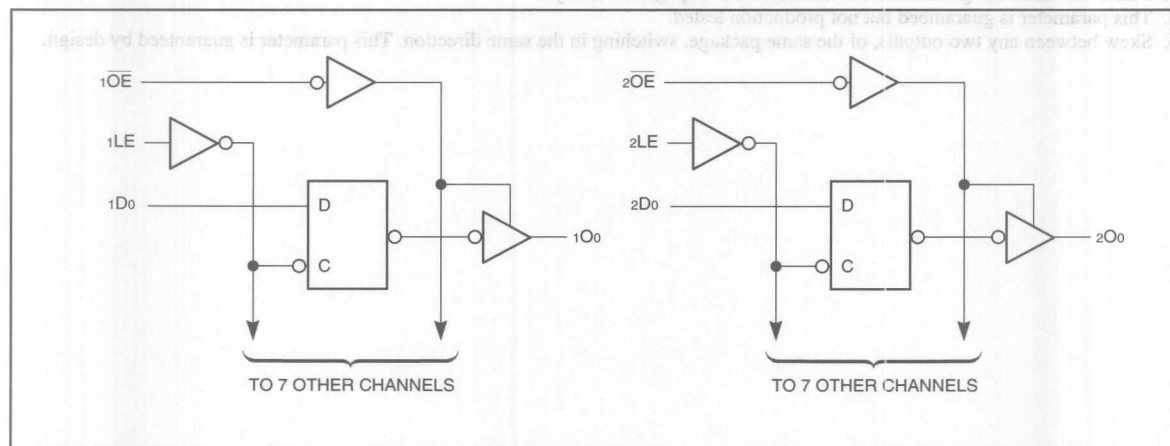
- Advanced Low Power CMOS Operation
- Can serve as a 5V to 3V translator
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
Compatible with LVC™ class of products.
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Inputs can be driven by 3.3V or 5V devices
- Multiple center pin and distributed Vcc/GND pins minimizing switching noise
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT163373 is a 16-bit transparent latch designed with 3-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{\text{OE}}$ is HIGH, the bus output is in the high impedance state.

Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xLE	Latch Enable Inputs (Active HIGH)
xDx	Data Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾			Outputs ⁽¹⁾
xDx	xLE	xOE	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Product Pin Configuration

1OE	1	48	1LE
1O0	2	47	1D0
1O1	3	46	1D1
GND	4	45	GND
1O2	5	44	1D2
1O3	6	43	1D3
Vcc	7	42	Vcc
1O4	8	41	1D4
1O5	9	40	1D5
GND	10	39	GND
1O6	11	38	1D6
1O7	12	37	1D7
2O0	13	36	2D0
2O1	14	35	2D1
GND	15	34	GND
2O2	16	33	2D2
2O3	17	32	2D3
Vcc	18	31	Vcc
2O4	19	30	2D4
2O5	20	29	2D5
GND	21	28	GND
2O6	22	27	2D6
2O7	23	26	2D7
2OE	24	25	2LE

4
Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max. VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max. VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max. VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max. VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max. VOUT = VCC	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max. VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min. IOH = -0.1 mA	Vcc-0.2	—	—	V
		VIN = VIH or VIL IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min. IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL IOL = 16 mA	—	0.2	0.4	V
		IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND xLE = V _{cc} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND xLE = V _{cc} One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND xLE = V _{cc} 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

4
Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{cp}/2 + f_i N_i)$
I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccZ})
ΔI_{cc} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{cp} = Number of Clock Inputs at f_{cp}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	FCT163373		FCT163373A		FCT163373C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	8.5	2.0	5.5	ns
tpZH tpZL	Output Enable Time xOE to xOx		1.5	12.0	1.5	6.5	1.5	5.5	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ xOE to xOx		1.5	7.5	1.5	5.5	1.5	5.0	ns
tsu	Setup Time HIGH or LOW, xDx to xLE		2.0		2.0		2.0		ns
th	Hold Time HIGH or LOW, xDx to xLE		1.5		1.5		1.5		ns
tw	xLE Pulse Width HIGH		6.0		5.0		5.0		ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Fast CMOS 3.3V 16-Bit Register (3-State)

Product Features:

- Advanced Low Power CMOS Operation
- Can serve as a 5V to 3V translator
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
Compatible with LVC™ class of products.
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Inputs can be driven by 3.3V or 5V devices
- Multiple center pin and distributed Vcc/GND pins minimizing switching noise
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

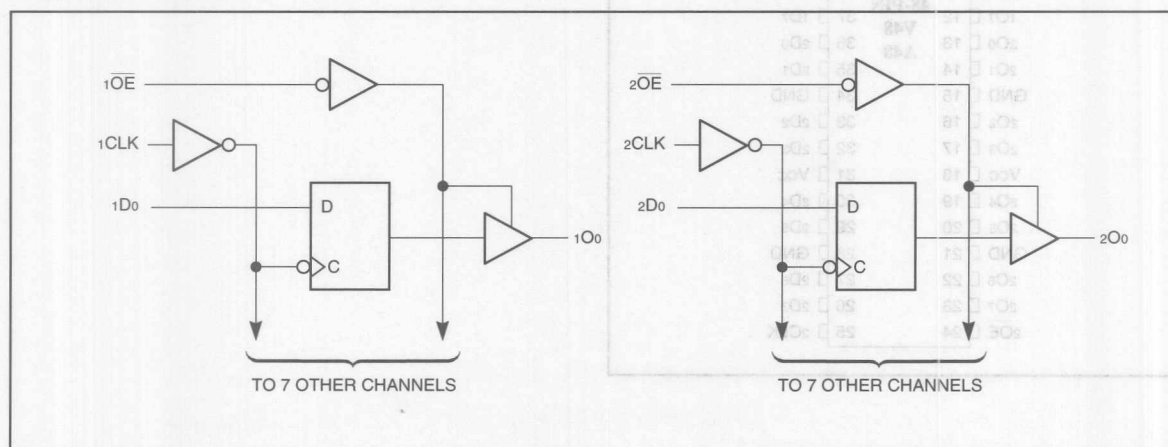
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT163374 is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and 3-state outputs. The Output Enable ($\overline{\text{xOE}}$) and clock (xCLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When OE is HIGH, the outputs are in the high-impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

4

Logic Block Diagram



Parameter	Description	Test Conditions	Typ	Max	Units
C_{in}	Input Capacitance	$V_{in} = 0\text{V}$	4.3	6	pf
C_{out}	Output Capacitance	$V_{out} = 0\text{V}$	2.2	8	pf

Note:
1. This parameter is determined by device characterization but is not production tested.

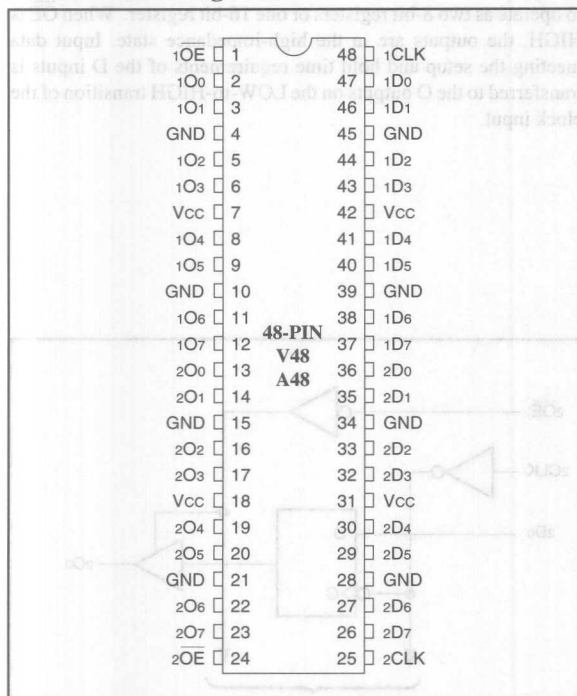
Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xCLK	Clock Inputs
xDx	Data Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Function	Inputs ⁽¹⁾			Outputs ⁽¹⁾
	xDx	xCLK	xOE	xOx
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

Product Pin Configuration



Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0 V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0 V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	µA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	µA
IOZH	High Impedance Output Current	VCC = Max., VOUT = VCC	—	—	±1	µA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	µA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., IOH = -0.1 mA	VCC-0.2	—	—	V
		VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		IOL = 24 mA	—	0.3	0.5	V
Ios	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open fi = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open fi = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_t + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
ΔI_{CC} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_t = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{CP} = Number of Clock Inputs at f_{CP}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	FCT163374		FCT163374A		FCT163374C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50 pF RL = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	ns
tPZH tPZL	Output Enable Time xOE to xOx		1.5	12.5	1.5	6.5	1.5	5.5	ns
tPHZ tPLZ	Output Disable Time ⁽⁴⁾ xOE to xOx		1.5	8.0	1.5	5.5	1.5	5.0	ns
tSU	Setup Time HIGH or LOW, xDx to xCLK		2.0		2.0		2.0		ns
tH	Hold Time HIGH or LOW, xDx to xCLK		1.5		1.5		1.5		ns
tW	xCLK Pulse Width HIGH ⁽⁴⁾		7.0		5.0		5.0		ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

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Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	PCT163374		PCT163374A		PCT163374C		Unit
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tpd	Propagation Delay XCLK to XQx	CL = 50 pF RL = 500Ω	2.0	10.0	2.0	0.3	2.0	2.2	ns
			1.5	12.5	1.2	0.3	1.2	2.2	ns
tPHZ	Output Enable Time XOE to XQx		1.5	8.0	1.2	2.2	1.2	2.0	ns
			1.5	8.0	1.2	2.2	1.2	2.0	ns
tPLZ	Output Disable Time ⁽⁴⁾ XOE to XQx		2.0		2.0		2.0		ns
			1.2		1.2		1.2		ns
tH	Hold Time HIGH or LOW, XQx to XQLE		7.0		3.0		2.0		ns
			7.0		3.0		2.0		ns
tW	XCLK Pulse Width HIGH ⁽⁵⁾		0.3		0.3		0.3		ns
			0.3		0.3		0.3		ns

Notes:

1. Propagation Delays and Enable/Disable times are with VCC = 3.3V to 3.5V, normal range. For VCC = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 10%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Slew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

GENERAL INFORMATION**1****STANDARD AND 25Ω OUTPUT RESISTOR SERIES
5V FCT LOGIC PRODUCTS****2****DOUBLE DENSITY STANDARD
5V FCT LOGIC PRODUCTS****3****DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS****4****STANDARD 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****5****DOUBLE DENSITY 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****6****SPECIALTY LOGIC PRODUCTS****7****BUS SWITCH PRODUCTS****8****CLOCK DISTRIBUTION PRODUCTS****9****CLOCK GENERATOR PRODUCTS****10****NETWORKING PRODUCTS****11****APPLICATION NOTES****12****QUALITY AND RELIABILITY INFORMATION****13****PACKAGE MECHANICAL OUTLINES****14****SALES AND DISTRIBUTION LOCATIONS****15**

3.3V FCT LOGIC PRODUCTS WITH 5V TOLERANT I/O

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PI74LPT373	Fast CMOS 3.3V, 5V Tolerant I/O 8-Bit Transparent Latch	5.9
PI74LPT541	Fast CMOS 3.3V, 5V Tolerant I/O 8-Bit Register (3-State)	5.13
PI74LPT573	Fast CMOS 3.3V, 5V Tolerant I/O 8-Bit Transparent Latch	5.17



PI74LPT244

Fast CMOS 3.3V 8-Bit Buffer/Line Driver

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
 - Balanced drives (24 mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

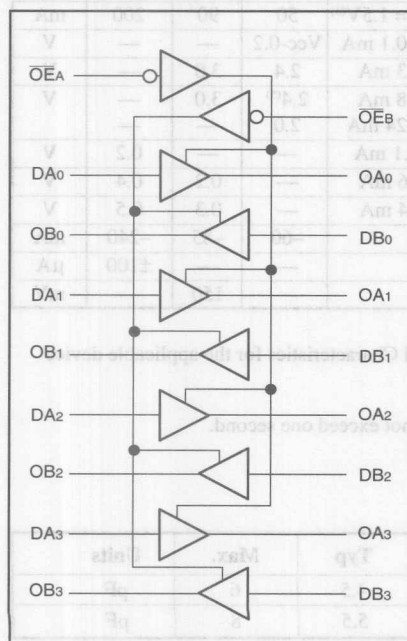
Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT244 is an 8-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines.

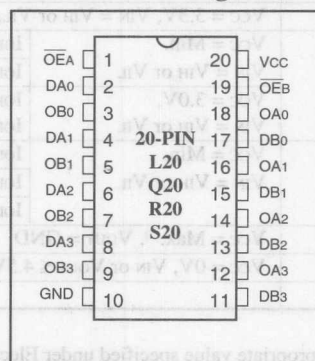
The PI74LPT244 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

5

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
OE A, OE B	3-State Output Enable Inputs (Active LOW)
Dxx	Inputs
Oxx	Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs		Outputs	
OE A	OE B	Dxx	Oxx
L	L	L	L
L	L	H	H
H	H	X	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max. VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max. VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max. VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max. VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max. VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max. VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min. IOH = -0.1 mA	VCC-0.2	—	—	V
		VIN = VIH or VIL IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min. IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL IOL = 16 mA	—	0.2	0.4	V
		IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = VCC - 0.6V at rated current.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open O _{EX} = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle O _{EX} = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle O _{EX} = GND 8 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

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Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_c = I_{CC} + ΔI_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)
I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
ΔI_{CC} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{CP} = Number of Clock Inputs at f_{CP}
f_i = Input Frequency
N_I = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT244		LPT244A		LPT244C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay Dxx to Oxx	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
tPZH tPZL	Output Enable Time OE _x to Oxx		1.5	8.0	1.5	6.2	1.5	5.8	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ OE _x to Oxx		1.5	7.0	1.5	5.6	1.5	5.2	ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Pericom Semiconductor Corporation

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Fast CMOS 3.3V 8-Bit Bidirectional Transceiver

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
 - Balanced drives (24 mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

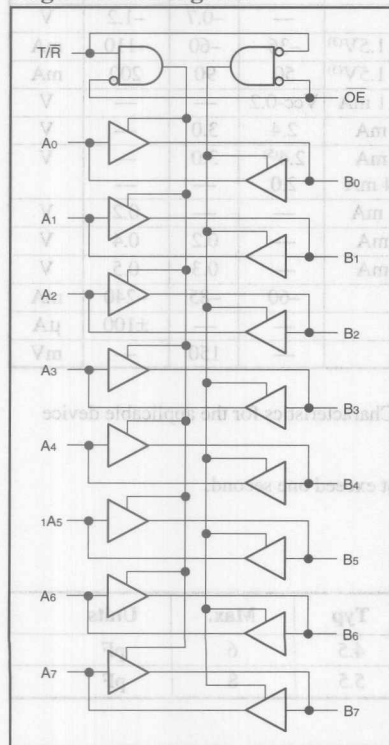
Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT245 is an 8-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The transmit/receive input pin (T/R) determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable (OE) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The PI74LPT245 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

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Logic Block Diagram



Product Pin Configuration

T/R	1	20	VCC
A0	2	19	OE
A1	3	18	B0
A2	4	17	B1
A3	5	16	B2
A4	6	15	B3
A5	7	14	B4
A6	8	13	B5
A7	9	12	B6
GND	10	11	B7

Product Pin Description

Pin Name	Description
OE	3-State Output Enable Inputs (Active LOW)
T/R	Direction Control Input
A7-A0	Side A Inputs or 3-State Outputs
B7-B0	Side B Inputs or 3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High StateZ

Note:

1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	VCC-0.2	—	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle OE = GND 8 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

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Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

ADVANCE INFORMATION

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT245		LPT245A		LPT245C		Unit
			Com.		Com.		Com.		
			Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	ns
tPHL	A to B, B to A								
tpZH	Output Enable Time		1.5	8.5	1.5	6.2	1.5	5.8	ns
tpZL	OE to A or B								
tpHZ	Output Disable Time ⁽⁴⁾		1.5	7.5	1.5	5.0	1.5	4.8	ns
tPLZ	OE to A or B								
tpZH	Output Enable Time	V _{CC} = 3.3V ± 0.3V V _{CC} = 2.7V ± 0.3V	1.5	8.5	1.5	6.2	1.5	5.8	ns
tpZL	T/R to A or B								
tpHZ	Output Disable Time ⁽⁴⁾		1.5	7.5	1.5	5.0	1.5	4.8	ns
tPLZ	T/R to A or B								
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ± 0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Fast CMOS 3.3V 8-Bit Transparent Latch

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

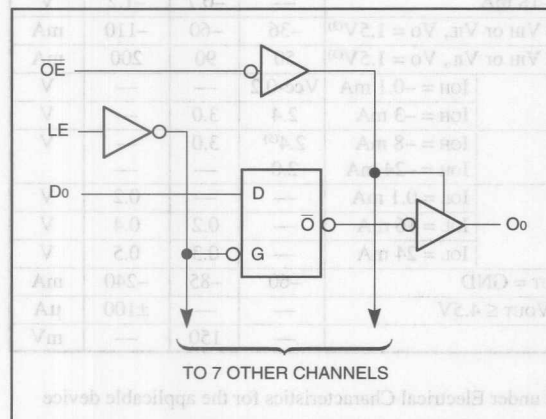
Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT373 is an 8-bit transparent latch designed with 3-state outputs and is intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When OE is HIGH, the bus output is in the high impedance state.

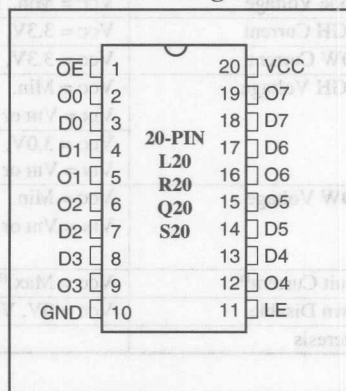
The PI74LPT373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

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Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D7-D0	Data Inputs
O7-O0	3-State Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs			Outputs
DN	LE	OE	ON
H	H	L	H
L	H	L	L
X	X	H	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	Vcc = Max., VIN = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	Vcc = Max., VIN = Vcc	—	—	±1	µA
IIL	Input LOW Current (Input pins)	Vcc = Max., VIN = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	Vcc = Max., VIN = GND	—	—	±1	µA
IOZH	High Impedance Output Current	Vcc = Max., VOUT = 5.5V	—	—	±1	µA
IOZL	(3-State Output pins)	Vcc = Max., VOUT = GND	—	—	±1	µA
VIK	Clamp Diode Voltage	Vcc = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	Vcc = Min., VIN = VIH or VIL, IOH = -0.1 mA	Vcc-0.2	—	—	V
		Vcc = Min., VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		Vcc = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		Vcc = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	Vcc = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		Vcc = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		Vcc = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	Vcc = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	Vcc = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	µA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = Vcc - 0.6V at rated current.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle OE = GND 8 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT373		LPT373A		LPT373C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay Dx to Ox	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay LE to Ox		2.0	8.5	2.0	8.5	2.0	5.5	ns
tpZH tpZL	Output Enable Time OE to Ox		1.5	8.5	1.5	6.5	1.5	5.5	ns
tpHZ tpLZ	Output Disable Time ⁽⁴⁾ OE to Ox		1.5	7.5	1.5	5.5	1.5	5.0	ns
tsU	Setup Time HIGH or LOW, Dx to LE		2.0		2.0		2.0		ns
tH	Hold Time HIGH or LOW, Dx to LE		1.5		1.5		1.5		ns
tw	LE Pulse Width HIGH ⁽⁴⁾		6.0		5.0		5.0		ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ± 0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74LPT541

Fast CMOS 3.3V 8-Bit Buffer/Line Driver

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
 - Balanced drives (24 mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

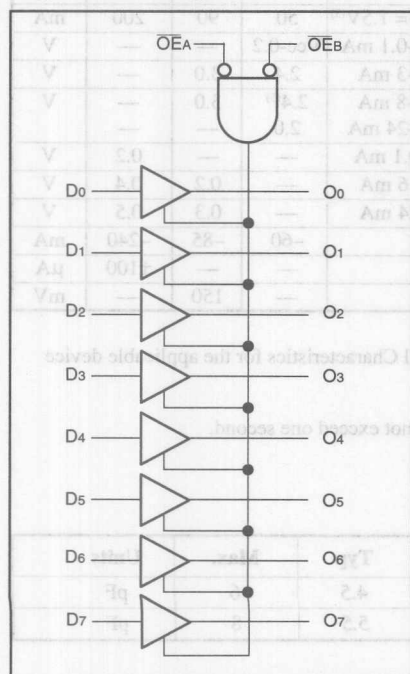
Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT541 is an 8-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines. This device offers a flow-through organization for ease of board layout.

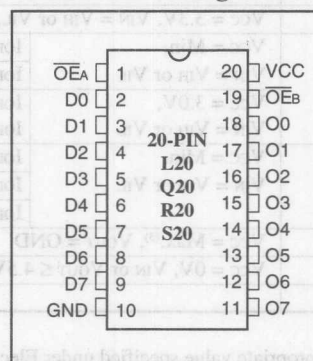
The PI74LPT541 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

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Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
OEa, OEb	3-State Output Enable Inputs (Active LOW)
D7-D0	Inputs
O7-O0	Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs			Outputs
OEa	OEb	Dx	Ox
L	L	L	L
L	L	H	H
H	H	X	Z

Note:

1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max.	VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max.	VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max.	VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max.	VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current (3-State Output pins)	VCC = Max.	VOUT = 5.5V	—	—	±1	μA
IOZL		VCC = Max.	VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min.	IOH = -0.1 mA	VCC-0.2	—	—	V
		VIN = VIH or VIL	IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V,	IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL	IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min.	IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL	IOL = 16 mA	—	0.2	0.4	V
			IOL = 24 mA	—	0.3	0.5	V
Ios	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V		—	—	±100	μA
VH	Input Hysteresis			—	150	—	mV

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = VCC - 0.6V at rated current.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{in} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{in} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open OE _x = GND One Bit Toggling 50% Duty Cycle	V _{in} = V _{cc} V _{in} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE _x = GND One Bit Toggling	V _{in} = V _{cc} - 0.6V V _{in} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle OE _x = GND 8 Bits Toggling	V _{in} = V _{cc} - 0.6V V _{in} = GND		2.1	4.7 ⁽⁵⁾	

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Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_I + I_{ccd} (f_{cp}/2 + f_i N_i)$
I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccz})
ΔI_{cc} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_I = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{cp} = Number of Clock Inputs at f_{cp}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT541		LPT541A		LPT541C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay Dx to Ox	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	4.8	1.5	4.1	ns
tpZH tpZL	Output Enable Time OEx to Ox		1.5	9.5	1.5	6.2	1.5	5.8	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ OEx to Ox		1.5	6.5	1.5	5.6	1.5	5.2	ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ± 0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Pericom Semiconductor Corporation

2380 Bering Drive • San Jose, CA 95131 (408) 435-0800 • Fax (408) 435-1100

Fast CMOS 3.3V 8-Bit Transparent Latch

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 150 mil wide plastic TQSOP (R20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

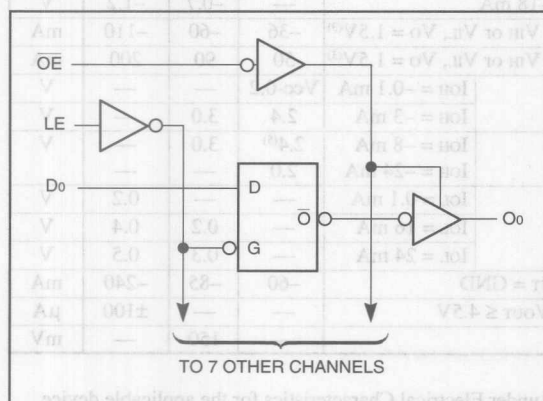
Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT573 is an 8-bit transparent latch designed with 3-state outputs and is intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When OE is HIGH, the bus output is in the high impedance state.

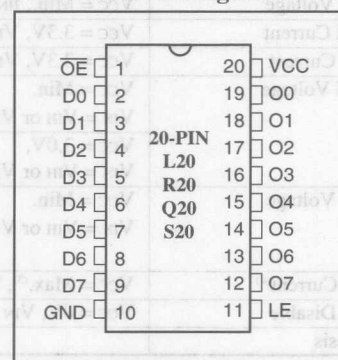
The PI74LPT573 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

5

Logic Block Diagram



Product Pin Configuration



Truth Table

Inputs ⁽¹⁾			Outputs ⁽¹⁾
DN	LE	OE	ON
H	H	L	H
L	H	L	L
X	X	H	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D7-D0	Data Inputs
O7-O0	3-State Outputs
GND	Ground
Vcc	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., IOH = -0.1 mA	VCC-0.2	—	—	V
		VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle OE = GND 8 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$$I_{CC} = \text{Quiescent Current (I}_{CC_L}, I_{CC_H} \text{ and } I_{CC_Z})$$

$$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$$

$$D_H = \text{Duty Cycle for TTL Inputs High}$$

$$N_T = \text{Number of TTL Inputs at } D_H$$

$$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$$

$$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$$

$$N_{CP} = \text{Number of Clock Inputs at } f_{CP}$$

$$f_i = \text{Input Frequency}$$

$$N_i = \text{Number of Inputs at } f_i$$

All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT573		LPT573A		LPT573C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay Dx to Ox	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay LE to Ox		2.0	12.0	2.0	8.5	2.0	5.5	ns
tPZH tPZL	Output Enable Time OE to Ox		1.5	9.5	1.5	6.5	1.5	5.5	ns
tPHZ tPLZ	Output Disable Time ⁽⁴⁾ OE to Ox		1.5	6.5	1.5	5.5	1.5	5.0	ns
tsu	Setup Time HIGH or LOW, Dx to LE		2.0		2.0		2.0		ns
th	Hold Time HIGH or LOW, Dx to LE		1.5		1.5		1.5		ns
tw	LE Pulse Width ⁽⁴⁾ HIGH		6.0		5.0		5.0		ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ± 0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

GENERAL INFORMATION**1****STANDARD AND 25Ω OUTPUT RESISTOR SERIES
5V FCT LOGIC PRODUCTS****2****DOUBLE DENSITY STANDARD
5V FCT LOGIC PRODUCTS****3****DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS****4****STANDARD 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****5****DOUBLE DENSITY 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****6****SPECIALTY LOGIC PRODUCTS****7****BUS SWITCH PRODUCTS****8****CLOCK DISTRIBUTION PRODUCTS****9****CLOCK GENERATOR PRODUCTS****10****NETWORKING PRODUCTS****11****APPLICATION NOTES****12****QUALITY AND RELIABILITY INFORMATION****13****PACKAGE MECHANICAL OUTLINES****14****SALES AND DISTRIBUTION LOCATIONS****15**

**DOUBLE DENSITY
3.3V FCT LOGIC PRODUCTS
WITH 5V TOLERANT I/O**

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PI74LPT16245	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Bidirectional Transceiver	6.11
PI74LPT16373	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Transparent Latch	6.16
PI74LPT16374	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Register (3-State)	6.21
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PI74LPT16543	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Latched Transceivers	6.31
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PI74LPT16952	Fast CMOS 3.3V, 5V Tolerant I/O 16-Bit Registered Transceivers	6.53

**Fast CMOS 3.3V 16-Bit
Buffer/Line Driver**
Product Features:

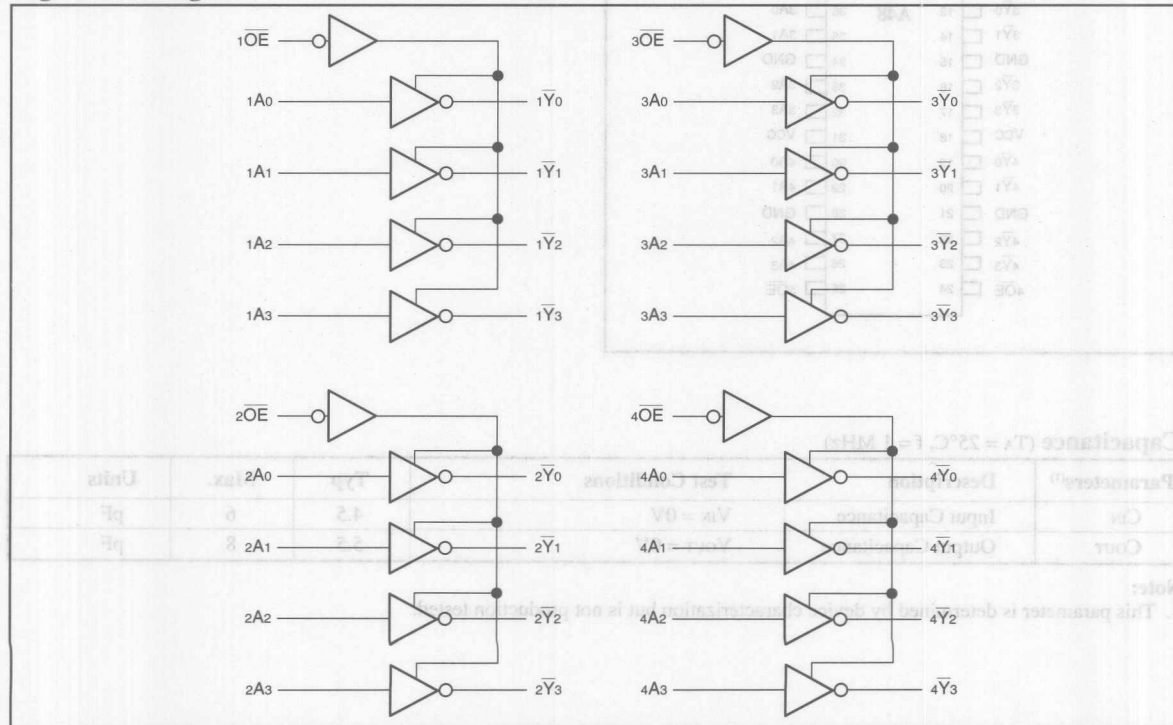
- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 48-pin 240 mil wide thin plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

Product Description:

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16240 is an inverting 16-bit buffer/line driver designed for applications driving high-capacitance loads and low impedance backplanes. This high-speed, low power device offers bus/backplane interface capability and a flow-through organization for ease of board layout. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The PI74LPT16240 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

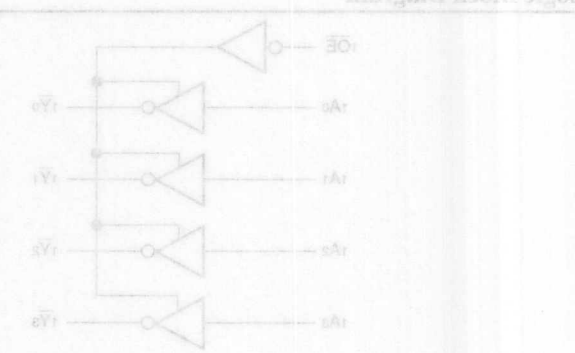
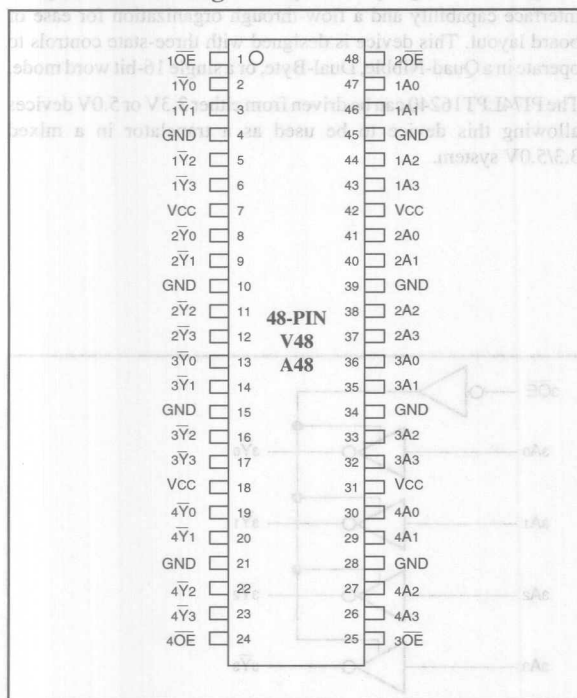
6
Logic Block Diagram


Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
Vcc	Power

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	H
L	H	L
H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Product Pin Configuration



Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max. VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max. VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max. VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max. VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max. VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max. VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, Vo = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, Vo = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min. IOH = -0.1 mA	Vcc-0.2	—	—	V
		VIN = VIH or VIL IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min. IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL IOL = 16 mA	—	0.2	0.4	V
		IOL = 24 mA	—	0.3	0.5	V
Ios	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = Vcc - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{cp}/2 + f_i N_i)$
I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccZ})
ΔI_{cc} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{cp} = Number of Clock Inputs at f_{cp}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

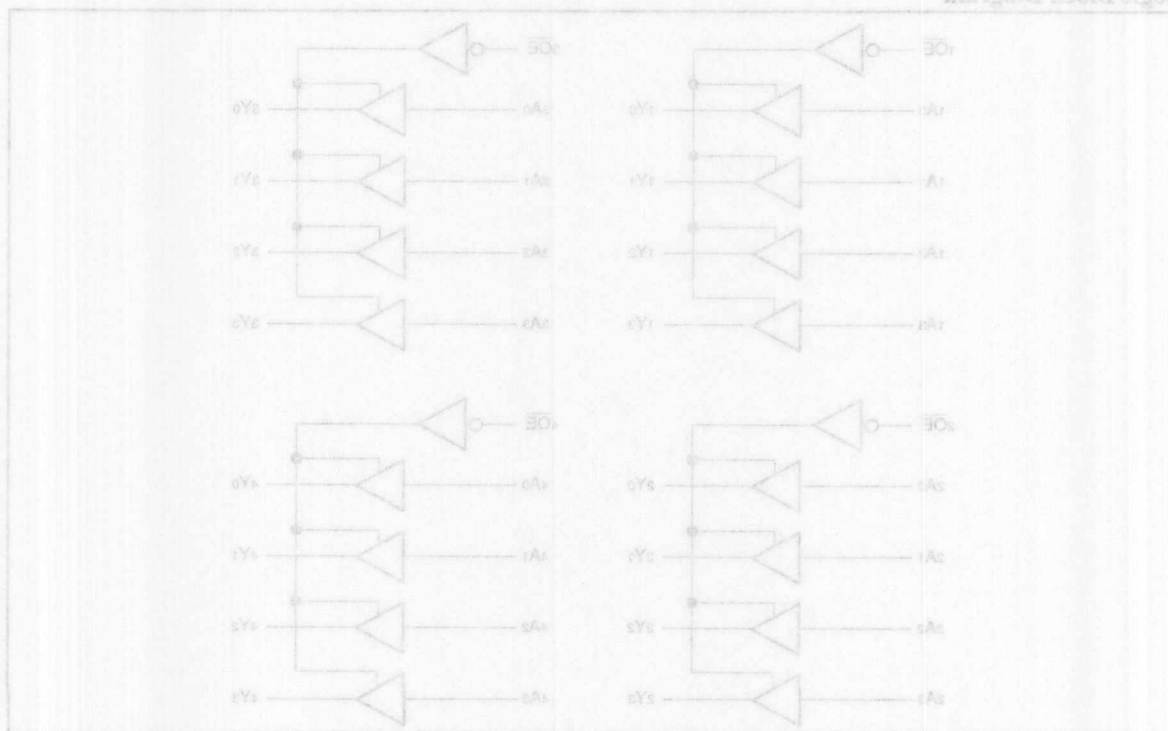
Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16240		LPT16240A		LPT16240C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	4.9	1.5	4.8	1.5	4.3	ns
tPHL	xAx to xYx								
tpZH	Output Enable Time		1.5	7.0	1.5	6.2	1.5	5.8	ns
tpZL	xOE to xYx								
tpHZ	Output Disable Time ⁽⁴⁾		1.5	7.0	1.5	5.6	1.5	5.2	ns
tplZ	xOE to xYx								
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ± 0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

6



Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 48-pin 240 mil wide thin plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

Fast CMOS 3.3V 16-Bit Buffer/Line Driver

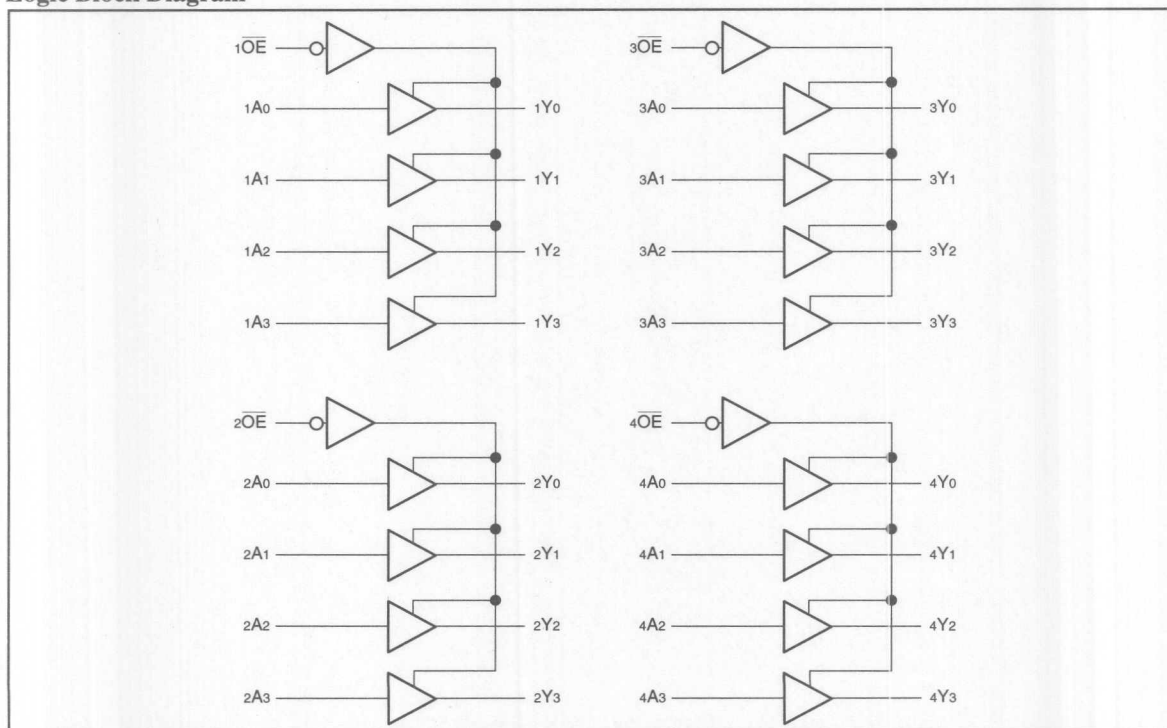
Product Description:

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16244 is a 16-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The PI74LPT16244 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
xOE	xAx	xYx
L	L	L
L	H	H
H	X	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Product Pin Configuration

1OE	1	48	2OE
1Y0	2	47	1A0
1Y1	3	46	1A1
GND	4	45	GND
1Y2	5	44	1A2
1Y3	6	43	1A3
Vcc	7	42	Vcc
2Y0	8	41	2A0
2Y1	9	40	2A1
GND	10	39	GND
2Y2	11	38	2A2
2Y3	12	37	2A3
3Y0	13	36	3A0
3Y1	14	35	3A1
GND	15	34	GND
3Y2	16	33	3A2
3Y3	17	32	3A3
Vcc	18	31	Vcc
4Y0	19	30	4A0
4Y1	20	29	4A1
GND	21	28	GND
4Y2	22	27	4A2
4Y3	23	26	4A3
4OE	24	25	4OE

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Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max. VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max. VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max. VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max. VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max. VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max. VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min. IOH = -0.1 mA	Vcc-0.2	—	—	V
		VIN = VIH or VIL IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min. IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL IOL = 16 mA	—	0.2	0.4	V
		IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

6
Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_{CP}/2 + f_iN_i)
I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CCZ})
ΔI_{CC} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{CP} = Number of Clock Inputs at f_{CP}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16244		LPT16244A		LPT16244C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay xAX to xYx	CL = 50 pF RL = 500Ω	1.5	5.2	1.5	4.8	1.5	4.1	ns
tpZH tpZL	Output Enable Time xOE to xYx		1.5	7.0	1.5	6.2	1.5	5.8	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ xOE to xYx		1.5	7.0	1.5	5.6	1.5	5.2	ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74LPT16245

Fast CMOS 3.3V 16-Bit Bidirectional Transceiver

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 48-pin 240 mil wide thin plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

Product Description:

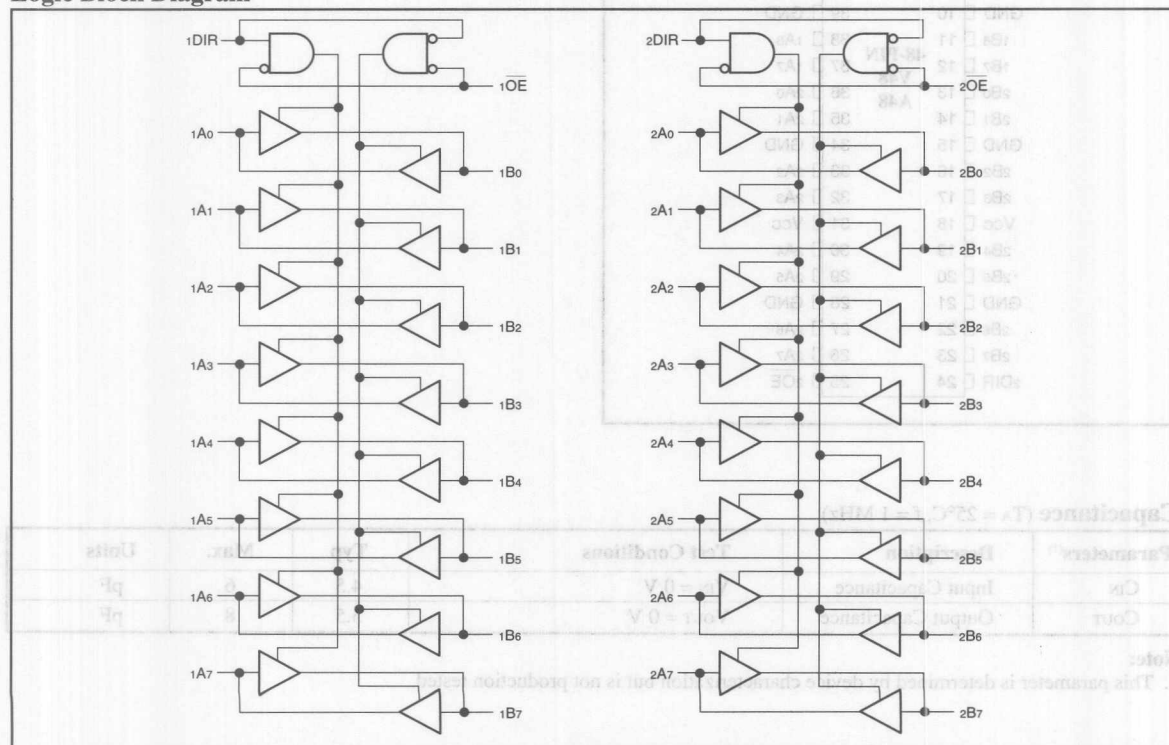
Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16245 is a 16-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The direction control input pin (xDIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The PI74LPT16245 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

6

Logic Block Diagram



Product Pin Description

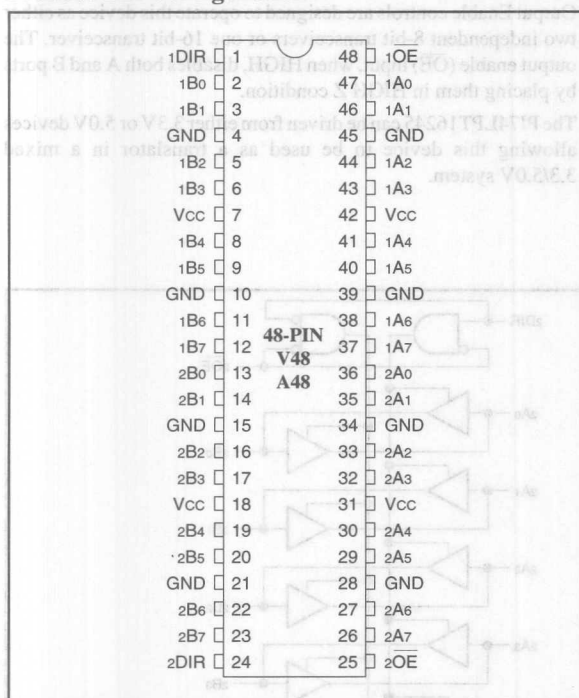
Pin Name	Description
x $\overline{\text{OE}}$	3-State Output Enable Inputs (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Inputs
xBx	Side B Outputs or 3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾		Outputs ⁽¹⁾
x $\overline{\text{OE}}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Product Pin Configuration

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0 V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0 V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	Vcc-0.2	—	—	V
		VCC = 3.0V, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VCC = 3.0V, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = xDIR = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = xDIR = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = xDIR = GND 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

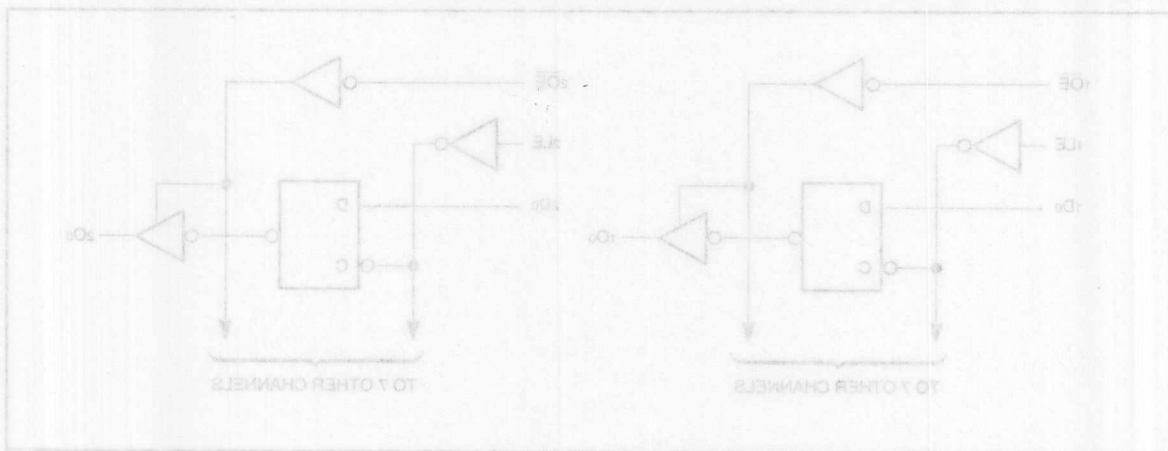
- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
ΔI_{CC} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{CP} = Number of Clock Inputs at f_{CP}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16245		LPT16245A		LPT16245C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	5.2	1.5	4.6	1.5	4.1	ns
tPHL	A to B, B to A								
tpZH	Output Enable Time	xOE to A or B	1.5	7.2	1.5	6.2	1.5	5.8	ns
tpZL	xOE to A or B								
tpHZ	Output Disable Time ⁽⁴⁾	xOE to A or B	1.5	7.2	1.5	5.0	1.5	4.8	ns
tpLZ	xOE to A or B								
tpZH	Output Enable Time	xDIR to A or B	1.5	7.2	1.5	6.2	1.5	5.8	ns
tpZL	xDIR to A or B								
tpHZ	Output Disable Time	xDIR to A or B ⁽⁴⁾	1.5	7.2	1.5	5.0	1.5	4.8	ns
tpLZ	xDIR to A or B ⁽⁴⁾								
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



Fast CMOS 3.3V 16-Bit Transparent Latch

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 48-pin 240 mil wide thin plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

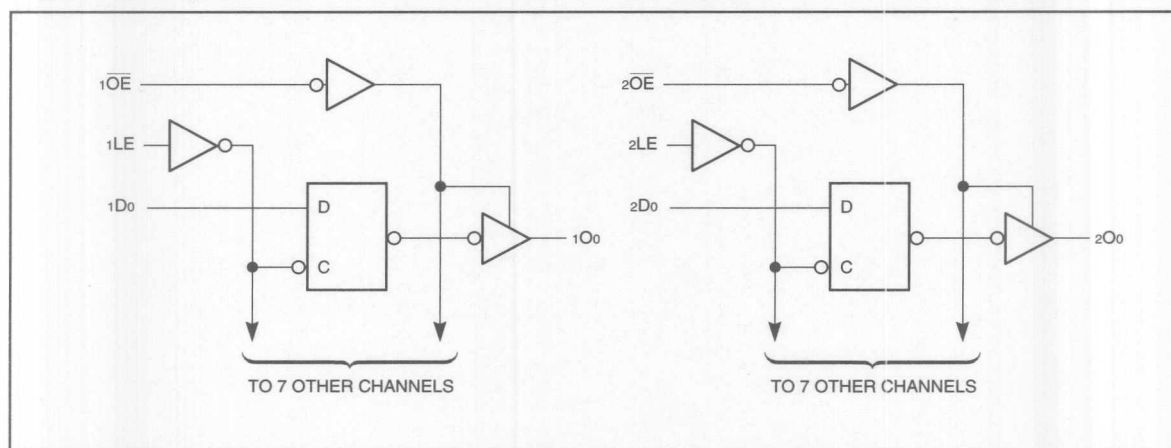
Product Description:

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16373 is a 16-bit transparent latch designed with 3-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{\text{OE}}$ is HIGH, the bus output is in the high impedance state.

The PI74LPT16373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xLE	Latch Enable Inputs (Active HIGH)
xDx	Data Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾			Outputs ⁽¹⁾
xDx	xLE	xOE	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Product Pin Configuration

Pin		Pin	
1OE	1	48	1LE
1O0	2	47	1D0
1O1	3	46	1D1
GND	4	45	GND
1O2	5	44	1D2
1O3	6	43	1D3
Vcc	7	42	Vcc
1O4	8	41	1D4
1O5	9	40	1D5
GND	10	39	GND
1O6	11	38	1D6
1O7	12	37	1D7
2O0	13	36	2D0
2O1	14	35	2D1
GND	15	34	GND
2O2	16	33	2D2
2O3	17	32	2D3
Vcc	18	31	Vcc
2O4	19	30	2D4
2O5	20	29	2D5
GND	21	28	GND
2O6	22	27	2D6
2O7	23	26	2D7
2OE	24	25	2LE

6
Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	VCC-0.2	—	—	V
		VCC = Min., VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
Ios	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND xLE = V _{CC} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND xLE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND xLE = V _{CC} 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
 - Typical values are at V_{CC} = 3.3V, +25°C ambient.
 - Per TTL driven input; all other inputs at V_{CC} or GND.
 - This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
 - Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{\text{CC}} + \Delta I_{\text{CC}} D_H N_T + I_{\text{CCD}} (f_{\text{CP}}/2 + f_i N_i)$
 $I_{\text{CC}} = \text{Quiescent Current (IcCL, IcCH and IcCZ)}$
 $\Delta I_{\text{CC}} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{\text{CCD}} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{\text{CP}} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{\text{CP}} = \text{Number of Clock Inputs at } f_{\text{CP}}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16373		LPT16373A		LPT16373C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	7.0	2.0	6.5	2.0	5.5	ns
tpZH tpZL	Output Enable Time xOE to xOx		1.5	7.2	1.5	6.5	1.5	5.5	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ xOE to xOx		1.5	7.2	1.5	5.5	1.5	5.0	ns
tsu	Setup Time HIGH or LOW, xDx to xLE		2.0		2.0		2.0		ns
th	Hold Time HIGH or LOW, xDx to xLE		1.5		1.5		1.5		ns
tw	xLE Pulse Width ⁽⁴⁾ HIGH		6.0		5.0		5.0		ns
tsk(o)	Output Skew ⁽⁵⁾			0.5		0.5		0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Fast CMOS 3.3V 16-Bit Register (3-State)

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A48)
 - 48-pin 300 mil wide plastic SSOP (V48)

Product Description:

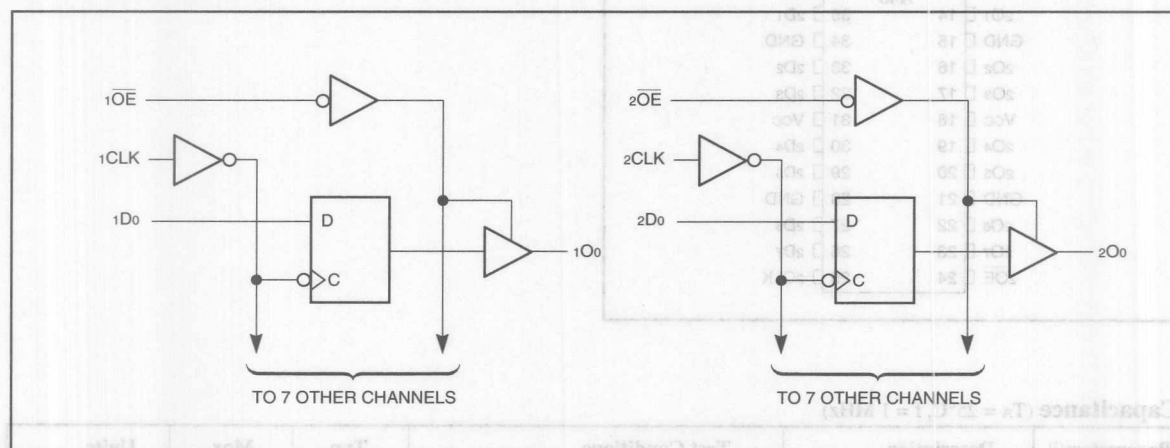
Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16374 is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and 3-state outputs. The Output Enable (xOE) and clock (xCLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When OE is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The PI74LPT16374 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

6

Logic Block Diagram



Pin	Max	Typ	Test Conditions	Function	Parameter
1	8	4.5	V _{in} = 0V	Input Capacitance	C _{in}
2	8	4.5	V _{out} = 0V	Output Capacitance	C _{out}

Note: 1. This parameter is determined by device characterization but is not production tested.

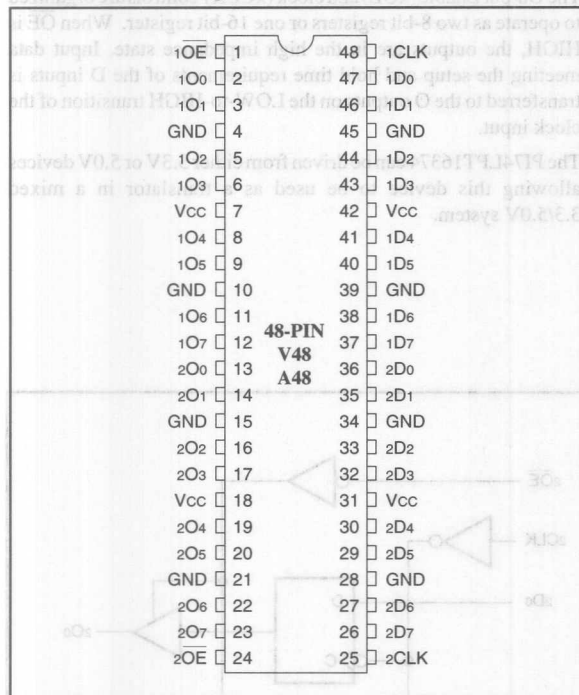
Product Pin Description

Pin Name	Description
xOE	3-State Output Enable Inputs (Active LOW)
xCLK	Clock Inputs
xDx	Data Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Function	Inputs ⁽¹⁾			Outputs ⁽¹⁾
	xDx	xCLK	xOE	xOx
High-Z	X	L	H	Z
	X	H	H	Z
Load	L	↑	L	L
Register	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

Product Pin Configuration



Note:

1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Z = High Impedance

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOU = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	V _{CC} +0.5	V
V _{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max. V _{IN} = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	V _{CC} = Max. V _{IN} = V _{CC}	—	—	±1	μA
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max. V _{IN} = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	V _{CC} = Max. V _{IN} = GND	—	—	±1	μA
IOZH	High Impedance Output Current	V _{CC} = Max. V _{OUT} = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	V _{CC} = Max. V _{OUT} = GND	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. I _{OH} = -0.1 mA	V _{CC} -0.2	—	—	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -3 mA	2.4	3.0	—	V
		V _{CC} = 3.0V, I _{OH} = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -24 mA	2.0	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. I _{OL} = 0.1 mA	—	—	0.2	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 16 mA	—	0.2	0.4	V
		I _{OL} = 24 mA	—	0.3	0.5	V
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-60	-85	-240	mA
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA
V _H	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
ΔI_{CC} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{CP} = Number of Clock Inputs at f_{CP}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

3.3V 16-BIT REGISTER (3-STATE)

6

Notes:

ADVANCE INFORMATION



PI74LPT16501

Fast CMOS 18-Bit Registered Transceivers

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

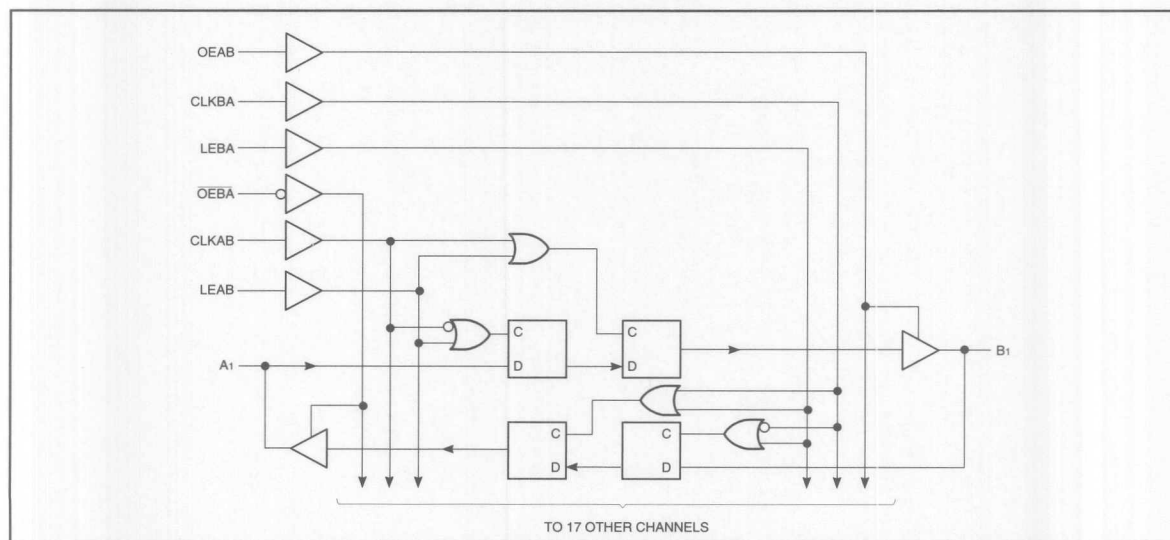
Product Description:

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16501 is an 18-bit registered bus transceiver designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and OEBA), Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using OEBA, LEBA and CLKBA. This high-speed, low power device offers a flow-through organization for ease of board layout.

The PI74LPT16501 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.

Logic Block Diagram



Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
Vcc	Power

Truth Table^(1,4)

Inputs			Outputs	
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B ⁽²⁾
H	L	H	X	B ⁽³⁾

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = High Voltage Level
L = Low Voltage Level
Z = High Impedance
↑ = LOW-to-HIGH Transition

Product Pin Configuration

OEAB	1	56	GND
LEAB	2	55	CLKAB
A0	3	54	B0
GND	4	53	GND
A1	5	52	B1
A2	6	51	B2
VCC	7	50	VCC
A3	8	49	B3
A4	9	48	B4
A5	10	47	B5
GND	11	46	GND
A6	12	45	B6
A7	13	44	B7
A8	14	43	B8
A9	15	42	B9
A10	16	41	B10
A11	17	40	B11
GND	18	39	GND
A12	19	38	B12
A13	20	37	B13
A14	21	36	B14
VCC	22	35	VCC
A15	23	34	B15
A16	24	33	B16
GND	25	32	GND
A17	26	31	B17
OEBA	27	30	CLKBA
LEBA	28	29	GND

ADVANCE INFORMATION

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	VCC-0.2	—	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
ΔI_{CC} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{CP} = Number of Clock Inputs at f_{CP}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Parameter ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	2.5	8	pF

Note: 1. This parameter is determined by device characterization but is not production tested.

PI74LPT16501 Switching Characteristics over Operating Range⁽¹⁾

Parameters			Description	Conditions ⁽²⁾	LPT16501		LPT16501A		LPT16501C		Unit
					Com.		Com.		Com.		
					Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tMAX	CLKAB or CLKBA frequency		CL = 50 pF	—	100	—	150	—	150	MHz	
tPLH tPHL	Propagation Delay Ax to Bx or Ax to Bx			1.5	6.5	1.5	5.1	1.5	4.6	ns	
tPLH tPHL	Propagation Delay LEBA to Ax, LEAB to Bx		RL = 500 Ω	1.5	7.5	1.5	5.6	1.5	4.6	ns	
tPLH tPHL	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	8.0	1.5	5.6	1.5	5.3	ns	
tPZH tPZL	Output Enable Time OEBA to Ax, OEAB to Bx			1.5	8.0	1.5	6.0	1.5	5.6	ns	
tPHZ tPLZ	Output Disable Time ⁽⁴⁾ OEBA to Ax, OEAB to Bx			1.5	7.5	1.5	5.6	1.5	5.2	ns	
tsu	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			4.0	—	3.0	—	3.0	—	ns	
th	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	ns	
tsu	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock HIGH		4.0	—	3.0	—	3.0	—	ns	
		Clock LOW		1.5	—	1.5	—	1.5	—	ns	
th	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	ns	
tw	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾			3.0	—	3.0	—	3.0	—	ns	
tw	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾			3.0	—	3.0	—	3.0	—	ns	
tsk(o)	Output Skew ⁽⁵⁾			—	0.5	—	0.5	—	0.5	ns	

Notes:

- Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Note:

- This parameter is determined by device characterization but is not production tested.



PI74LPT16543

Fast CMOS 16-Bit Latched Transceivers

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

Product Description:

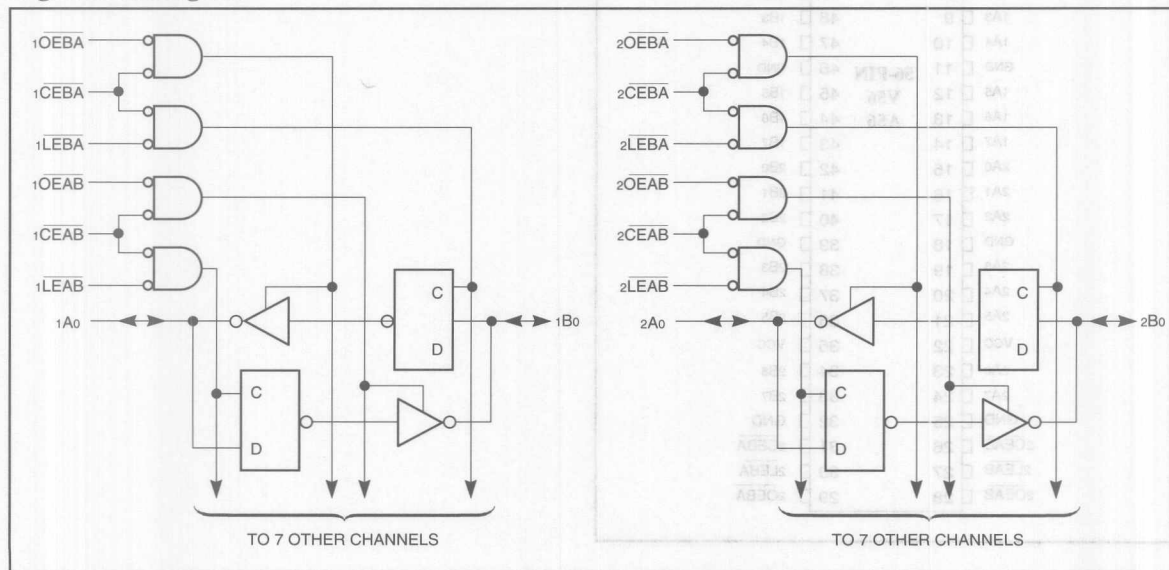
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16543 is 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (xCEAB) input must be LOW in order to enter data from xAx or to take data from xBx, as indicated in the Truth Table. With xCEAB LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the xLEAB signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With xCEAB and xOEAB both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the xCEAB, xLEAB, and xOEAB inputs.

The PI74FCT16543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

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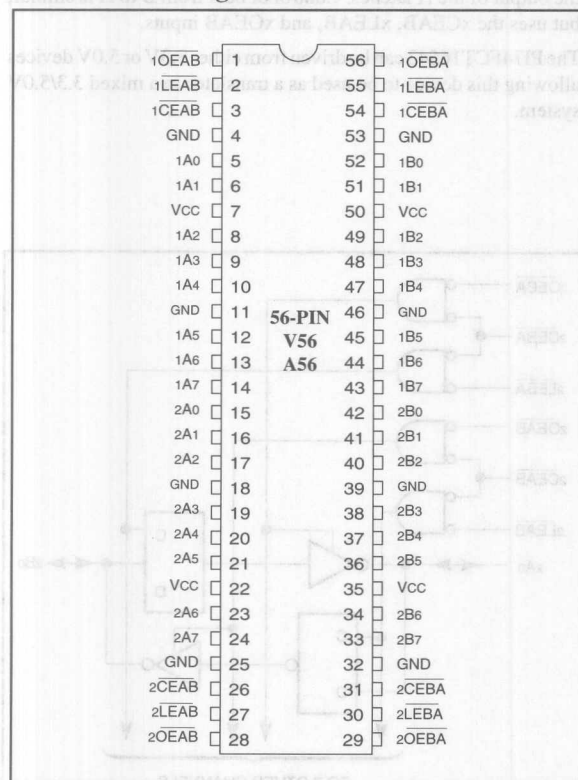
Logic Block Diagram



Product Pin Description

Pin Name	Description
\overline{xOEAB}	A-to-B Output Enable Input (Active LOW)
\overline{xOEBA}	B-to-A Output Enable Input (Active LOW)
\overline{xCEAB}	A-to-B Enable Input (Active LOW)
\overline{xCEBA}	B-to-A Enable Input (Active LOW)
\overline{xLEAB}	A-to-B Latch Enable Input (Active LOW)
\overline{xLEBA}	B-to-A Latch Enable Input (Active LOW)
\overline{xAx}	A-to-B Data Inputs or B-to-A 3-State Outputs
\overline{xBx}	B-to-A Data Inputs or B-to-A 3-State Outputs
GND	Ground
Vcc	Power

Product Pin Configuration

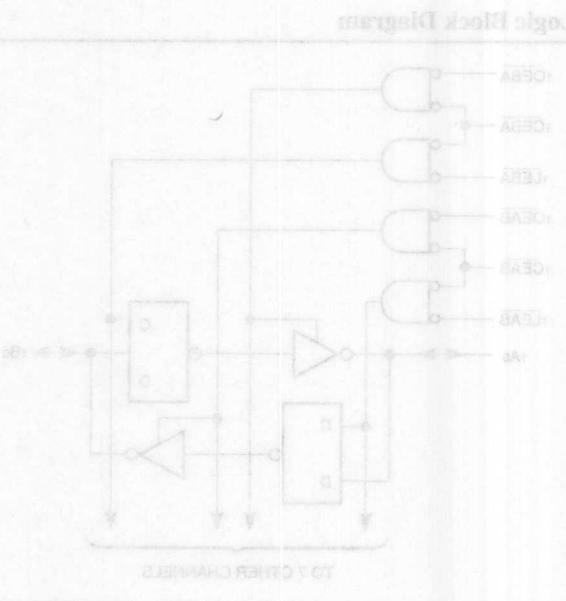


Truth Table⁽¹⁾

Inputs			Latch Status	Output Buffers
\overline{xCEAB}	\overline{xLEAB}	\overline{xOEAB}	\overline{xAx} to \overline{xBx}	\overline{xBx}
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES:

- *Before \overline{xLEAB} LOW-to-HIGH Transition
H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
Z = High Impedance
- A-to-B data flow shown. B-to-A flow control is the same, except using \overline{xCEBA} , \overline{xLEBA} , and \overline{xOEBA} .



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	V _{CC} +0.5	V
V _{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max., V _{IN} = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	V _{CC} = Max., V _{IN} = V _{CC}	—	—	±1	μA
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max., V _{IN} = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	V _{CC} = Max., V _{IN} = GND	—	—	±1	μA
I _{OZH}	High Impedance Output Current	V _{CC} = Max., V _{OUT} = 5.5V	—	—	±1	μA
I _{OZL}	(3-State Output pins)	V _{CC} = Max., V _{OUT} = GND	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA	—	-0.7	-1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -0.1 mA	V _{CC} -0.2	—	—	V
		V _{IN} = V _{IH} or V _{IL} , I _{OH} = -3 mA	2.4	3.0	—	V
		V _{CC} = 3.0V, I _{OH} = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		V _{IN} = V _{IH} or V _{IL} , I _{OH} = -24 mA	2.0	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 0.1 mA	—	—	0.2	V
		V _{IN} = V _{IH} or V _{IL} , I _{OL} = 16 mA	—	0.2	0.4	V
		I _{OL} = 24 mA	—	0.3	0.5	V
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-60	-85	-240	mA
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA
V _H	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{in} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{in} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{in} = V _{cc} V _{in} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{in} = V _{cc} - 0.6V V _{in} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{in} = V _{cc} - 0.6V V _{in} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{cp}/2 + f_i N_i)$
I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccZ})
ΔI_{cc} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{cp} = Number of Clock Inputs at f_{cp}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ²⁾	LPT16543		LPT16543A		LPT16543C		Unit
			Com.		Com.		Com.		
			Min ³⁾	Max	Min ³⁾	Max	Min ³⁾	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	ns
tPHL	Transparent Mode xAx to xBx or xBx to xAx								
tPLH	Propagation Delay		2.5	12.5	2.5	8.0	2.5	7.0	ns
tPHL	xLEBA to xAx, xLEAB to xBx								
tpZH	Output Enable Time		2.0	12.0	2.0	9.0	2.0	8.0	ns
tpZL	xOEBA or xOEAB to xAx or xBx								
tpHZ	Output Disable Time ⁴⁾		2.0	9.0	2.0	7.5	2.0	6.5	ns
tpLZ	xOEBA or xOEAB to xAx or xBx								
tsu	Setup Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		3.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	ns
tw	xLEAB or xLEBA Pulse Width LOW		5.0	—	5.0	—	5.0	—	ns
tsk(o)	Output Skew ⁵⁾		—	0.5	—	0.5	—	0.5	ns

Notes:

- Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOU = 0V	5.5	8	pF

Note:

- This parameter is determined by device characterization but is not production tested.

ADVANCE INFORMATION

Fast CMOS 3.3V 16-Bit Registered Transceivers

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

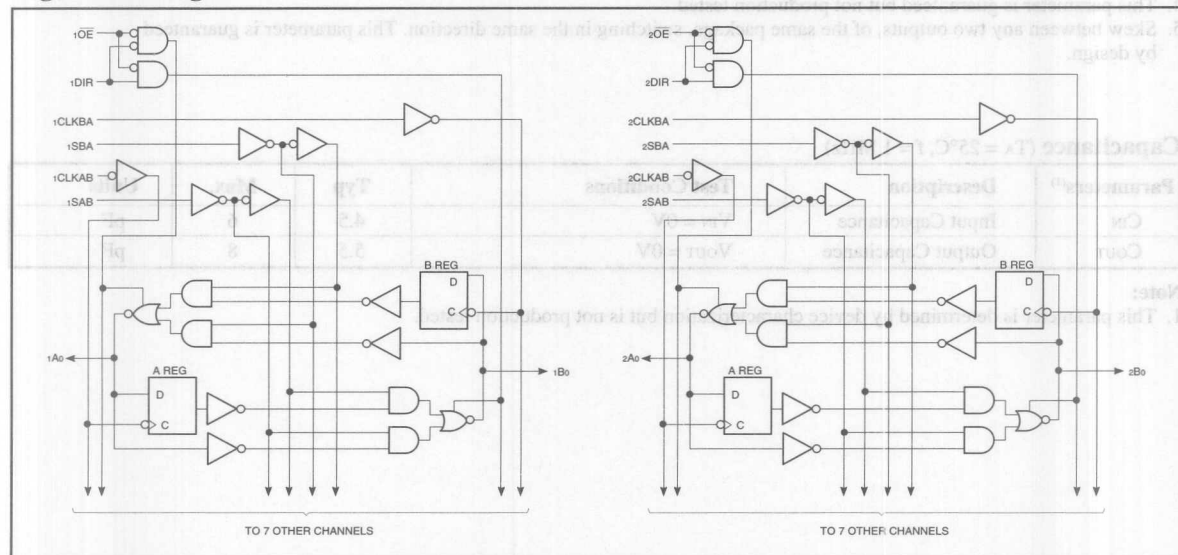
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16646 is a 16-bit registered transceiver organized as two independent 8-bit bus transceivers designed with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable control (xOE) and direction pins (xDIR) to control the transceiver functions. The Select (xSAB and xSBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74LPT16646 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

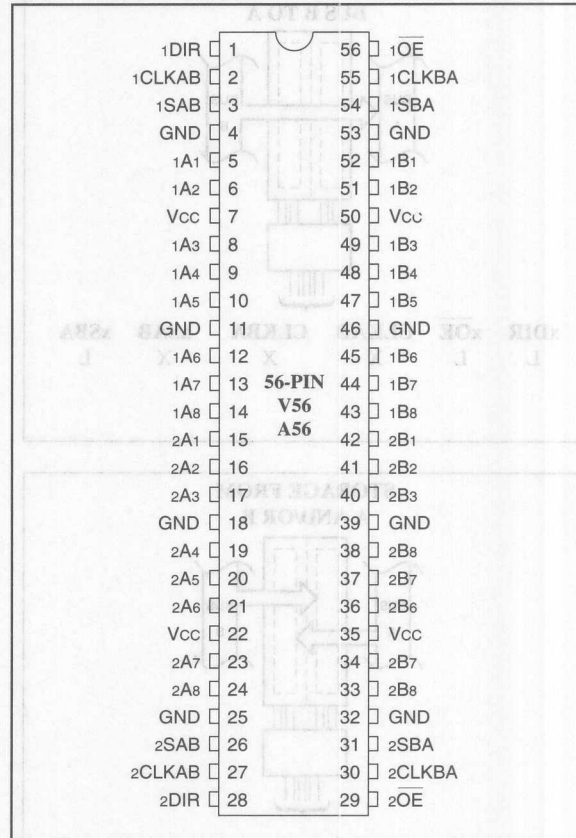
Logic Block Diagram



Product Pin Description

Pin Name	Description
xOE, xDIR	Output Enable Inputs (Active LOW)
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
GND	Ground
Vcc	Power

Product Pin Configuration



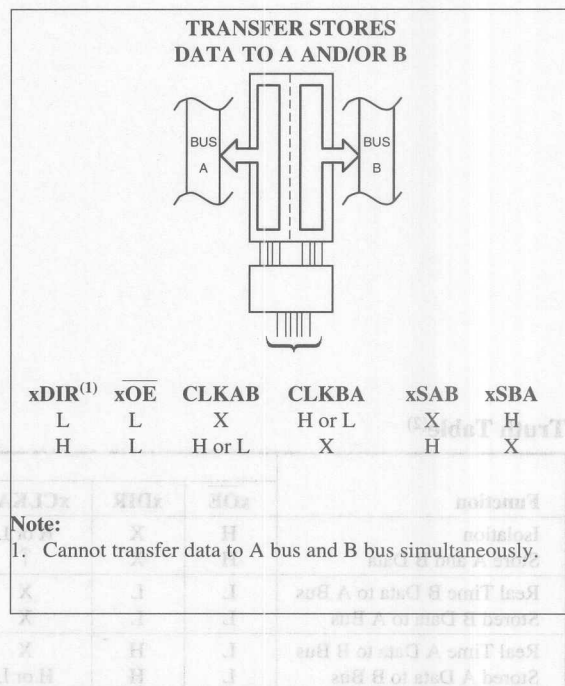
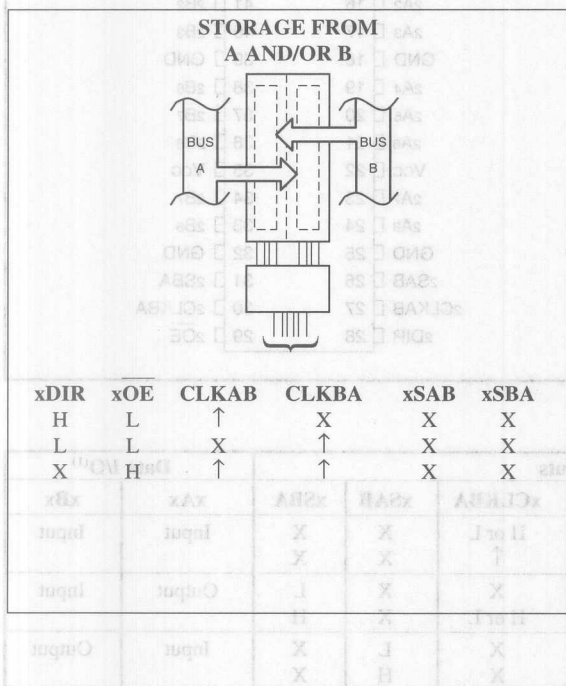
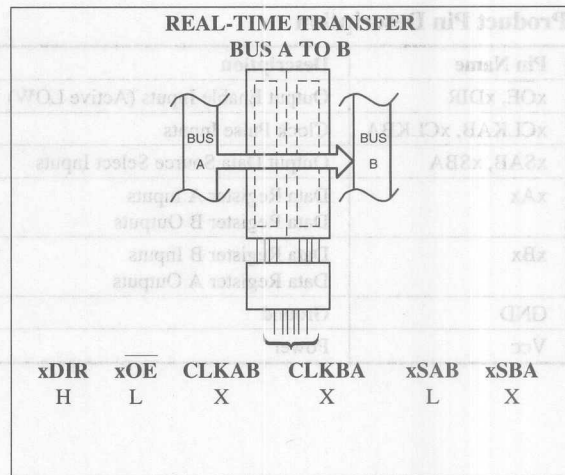
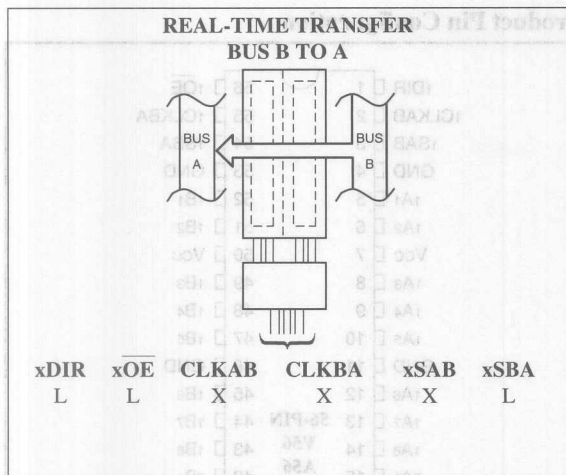
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Truth Table⁽²⁾

Function	Inputs						Data I/O ⁽¹⁾	
	xOE	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

Note:

- The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, ↑ = LOW-to-HIGH Transition



Note:

1. Cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	Vcc = Max., VIN = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	Vcc = Max., VIN = Vcc	—	—	±1	µA
IIL	Input LOW Current (Input pins)	Vcc = Max., VIN = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	Vcc = Max., VIN = GND	—	—	±1	µA
IOZH	High Impedance Output Current	Vcc = Max., VOUT = 5.5V	—	—	±1	µA
IOZL	(3-State Output pins)	Vcc = Max., VOUT = GND	—	—	±1	µA
VIK	Clamp Diode Voltage	Vcc = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	Vcc = Min., IOH = -0.1 mA	Vcc-0.2	—	—	V
		VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		Vcc = 3.0V, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	Vcc = Min., IOL = 0.1 mA	—	—	0.2	V
		VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	Vcc = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	Vcc = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	µA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = Vcc - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccD}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_t + I_{ccD} (f_{cp}/2 + f_i N_i)$
I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccZ})
ΔI_{cc} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_t = Number of TTL Inputs at D_H
I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{cp} = Number of Clock Inputs at f_{cp}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16646		LPT16646A		LPT16646C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH tPHL	Propagation Delay Bus to Bus	C _L = 50 pF R _L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	ns
tpZH tpZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	9.8	1.5	7.8	ns
tpHZ tPLZ	Output Disable Time ⁽⁴⁾ xDIR or xOE to Bus		2.0	9.0	2.0	6.3	1.5	6.3	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width ⁽⁴⁾ HIGH or LOW		6.0	—	5.0	—	5.0	—	ns
tsk(o)	Output Skew ⁽⁵⁾		—	0.5	—	0.5	—	0.5	ns

Notes:

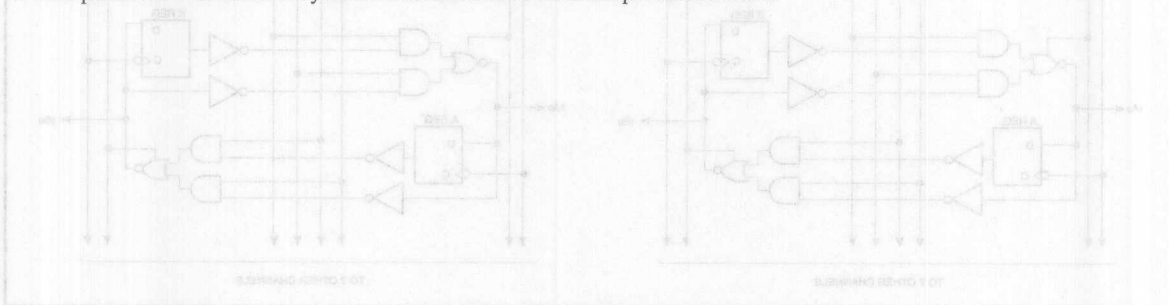
- Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. For $V_{CC} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance ($T_A = 25^\circ C$, $f = 1$ MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
COUT	Output Capacitance	$V_{OUT} = 0V$	5.5	8	pF

Note:

- This parameter is determined by device characterization but is not production tested.





PI74LPT16652

Fast CMOS 16-Bit Registered Transceivers

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

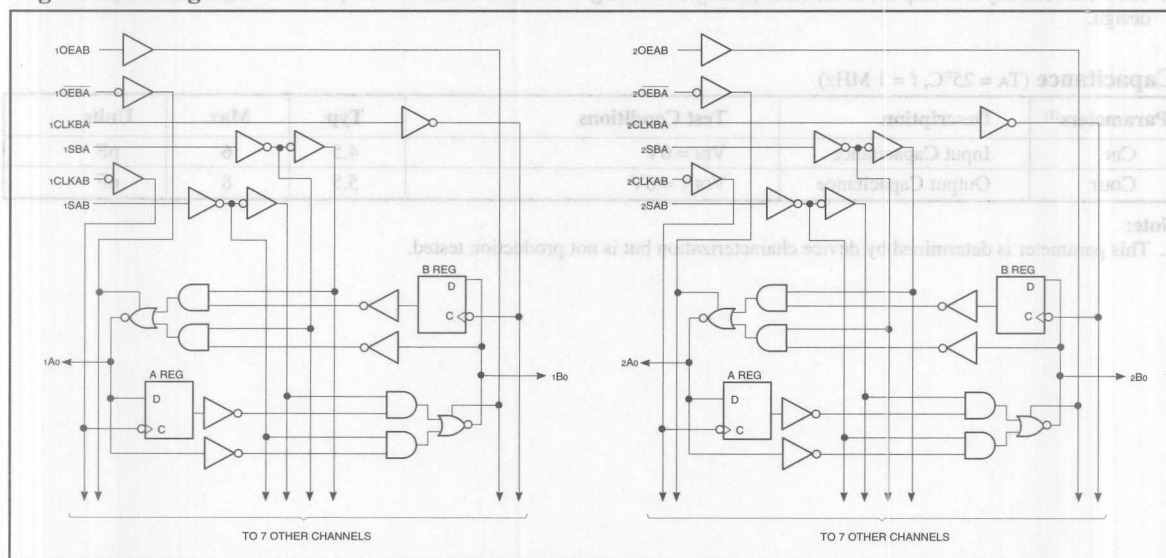
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16652 is 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls (xOEAB and x OEBA) to control the transceiver functions. The Select (xSAB and xSBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74LPT16652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Logic Block Diagram



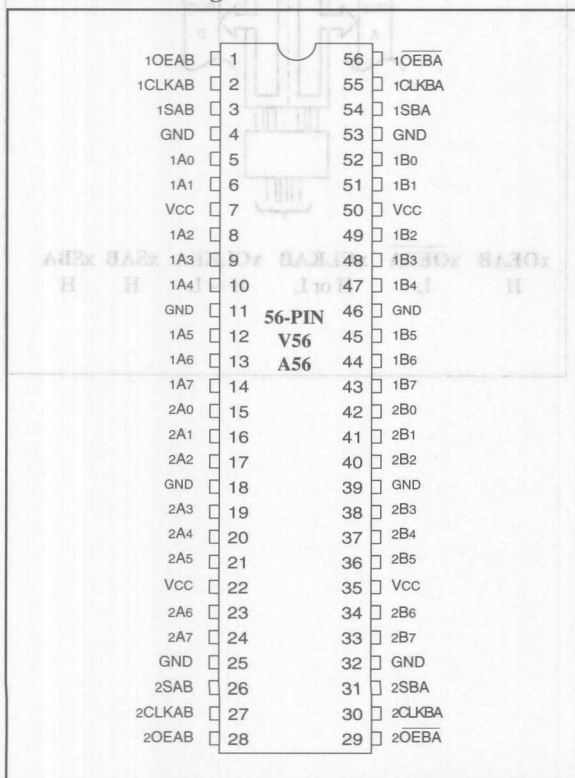
Truth Table

Function/Operation	Inputs						DATA I/O ⁽²⁾	
	xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾
Store A in Both Registers	H	H	↑	↑	X ⁽²⁾	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified ⁽¹⁾	Input
Store B in Both Registers	L	L	↑	↑	X	X ⁽²⁾	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

- The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.
H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition

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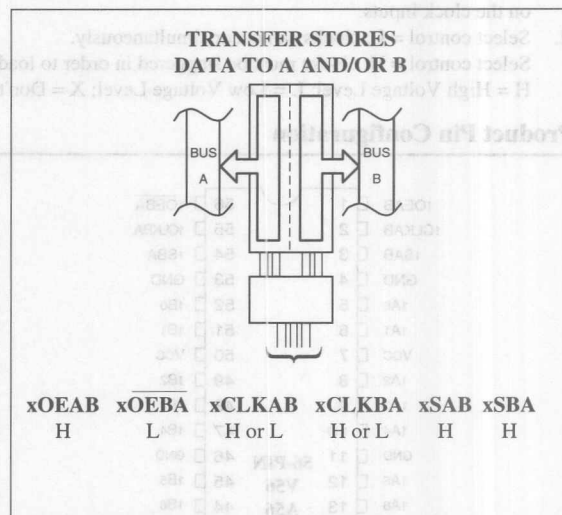
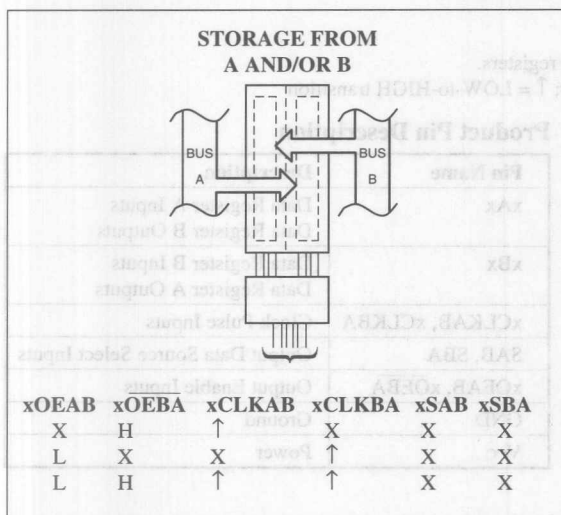
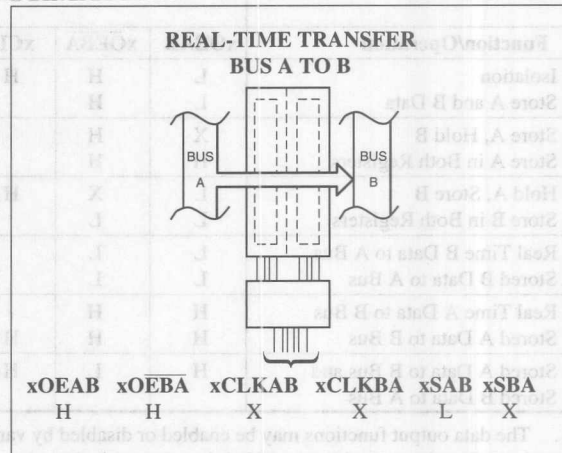
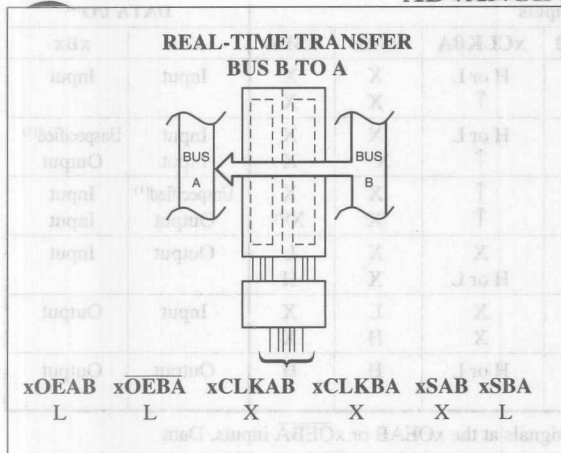
Product Pin Configuration



Product Pin Description

Pin Name	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
xOEAB, xOEBA	Output Enable Inputs
GND	Ground
Vcc	Power

ADVANCE INFORMATION



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	VCC-0.2	—	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccD}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_c = I_{cc} + \Delta I_{cc} D_H N_t + I_{ccD} (f_{cp}/2 + f_i N_i)$
I_{cc} = Quiescent Current (I_{ccL}, I_{ccH} and I_{ccZ})
ΔI_{cc} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_t = Number of TTL Inputs at D_H
I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{cp} = Number of Clock Inputs at f_{cp}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16652		LPT16652A		LPT16652C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	ns
tPHL	Bus to Bus								
tPZH	Output Enable Time	xOEAB or xOEBA to Bus	2.0	14.0	2.0	9.8	1.5	7.8	ns
tPZL	xOEAB or xOEBA to Bus								
tPHZ	Output Disable Time ⁽⁴⁾	xOEAB or xOEBA to Bus	2.0	9.0	2.0	6.3	1.5	6.3	ns
tPLZ	xOEAB or xOEBA to Bus								
tPLH	Propagation Delay	Clock to Bus	2.0	9.0	2.0	6.3	1.5	5.7	ns
tPHL	Clock to Bus								
tPLH	Propagation Delay	xSBA or xSAB to Bus	2.0	11.0	2.0	7.7	1.5	6.2	ns
tPHL	xSBA or xSAB to Bus								
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width ⁽⁴⁾ HIGH or LOW		6.0	—	5.0	—	5.0	—	ns
tsk(o)	Output Skew ⁽⁵⁾		—	0.5	—	0.5	—	0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

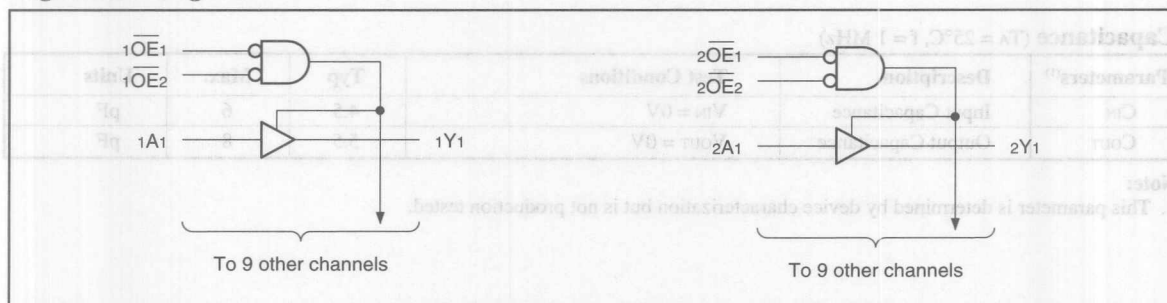
Product Description:

- Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16827 is a 20-bit wide bus driver designed to provide buffering and high-performance bus interfacing for wide data/address paths or busses with parity. Two pair of nanded output enable controls allow the device to be operated as two 10-bit buffers or as one 20-bit buffer. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The PI74LPT16827 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Logic Block Diagram



Product Pin Configuration

1OE1	1	56	1OE2
1Y1	2	55	1A1
1Y2	3	54	1A2
GND	4	53	GND
1Y3	5	52	1A3
1Y4	6	51	1A4
Vcc	7	50	Vcc
1Y5	8	49	1A5
1Y6	9	48	1A6
1Y7	10	47	1A7
GND	11	46	GND
1Y8	12	45	1A8
1Y9	13	44	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
GND	18	39	GND
2Y4	19	38	2A4
2Y5	20	37	2A5
2Y6	21	36	2A6
Vcc	22	35	Vcc
2Y7	23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9	26	31	2A9
2Y10	27	30	2A10
2OE1	28	29	2OE2

Product Pin Description

Pin Name	Description
xOEx	Output Enable Inputs (Active LOW)
xAx	Data Inputs
XYx	3-State Outputs

Truth Table(1)

Inputs			Outputs
xOE1	xOE2	xAx	XYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	μA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	μA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	μA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	Vcc-0.2	—	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	μA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = Vcc - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

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Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- $$I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_c = I_{\text{cc}} + \Delta I_{\text{cc}} D_H N_T + I_{\text{ccd}} (f_{\text{CP}}/2 + f_i N_i)$$

$$I_{\text{cc}} = \text{Quiescent Current (Iccl, Icch and Iccz)}$$

$$\Delta I_{\text{cc}} = \text{Power Supply Current for a TTL High Input}$$

$$D_H = \text{Duty Cycle for TTL Inputs High}$$

$$N_T = \text{Number of TTL Inputs at } D_H$$

$$I_{\text{ccd}} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$$

$$f_{\text{CP}} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$$

$$N_{\text{CP}} = \text{Number of Clock Inputs at } f_{\text{CP}}$$

$$f_i = \text{Input Frequency}$$

$$N_i = \text{Number of Inputs at } f_i$$

All currents are in milliamps and all frequencies are in megahertz.

ADVANCE INFORMATION

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16827A		LPT16827B		LPT16827C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
t _{PLH} t _{PHL}	Propagation Delay DN to Y _N	C _L = 50 pF R _L = 500Ω	1.5	6.5	1.5	5.0	1.5	4.4	ns
		C _L = 300 pF ⁽⁴⁾ R _L = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	ns
t _{PZH} t _{PZL}	Output Enable Time O _{EN} to Y _N	C _L = 50 pF R _L = 500Ω	1.5	9.5	1.5	8.0	1.5	7.0	ns
		C _L = 300 pF ⁽⁴⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽⁴⁾ O _{EN} to Y _N	C _L = 5 pF ⁽⁴⁾ R _L = 500Ω	1.5	8.5	1.5	6.0	1.5	5.7	ns
		C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns
t _{SK} (o)	Output Skew ⁽⁵⁾		—	0.5	—	0.5	—	0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.



PI74LPT16952

Fast CMOS 3.3V 16-Bit Registered Transceivers

Product Features:

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
 - Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A56)
 - 56-pin 300 mil wide plastic SSOP (V56)

Product Description:

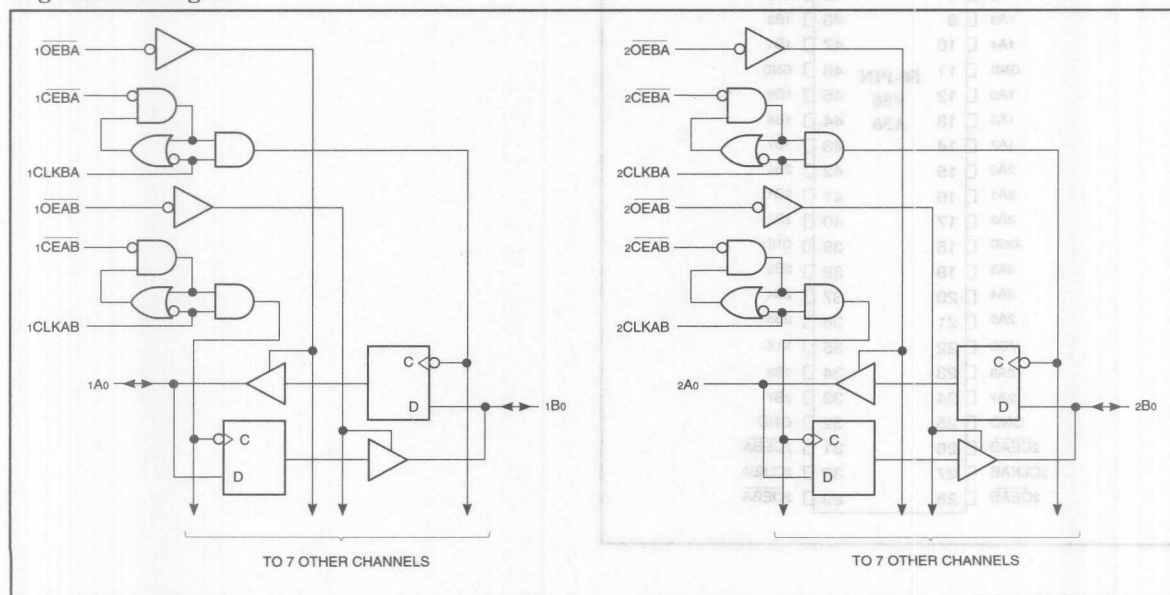
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16952 is a 16-bit registered transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (xCEAB) input must be LOW in order to enter data from xAx. The data present on the A port will be clocked on the B register when xCLKAB toggles from LOW-to-HIGH. The xOEAB control performs the output enable function on the B port. Control of data from B to A is similar, but uses the xCEAB, xCLKAB, and xOEAB inputs. By connecting the control pins of the two independent transceivers together, a full 16-bit operation can be achieved. The output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74LPT16952 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

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Logic Block Diagram



Product Pin Description

Pin Name	Description
xOEAB	A-to-B Output Enable Input (Active LOW)
xOEBA	B-to-A Output Enable Input (Active LOW)
xCEAB	A-to-B Clock Enable Input (Active LOW)
xCEBA	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or B-to-A 3-State Outputs
GND	Ground
Vcc	Power

Truth Table^(1,2)

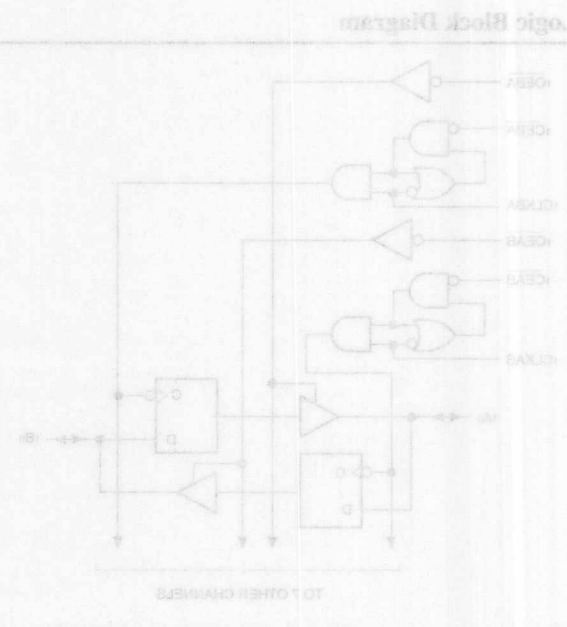
Inputs				Outputs
xCEAB	xCLKAB	xOEAB	xAx	xBx
H	X	L	X	B ⁽³⁾
X	L	L	X	B ⁽³⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	High Z

NOTES:

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
↑ = LOW-to-HIGH Transition
Z = High Impedance
- A-to-B data flow shown. B-to-A flow control is the same, except using xCEBA, xCLKBA, and xOEBA.
- Level of B before the indicated steady-state input conditions were established.

Product Pin Configuration

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A0	5	52	1B0
1A1	6	51	1B1
VCC	7	50	VCC
1A2	8	49	1B2
1A3	9	48	1B3
1A4	10	47	1B4
GND	11	46	GND
1A5	12	45	1B5
1A6	13	44	1B6
1A7	14	43	1B7
2A0	15	42	2B0
2A1	16	41	2B1
2A2	17	40	2B2
GND	18	39	GND
2A3	19	38	2B3
2A4	20	37	2B4
2A5	21	36	2B5
VCC	22	35	VCC
2A6	23	34	2B6
2A7	24	33	2B7
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level	2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)		2.0	—	Vcc+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max., VIN = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	VCC = Max., VIN = VCC	—	—	±1	µA
IIL	Input LOW Current (Input pins)	VCC = Max., VIN = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	VCC = Max., VIN = GND	—	—	±1	µA
IOZH	High Impedance Output Current	VCC = Max., VOUT = 5.5V	—	—	±1	µA
IOZL	(3-State Output pins)	VCC = Max., VOUT = GND	—	—	±1	µA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA	—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, Vo = 1.5V ⁽³⁾	-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, Vo = 1.5V ⁽³⁾	50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL, IOH = -0.1 mA	Vcc-0.2	—	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -3 mA	2.4	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -8 mA	2.4 ⁽⁶⁾	3.0	—	V
		VCC = 3.0V, VIN = VIH or VIL, IOH = -24 mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL, IOL = 0.1 mA	—	—	0.2	V
		VCC = Min., VIN = VIH or VIL, IOL = 16 mA	—	0.2	0.4	V
		VCC = Min., VIN = VIH or VIL, IOL = 24 mA	—	0.3	0.5	V
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-85	-240	mA
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V	—	—	±100	µA
VH	Input Hysteresis		—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	10	μA
ΔI _{cc}	Quiescent Power Supply Current TTL Inputs HIGH	V _{cc} = Max.	V _{IN} = V _{cc} - 0.6V ⁽³⁾		2.0	30	μA
I _{ccd}	Dynamic Power Supply ⁽⁴⁾	V _{cc} = Max., Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		50	75	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle xOE = GND One Bit Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle xOE = GND 16 Bits Toggling	V _{IN} = V _{cc} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	mA

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{cp}/2 + f_i N_i)$$

I_{cc} = Quiescent Current (I_{ccl}, I_{ccch} and I_{ccd})
ΔI_{cc} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{cp} = Number of Clock Inputs at f_{cp}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamperes and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16952A		LPT16952B		LPT16952C		Unit
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
t _{PLH} t _{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C _L = 50 pF R _L = 500	2.0	10.0	2.0	7.5	2.0	6.3	ns
t _{PZH} t _{PZL}	Output Enable Time xOEBA, xOEAB to xAx, xBx		1.5	10.5	1.5	8.0	1.5	7.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽⁴⁾ xOEBA, xOEAB to xAx, xBx		1.5	10.0	1.5	7.5	1.5	6.5	ns
t _{SU}	Set-up Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	ns
t _H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	ns
t _{SU}	Setup Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	ns
t _H	Hold Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	ns
t _W	Pulse Width HIGH ⁽⁴⁾ or LOW, xCLKAB or xCLKBA		3.0	—	3.0	—	3.0	—	ns
t _{SK(o)}	Output Skew ⁽⁵⁾		—	0.5	—	0.5	—	0.5	ns

Notes:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

GENERAL INFORMATION**1****STANDARD AND 25Ω OUTPUT RESISTOR SERIES
5V FCT LOGIC PRODUCTS****2****DOUBLE DENSITY STANDARD
5V FCT LOGIC PRODUCTS****3****DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS****4****STANDARD 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****5****DOUBLE DENSITY 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****6****SPECIALTY LOGIC PRODUCTS****7****BUS SWITCH PRODUCTS****8****CLOCK DISTRIBUTION PRODUCTS****9****CLOCK GENERATOR PRODUCTS****10****NETWORKING PRODUCTS****11****APPLICATION NOTES****12****QUALITY AND RELIABILITY INFORMATION****13****PACKAGE MECHANICAL OUTLINES****14****SALES AND DISTRIBUTION LOCATIONS****15**

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Part Number	Description	Page No.
PI6M1010T	SIMM Decoder Chip	7.1



PI6M1010T

SIMM DECODER CHIP

Product Features

- Uses the half-working DRAM chips to build fully functional 30-pin and 72-pin DRAM simm modules.
- Integrates all the logic required by a simm module using half-working DRAM chips.
- Provides the decoder logic to increase the memory capacity on a simm module.
- Universal decoder chip for most DRAM simm module part types
—No PAL/GAL programming.
- Maximum propagation delay of 9 ns, 5.7 ns, and 4.9 ns speed grades
—Higher performance than PAL/GAL.
- Low cost solution
— Lower cost than PAL/GAL
- Small 16-pin 150-mil wide SOIC (W16), QSOP (Q16), and 20-pin TQSOP (R20) packages
—Smaller and thinner space than PAL/GAL
- Low noise, Low power
— Lower noise and lower power than PAL/GAL
- Design supports: Provides Turn-Key Manufacturing packages of selected DRAM simm modules for quick-to-market high-volume production of simm products.

General Description

As the memory capacity of a DRAM chip keeps increasing from 1 Megabits to 4 Megabits, 16 Megabits and beyond, the chance of bad bits on a DRAM chip during its manufacturing process also exponentially increases. As a result, the number of half-working chips, which have one-half capacity working and the other half capacity failing, is ever increasing. The half-working chips are normally treated as rejected parts. The PI6M1010T Simm Decoder chip is developed to use such partially working parts to build a fully functional DRAM simm module.

The PI6M1010T Simm Decoder chip provides a low cost solution for DRAM simm module applications. It integrates all the logic needed by a simm module which uses the low cost half-working DRAM chips. For example, a 1M x 8 simm module uses four half-working 1M x 4 DRAM chips plus PI6M1010T, as compared with two fully functional 1M x 4 DRAM chips without using the PI6M1010T decoder.

It can be also used to increase the memory capacity of a simm module when fully functional DRAM chips are used. A 1M x 8 simm module using two fully functional 1M x 4 DRAM chips, for example, can be expanded to a 2M x 8 simm module using four fully functional 1M x 4 DRAM chips plus the PI6M1010T.

The PI6M1010T chip is a universal logic chip to build any of the examples of supported DRAM modules. No PAL/GAL programming is needed for each individual simm module type. It also provides high-speed, high-drive, and low noise outputs to meet all the tight timing, heavy driving, and low noise requirements of simm modules.

Performance of Simm Modules Using Pericom Decoder Chip

A simm module using fully functional DRAM chips typically does not need any decoding logic circuit. In this case, the speed of a simm module is the same as the speed of the DRAM chips.

A simm module using half-working DRAM chips, however, needs a decoder logic, typically using 10 ns PAL or GAL, which results in DRAM speed degradation. In this case, the simm module speed will be typically 10 ns slower than the DRAM speed. The Pericom PI6M1010T decoder chip is designed to eliminate such DRAM speed degradation and achieves the highest performance. A simm module using PI6M1010T runs at the same speed as its DRAM chips.

Examples of Supported DRAM Modules

Configuration No.	Module Description	If Fully Functional DRAM Chips are Used: No. of Chips, Chip Capacity	If Half-working DRAM Chips are used: No. of Chips, Chip Capacity, High (H) or Low (L) Half-working Chips
1.1	1M x 8, 1M x 4-based	(2) 1M x 4 chips	(4) 1M x 4 (H) chips + M1010
1.2	1M x 8, 1M x 4-based	(2) 1M x 4 chips	(4) 1M x 4 (L) chips + M1010
1.3	1M x 9, 1M x 4-based	(2) 1M x 4 chips + 1M x 1 chip	(4) 1M x 4 (H) chips + M1010 + 1M x 1 chip
1.4	1M x 9, 1M x 4-based	(2) 1M x 4 chips + 1M x 1 chip	(4) 1M x 4 (L) chips + M1010 + 1M x 1 chip
2.1	2M x 8, 1M x 4-based	(4) 1M x 4 chips + M1010	
2.2	2M x 9, 1M x 4-based	(4) 1M x 4 chips + M1010 + 1M x 1 chip	
3.1	4M x 8, 4M x 4-based	(2) 4M x 4 chips	(4) 4M x 4 (H) chips + M1010
3.2	4M x 8, 4M x 4-based	(2) 4M x 4 chips	(4) 4M x 4 (L) chips + M1010
3.3	4M x 9, 4M x 4-based	(2) 4M x 4 chips + 4M x 1 chip	(4) 4M x 4 (H) chips + M1010 + 4M x 1 chip
3.4	4M x 9, 4M x 4-based	(2) 4M x 4 chips + 4M x 1 chip	(4) 4M x 4 (L) chips + M1010 + 4M x 1 chip
4.1	8M x 8, 4M x 4-based	(4) 4M x 4 chips + M1010	
4.2	8M x 9, 4M x 4-based	(4) 4M x 4 chips + M1010 + (2) 4M x 1 chips	
5.1	1M x 32, 1M x 4-based	(8) 1M x 4 chips	(16) 1M x 4 (H) chips + M1010
5.2	1M x 32, 1M x 4-based	(8) 1M x 4 chips	(16) 1M x 4 (L) chips + M1010
5.3	1M x 36, 1M x 4-based	(8) 1M x 4 chips + (4) 1M x 1 chips	(16) 1M x 4 (H) chips + (4) 1M x 1 chips + M1010
5.4	1M x 36, 1M x 4-based	(8) 1M x 4 chips + (4) 1M x 1 chips	(16) 1M x 4 (L) chips + (4) 1M x 1 chips + M1010
5.5	1M x 36, 1M x 18-based	(2) 1M x 18 chips	(4) 1M x 18 (H) chips + M1010
5.6	1M x 36, 1M x 18-based	(2) 1M x 18 chips	(4) 1M x 18 (L) chips + M1010
6.1	4M x 32, 4M x 4-based	(8) 4M x 4 chips	(16) 4M x 4 (H) chips + M1010
6.2	4M x 32, 4M x 4-based	(8) 4M x 4 chips	(16) 4M x 4 (L) chips + M1010
6.3	4M x 36, 4M x 4-based	(8) 4M x 4 chips + (4) 4M x 1 chips	(16) 4M x 4 (H) chips + (4) 4M x 1 chips + M1010
6.4	4M x 36, 4M x 4-based	(8) 4M x 4 chips + (4) 4M x 1 chips	(16) 4M x 4 (L) chips + (4) 4M x 1 chips + M1010

Product Pin Configuration

Packages Available:

- 16-pin, 150 mil wide, 50 mil pin pitch, plastic SOIC (W16)
- 16-pin, 150 mil wide, 25 mil pin pitch, plastic QSOP (Q16)

WE	1	16	VCC
RAS0	2	15	RAS0B
CAS0	3	14	RAS0A
UAIN	4	13	RAS2B
CAS1	5	12	RAS2A
CAS2	6	11	UAOUT
CAS3	7	10	SELHI
GND	8	9	RAS2

Product Pin Configuration

Packages Available:

- 20-pin, 150 mil wide, 25 mil pin pitch, plastic TQSOP, 1.1 mm height (R20)

NC	1	20	NC
WE	2	19	VCC
RAS0	3	18	RAS0B
CAS0	4	17	RAS0A
UAIN	5	16	RAS2B
CAS1	6	15	RAS2A
CAS2	7	14	UAOUT
CAS3	8	13	SELHI
GND	9	12	RAS2
NC	10	11	NC

Pin Description

Pin Name	W16 and Q16 Pin Number	R20 Pin Number	Pin Type	Description
WE	1	2	Input	Write Enable Input, Active LOW
RAS0	2	3	Input	RAS0, Input, Active LOW
CAS0	3	4	Input	CAS0 Input, Active LOW
UAIN	4	5	Input	Upper Most Address Bit Input
CAS1	5	6	Input	CAS1 Input, Active LOW
CAS2	6	7	Input	CAS2 Input, Active LOW
CAS3	7	8	Input	CAS3 Input, Active LOW
GND	8	9	—	Ground
RAS2	9	12	Input	RAS2 Input, Active LOW
SELHI	10	13	Input	Select Upper-Half Working DRAM Chips
UAOUT	11	14	Output	Upper Most Address Bit Output
RAS2A	12	15	Output	RAS2 Output for Bank A, Active LOW
RAS2B	13	16	Output	RAS2 Output for Bank B, Active LOW
RAS0A	14	17	Output	RAS0 Output for Bank A, Active LOW
RAS0B	15	18	Output	RAS0 Output for Bank B, Active LOW
Vcc	16	19	—	Power Supply, +5V
		1, 10, 11, 20	—	No Connection

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -15.0\text{ mA}$	2.4	3.3		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 12\text{ mA}$ Device with 25Ω Internal Series Resistor		0.3	0.55	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 2.7\text{V}$			5	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = 0.5\text{V}$			-5	μA
I_I	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC} (\text{Max.})$			20	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_{OUT} = \text{GND}$	-60	-120	-300	mA
V_H	Input Hysteresis			200		mV

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

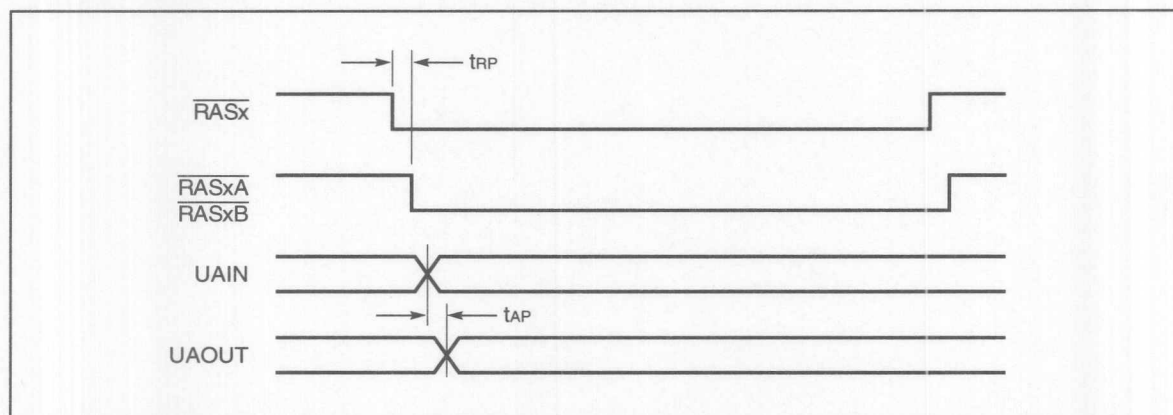
Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Switching Characteristics over Operating Range ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

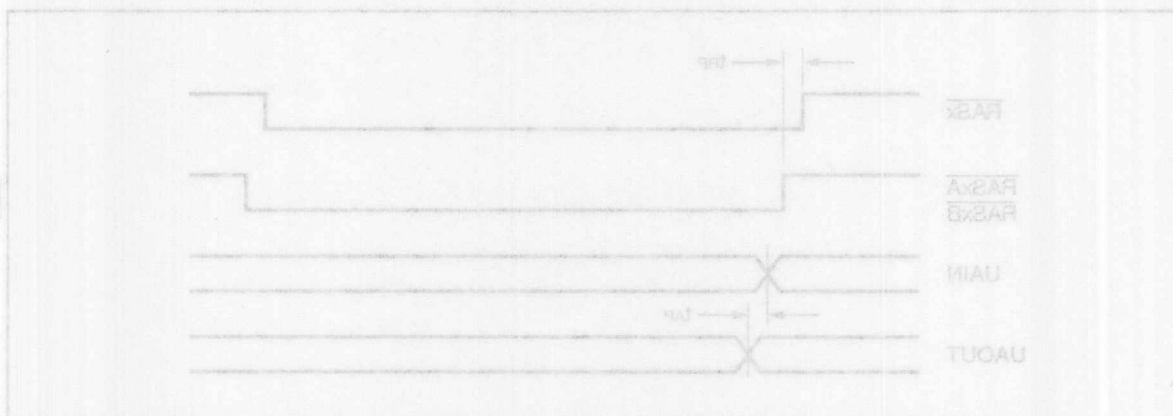
Parameters	Description	Conditions	M1010T		M1010AT		M1010CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
t _{RP}	Propagation Delay RASx Input to RASxA or RASxB Output	CL = 50 pF RL = 500Ω	—	9.0	—	5.7	—	4.9	ns
t _{AP}	Propagation Delay UAIN Input to UAOUT Output		—	9.0	—	5.4	—	4.6	ns

Switching Waveforms


Switching Characteristics over Operating Range ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 2.0\text{V} \pm 5\%$)

Parameters	Description	Conditions	M1010T		M1010AT		M1010CT	
			Min	Max	Min	Max	Min	Max
t _{AP}	Propagation Delay R _{AS} input to R _{AS} A or R _{AS} B Output	C _L = 50 pF R _L = 50Ω	—	9.0	—	5.7	—	4.9
	Propagation Delay U _{AIN} input to U _{AOUT} Output		—	9.0	—	5.4	—	4.5

Switching Waveforms



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Quad Analog Switch with Individual Enables

Product Features:

- Near zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μ A Typical) – Ideally suited for notebook applications
- Packages available:
 - 14-pin 150 mil wide plastic SOIC (W14)
 - 16-pin 150 mil wide plastic QSOP (Q16)

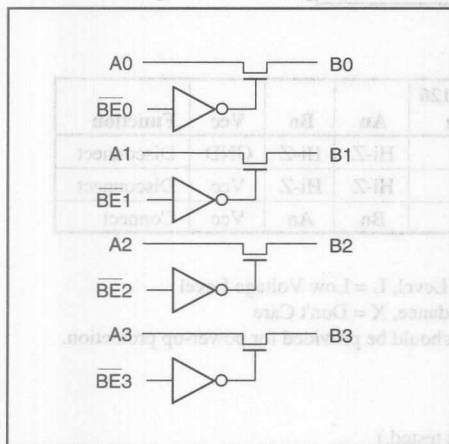
Product Description:

Pericom Semiconductor's PI5C series of logic circuits are produced using the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

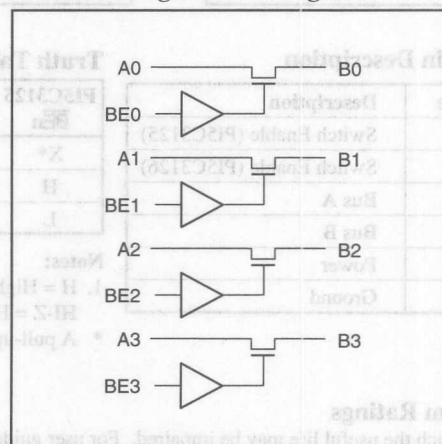
The PI5C3125 and PI5C3126 are quad analog and digital switches designed with four individual 5Ω bus switches with fast individual enables in an industry standard 74XX125/126 pinout. When enabled via the associated Bus Enable (\overline{BE}) pin, the "A" pin is directly connected to the "B" pin for that particular gate. The bus switch introduces no additional propagation delay or additional ground bounce noise.

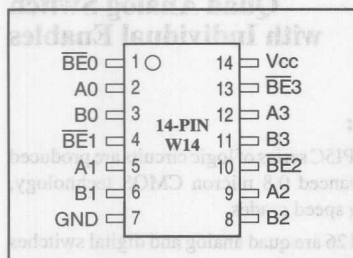
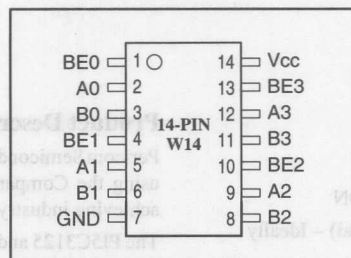
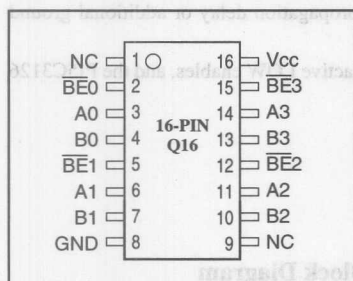
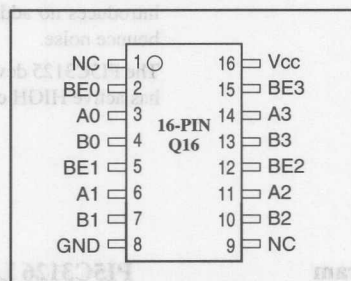
The PI5C3125 device has active LOW enables, and the PI5C3126 has active HIGH enables.

PI5C3125 Logic Block Diagram



PI5C3126 Logic Block Diagram



PI5C3125 14-Pin
Product Configuration

PI5C3126 14-Pin
Product Configuration

PI5C3125 16-Pin
Product Configuration

PI5C3126 16-Pin
Product Configuration

Product Pin Description

Pin Name	Description
\overline{BE}_n	Switch Enable (PI5C3125)
BE_n	Switch Enable (PI5C3126)
A3-A0	Bus A
B3-B0	Bus B
Vcc	Power
GND	Ground

Truth Table⁽¹⁾

PI5C3125 \overline{BE}_n	PI5C3126 BE_n	A _n	B _n	Vcc	Function
X*	X	Hi-Z	Hi-Z	GND	Disconnect
H	L	Hi-Z	Hi-Z	Vcc	Disconnect
L	H	B _n	A _n	Vcc	Connect

Notes:

- H = High Voltage Level, L = Low Voltage Level
 Hi-Z = High Impedance, X = Don't Care

* A pull-up resistor should be provided for power-up protection.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$			± 1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$			± 1	μA
I_{OZH}	High Impedance Output Current	$0 \leq A, B \leq V_{CC}$			± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current ⁽³⁾	$A (B) = 0 \text{ V}, B (A) = V_{CC}$	100			mA
V_H	Input Hysteresis at Control Pins			150		mV
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0V, I_{ON} = 48 \text{ mA}$ $V_{CC} = \text{Min.}, V_{IN} = 2.4V, I_{ON} = 15 \text{ mA}$		5 10	7 15	Ω

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OFF}	A/B Capacitance, Switch Off	$V_{IN} = 0V$		6	pF
C_{ON}	A/B Capacitance, Switch On	$V_{IN} = 0V$		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A, B) pins.
- This parameter is determined by device characterization but is not production tested.

8
Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		0.1	3.0	μA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$			2.5	mA
I_{CCD}	Supply Current per Input per MHz ⁽⁴⁾	$V_{CC} = \text{Max.},$ A and B Pins Open $\overline{BEN}/BEN = \text{GND}$ Control Input Toggling 50% Duty Cycle			0.25	mA/ MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$, control inputs only); A and B pins do not contribute to I_{CC} .
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

PI5C3125 Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PI5C3125 Com.		Unit
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω		0.25	ns
tPHL	A to B, B to A				
tpZH	Bus Enable Time		0.5	6.6	ns
tpZL					
tpHZ	Bus Disable Time		0.5	6.0	ns
tpLZ					

PI5C3126 Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PI5C3126 Com.		Unit
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω		0.25	ns
tPHL	A to B, B to A				
tpZH	Bus Enable Time		0.5	6.6	ns
tpZL					
tpHZ	Bus Disable Time		0.5	6.0	ns
tpLZ					

Notes:

1. See test circuit and wave forms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Bus Switch Buffer

Product Features:

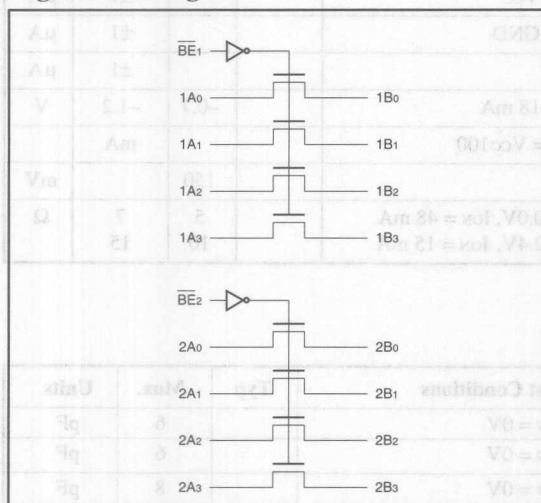
- Near zero propagation delay
- 5Ω switches connect inputs to outputs when enabled
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power ($0.2\ \mu\text{A}$ Typical) – Ideally suited for notebook applications
- Pin compatible with PI74FCT244T
- Packages available:
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

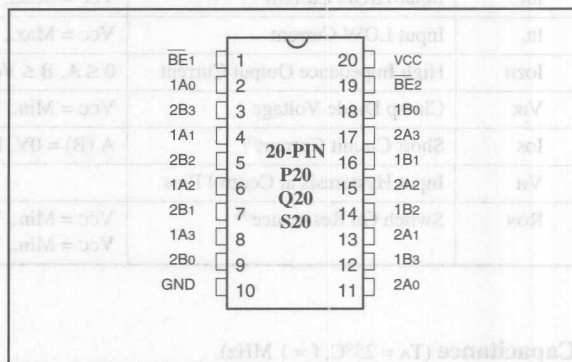
Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3244 features a set of eight bus switches which is pinout and function compatible with the PI74FCT244T, 74F244, and 74ALS/AS/LS 244 8-bit drivers. Two enable signals ($\overline{\text{BEn}}$) turn the switches on similar to the enable signals of the 244. The bus switch creates no additional propagation delay or ground bounce noise.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{\text{BEn}}$	Bus Output Enable (Active LOW)
A0-A3	Bus A
B0-B3	Bus B
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

$\overline{\text{BE1}}$	$\overline{\text{BE2}}$	1A, 1B	2A, 2B
H	H	Disconnect	Disconnect
L	H	1A = 1B	Disconnect
H	L	Disconnect	2A = 2B
L	L	1A = 1B	2A = 2B

NOTE: 1. H = High Voltage Level
L = Low Voltage Level

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$			± 1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$			± 1	μA
I_{OZH}	High Impedance Output Current	$0 \leq A, B \leq V_{CC}$			± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current ⁽³⁾	$A (B) = 0V, B (A) = V_{CC} 100$			mA	
V_H	Input Hysteresis at Control Pins			150		mV
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0V, I_{ON} = 48 \text{ mA}$ $V_{CC} = \text{Min.}, V_{IN} = 2.4V, I_{ON} = 15 \text{ mA}$		5 10	7 15	Ω

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OFF}	A/B Capacitance, Switch Off	$V_{IN} = 0V$		6	pF
C_{ON}	A/B Capacitance, Switch On	$V_{IN} = 0V$		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	3.0	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., A and B Pins Open BE1 or BE2 = GND Control Input Toggling 50% Duty Cycle				0.25	mA/ MHz

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{cc} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{cc}.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PISC3244		Unit
			Com.		
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω		0.25	ns
tPHL	Ax to Bx				
tPZH	Bus Enable Time		1.5	5.6	ns
tPZL	B̄Ex to Ax or Bx				
tPHZ	Bus Disable Time		1.5	5.2	ns
tPLZ	B̄Ex to Ax or Bx				

Notes:

1. See test circuit and wave forms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.



PI5C3245

8-Bit, 2-Port Bus Switch

Product Features:

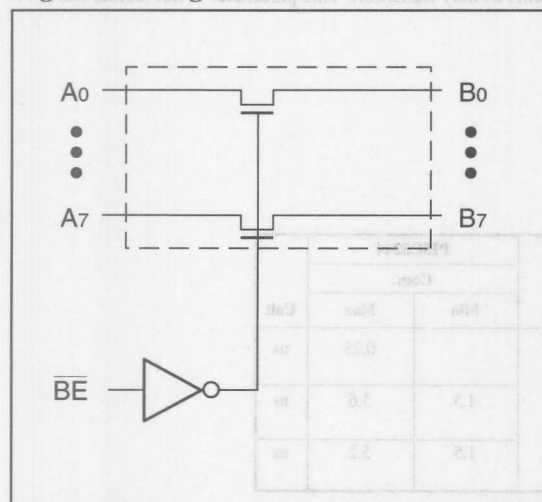
- Near zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μA Typical) – Ideally suited for notebook applications
- Packages available:
 - 20-pin 300 mil wide plastic PDIP (P20)
 - 20-pin 150 mil wide plastic QSOP (Q20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Product Description:

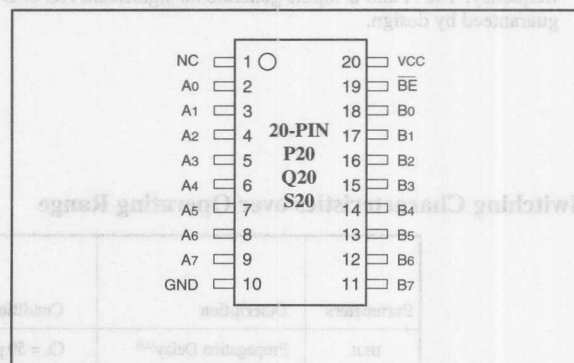
Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3245 is a 8-bit, 2-port bus switch designed with a low ON resistance (5Ω) allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or additional ground bounce noise. The switches are turned ON by the Bus Enable (BE) input signal. The pinout is compatible with PI74FCT245T (Octal Bidirectional Transceiver).

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
BE	Bus Enable Input (Active LOW)
A0-7	Bus A
B0-7	Bus B
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Function	BE	A0-7
Disconnect	H	Hi-Z
Connect	L	B0-7

NOTE: 1. H = High Voltage Level
L = Low Voltage Level
Hi-Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I _{IH}	Input HIGH Current	VCC = Max., V _{IN} = VCC			±1	μA
I _{IL}	Input LOW Current	VCC = Max., V _{IN} = GND			±1	μA
I _{OZH}	High Impedance Output Current	0 ≤ A, B ≤ VCC			±1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current ⁽³⁾	A (B) = 0V, B (A) = VCC	100			mA
V _H	Input Hysteresis at Control Pins			150		mV
RON	Switch On Resistance ⁽⁴⁾	VCC = Min., V _{IN} = 0.0V, I _{ON} = 48 mA VCC = Min., V _{IN} = 2.4V, I _{ON} = 15 mA		5 10	7 15	Ω

8
Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OFF}	A/B Capacitance, Switch Off	V _{IN} = 0V		6	pF
C _{ON}	A/B Capacitance, Switch On	V _{IN} = 0V		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, TA = 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	3.0	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{cc}.
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

		PI5C3245			
		Com.			
Parameters	Description	Conditions ⁽¹⁾	Min	Max	Unit
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω		0.25	ns
tPHL	Ax to Bx, Bx to Ax				
tPZH	Bus Enable Time		1.5	6.5	ns
tPZL	BE to Ax or Bx				
tPHZ	Bus Disable Time		1.5	5.5	ns
tPLZ	BE to Ax or Bx				

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not tested on Propagation Delays.
- The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Bus Switch 8:1 MUX/DEMUX

Product Features:

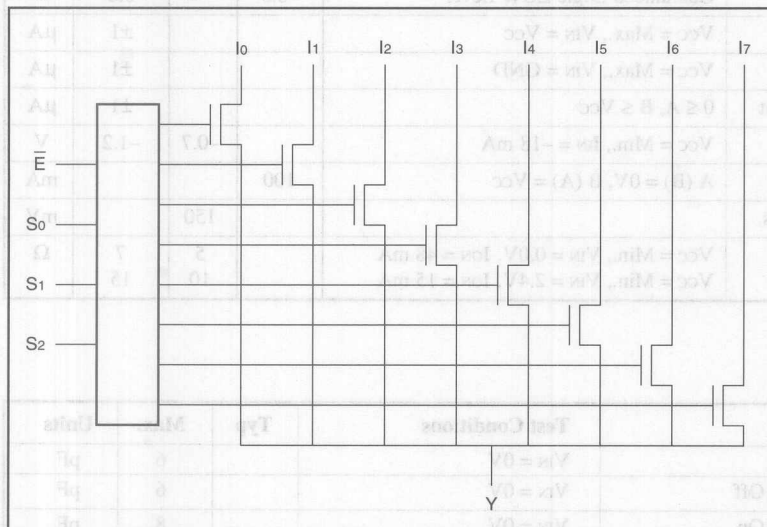
- Near zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power ($0.2\mu A$ Typical) – Ideally suited for notebook applications
- Pin compatible with PI74FCT251T
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

Product Description:

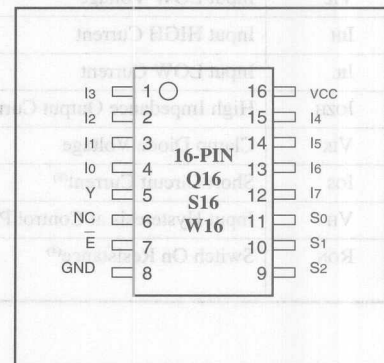
Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3251 is a Dual 8:1 Multiplexer/demultiplexer with three-state outputs that is pinout compatible with the PI74FCT251T, 74F251, and 74ALS/AS/LS 251. Inputs can be connected to outputs with low on resistance (5Ω) with no additional ground bounce noise or propagation delay.

Logic Block Diagram



Product Pin Configuration



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Product Pin Description

Pin Name	Description
I0-7	Data Inputs
S0-2	Select Inputs
E	Enable
Y	Data Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

E	Select			Y	Function
	S2	S1	S0		
H	X	X	X	Hi-Z	Disable
L	L	L	L	I0	S2-0 = 0
L	L	L	H	I1	S2-0 = 1
L	L	H	L	I2	S2-0 = 2
L	L	H	H	I3	S2-0 = 3
L	H	L	L	I4	S2-0 = 4
L	H	L	H	I5	S2-0 = 5
L	H	H	L	I6	S2-0 = 6
L	H	H	H	I7	S2-0 = 7

NOTE: 1. H = High Voltage Level
L = Low Voltage Level

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			±1	μA
I _{OZH}	High Impedance Output Current	0 ≤ A, B ≤ V _{CC}			±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current ⁽³⁾	A (B) = 0V, B (A) = V _{CC}	100			mA
V _H	Input Hysteresis at Control Pins			150		mV
R _{ON}	Switch On Resistance ⁽⁴⁾	V _{CC} = Min., V _{IN} = 0.0V, I _{ON} = 48 mA V _{CC} = Min., V _{IN} = 2.4V, I _{ON} = 15 mA		5 10	7 15	Ω

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OFF}	A/B Capacitance, Switch Off	V _{IN} = 0V		6	pF
C _{ON}	A/B Capacitance, Switch On	V _{IN} = 0V		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	3.0	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/ MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{CC}.
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PIS3251		Unit
			Com.		
			Min	Max	
trY	Propagation Delay ^(2,3) In to Y	CL = 50 pF RL = 500Ω		0.25	ns
tsY	Bus Enable Time Sn to Y		0.5	6.6	ns
tPHZ	Bus Disable Time En to Y		0.5	6.0	ns
tPLZ	Bus Disable Time En to Y		0.5	6.0	ns

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not tested on Propagation Delays.
- The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Bus Switch Dual 4:1 MUX/DEMUX

Product Features:

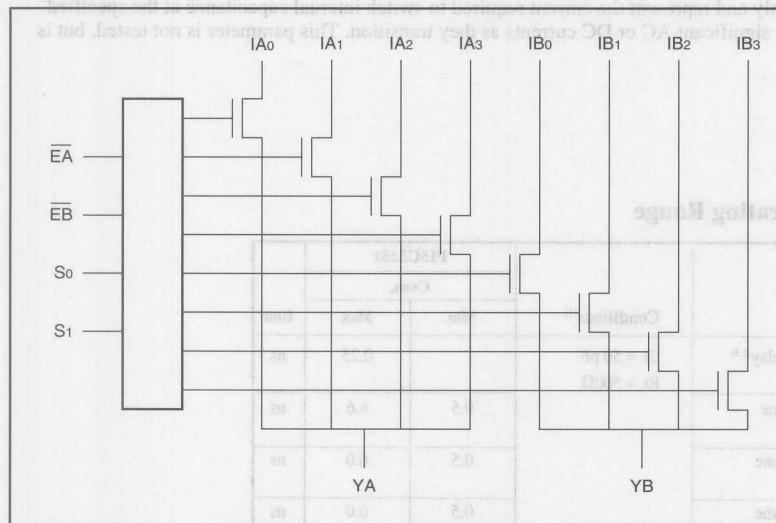
- Near zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μA Typical) – Ideally suited for notebook applications
- Pin compatible with PI74FCT253T
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

Product Description:

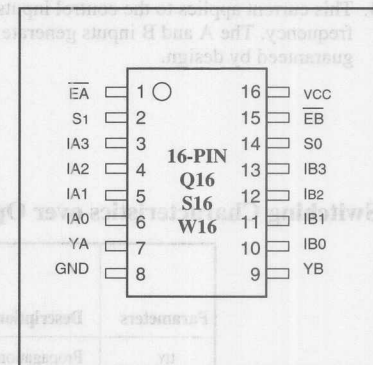
Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3253 is a Dual 4:1 Multiplexer/demultiplexer with three-state outputs that is pinout compatible with the PI74FCT253T, 74F253, and 74ALS/AS/LS 253. Inputs can be connected to outputs with low on resistance (5Ω) with no additional ground bounce noise or propagation delay.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
IA _n , IB _n	Data Inputs
S0–1	Select Inputs
EA, EB	Enable
YA, YB	Data Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Enable		Select				Function
EA	EB	S1	S0	YA	YB	
H	X	X	X	Hi-Z	X	Disable A
X	H	X	X	X	Hi-Z	Disable B
L	L	L	L	IA0	IB0	S1-0 = 0
L	L	L	H	IA1	IB1	S1-0 = 1
L	L	H	L	IA2	IB2	S1-0 = 2
L	L	H	H	IA3	IB3	S1-0 = 3

NOTE: 1. H = High Voltage Level
L = Low Voltage Level

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I _{IH}	Input HIGH Current	VCC = Max., V _{IN} = VCC			±1	μA
I _{IL}	Input LOW Current	VCC = Max., V _{IN} = GND			±1	μA
I _{OZH}	High Impedance Output Current	0 ≤ A, B ≤ VCC			±1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current ⁽³⁾	A (B) = 0V, B (A) = VCC	100			mA
V _H	Input Hysteresis at Control Pins			150		mV
RON	Switch On Resistance ⁽⁴⁾	VCC = Min., V _{IN} = 0.0V, I _{ON} = 48 mA VCC = Min., V _{IN} = 2.4V, I _{ON} = 15 mA		5 10	7 15	Ω

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Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OFF}	A/B Capacitance, Switch Off	V _{IN} = 0V		6	pF
C _{ON}	A/B Capacitance, Switch On	V _{IN} = 0V		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, TA = 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	3.0	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/ MHz

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient.
3. Per TTL driven input ($V_{IN} = 3.4V$, control inputs only); A and B pins do not contribute to I_{CC} .
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	P15C3253		Unit
			Com.		
			Min	Max	
t _{PD}	Propagation Delay ^(2,3) In to Y	C _L = 50 pF R _L = 500Ω		0.25	ns
t _{SE}	Bus Enable Time Sn to Y		0.5	6.6	ns
t _{PHZ} t _{PLZ}	Bus Disable Time En to Y		0.5	6.0	ns
t _{DE}	Bus Disable Time En to Y		0.5	6.0	ns

Notes:

1. See test circuit and wave forms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Bus Switch Quad 2:1 MUX/DEMUX

Product Features:

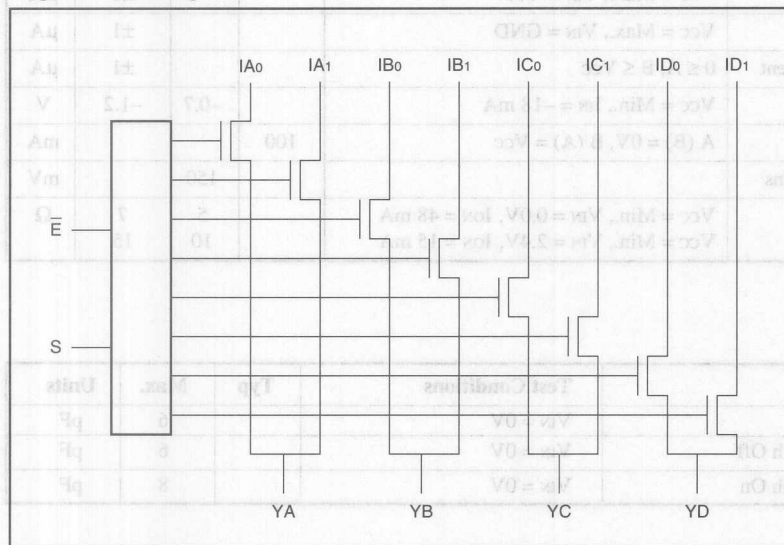
- Near zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μA Typical) – Ideally suited for notebook applications
- Pin compatible with PI74FCT257T
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q16)
 - 16-pin 300 mil wide plastic SOIC (S16)
 - 16-pin 150 mil wide plastic SOIC (W16)

Product Description:

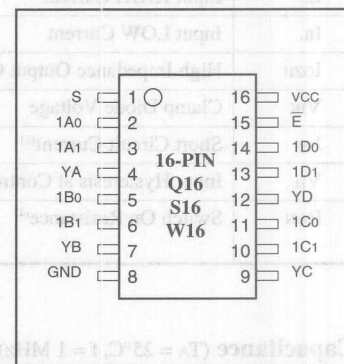
Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3257 is a Quad 2:1 multiplexer/demultiplexer with three-state outputs that is pinout and function compatible with the PI74FCT257T, 74F257, and 74ALS/AS/LS 257. Inputs can be connected to outputs with low on resistance (5Ω) with no additional ground bounce noise or propagation delay.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
IA _n -ID _n	Data Inputs
S	Select Inputs
\bar{E}	Enable
YA-YD	Data Outputs
GND	Ground
VCC	Power

Truth Table⁽¹⁾

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

NOTE: 1. H = High Voltage Level
L = Low Voltage Level

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$			± 1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$			± 1	μA
I_{OZH}	High Impedance Output Current	$0 \leq A, B \leq V_{CC}$			± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current ⁽³⁾	$A (B) = 0V, B (A) = V_{CC}$	100			mA
V_H	Input Hysteresis at Control Pins			150		mV
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0V, I_{ON} = 48 \text{ mA}$ $V_{CC} = \text{Min.}, V_{IN} = 2.4V, I_{ON} = 15 \text{ mA}$		5 10	7 15	Ω

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OFF}	A/B Capacitance, Switch Off	$V_{IN} = 0V$		6	pF
C_{ON}	A/B Capacitance, Switch On	$V_{IN} = 0V$		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	3.0	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., A and B Pins Open \overline{BE} = GND Control Input Toggling 50% Duty Cycle				0.25	mA/MHz

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{cc} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{cc}.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

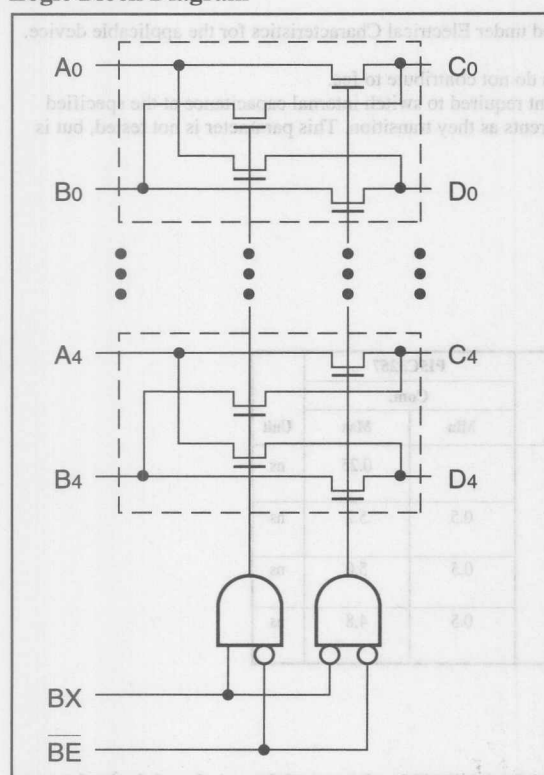
Parameters	Description	Conditions ⁽¹⁾	PIS3257		Unit
			Com.		
			Min	Max	
t _{ry}	Propagation Delay ^(2,3) In to Y	C _L = 50 pF R _L = 500Ω		0.25	ns
t _{SY}	Bus Enable Time S _n to Y		0.5	5.2	ns
t _{PHZ} t _{PLZ}	Bus Disable Time En to Y		0.5	5.0	ns
t _{Ey}	Bus Disable Time En to Y		0.5	4.8	ns

Notes:

1. See test circuit and wave forms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Product Features:

- Near zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power ($0.2\ \mu\text{A}$ Typical) – Ideally suited for notebook applications
- Packages available:
 - 24-pin 300 mil wide plastic PDIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Logic Block Diagram

Truth Table⁽¹⁾

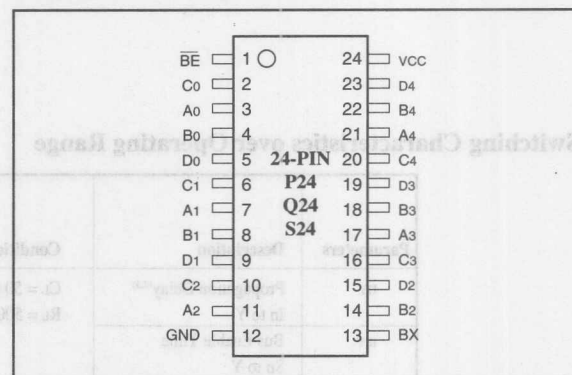
Function	BE	BX	A0-4	B0-4
Disconnect	H	X	Hi-Z	Hi-Z
Connect	L	L	C0-4	D0-4
Exchange	L	H	D0-4	C0-4

NOTE: 1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Hi-Z = High Impedance

Product Description:

Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3383 is a 5-bit, 4-port bus switch with exchange designed with a low ON resistance (5Ω) allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or additional ground bounce noise. The switches are turned ON by the Bus Enable ($\overline{\text{BE}}$) input signal, and the Bus Exchange (BX) input signal offers nibble swapping of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters, etc.

Product Pin Configuration

Product Pin Description

Pin Name	Description
$\overline{\text{BE}}$	Bus Enable Input (Active LOW)
BX	Bus Exchange Input
Ax	Bus A
Bx	Bus B
Cx	Bus C
Dx	Bus D
GND	Ground
Vcc	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			±1	μA
I _{OZH}	High Impedance Output Current	0 ≤ A, B ≤ V _{CC}			±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current ⁽³⁾	A (B) = 0V, B (A) = V _{CC}	100			mA
V _H	Input Hysteresis at Control Pins			150		mV
R _{ON}	Switch On Resistance ⁽⁴⁾	V _{CC} = Min., V _{IN} = 0.0V, I _{ON} = 48 mA V _{CC} = Min., V _{IN} = 2.4V, I _{ON} = 15 mA		5 10	7 15	Ω

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Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OFF}	A/B Capacitance, Switch Off	V _{IN} = 0V		6	pF
C _{ON}	A/B Capacitance, Switch On	V _{IN} = 0V		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{CC}		0.1	3.0	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{cc}.
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PISC3383		Unit
			Com.		
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω		0.25	ns
tPHL	Ax to Cx, Bx to Dx				
tPZH	Bus Enable Time		1.5	6.5	ns
tPZL	BE to Cx or Dx				
tPHZ	Bus Disable Time		1.5	5.5	ns
tPLZ	BE to Cx or Dx				
tBX	Bus Exchange Time		1.5	6.5	ns
	BX to Cx or Dx				

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not tested on Propagation Delays.
- The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.



PI5C3384 PI5C3384A PI5C32384 (25Ω)

10-Bit, 2-Port Bus Switch

Product Features:

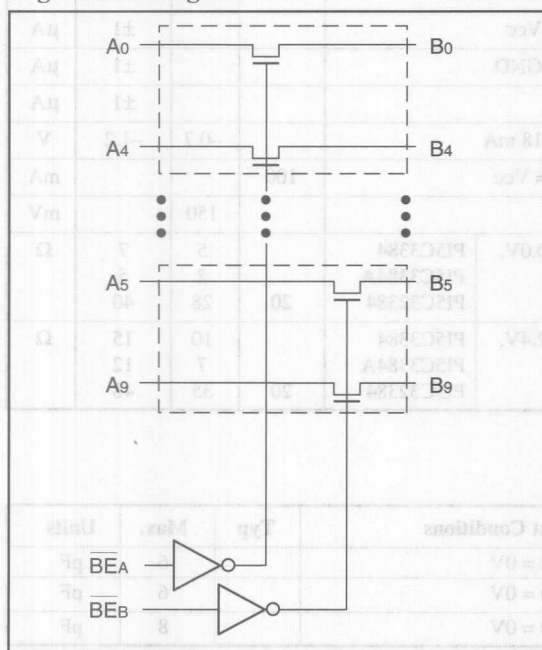
- Near zero propagation delay
- Low noise, 25Ω version (PI5C32383)
- 5Ω switches connect inputs to outputs (PI5C3384)
- 2Ω switches connect inputs to outputs (PI5C3384A)
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μA Typical) – Ideally suited for notebook applications
- Packages available:
 - 24-pin 300 mil wide plastic PDIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

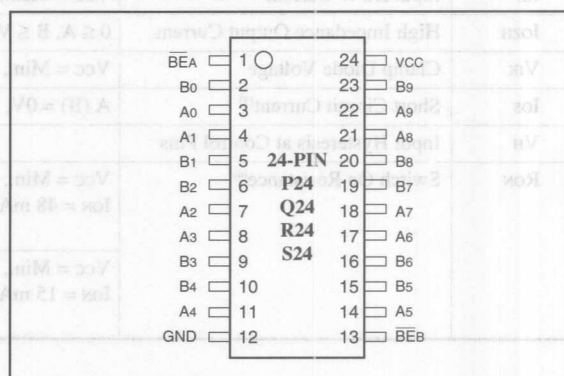
Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3384, PI5C3384A, and PI5C32384 are 10-bit, 2-port bus switches with exchange designed with a low ON resistance allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or additional ground bounce noise. The switches are turned ON by the Bus Enable (\overline{BE}) input signal. Two bus enable signals are provided, one for each of the upper and lower five bits of the two 10-bit buses. The PI5C32384 is designed with an internal 25Ω resistor reducing noise reflection in high-speed applications.

Logic Block Diagram



Product Pin Configuration



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Product Pin Description

Pin Name	Description
\overline{BEA} , \overline{BEB}	Bus Enable Inputs (Active LOW)
A0-9	Bus A
B0-9	Bus B
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Function	\overline{BEA}	\overline{BEB}	B0-4	B5-9
Disconnect	H	H	Hi-Z	Hi-Z
Connect	L	H	A0-4	Hi-Z
Connect	H	L	Hi-Z	A5-9
Connect	L	L	A0-4	A5-9

NOTE: 1. H = High Voltage Level, L = Low Voltage Level, Hi-Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			±1	μA
I _{OZH}	High Impedance Output Current	0 ≤ A, B ≤ V _{CC}			±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current ⁽³⁾	A (B) = 0V, B (A) = V _{CC}	100			mA
V _H	Input Hysteresis at Control Pins			150		mV
R _{ON}	Switch On Resistance ⁽⁴⁾	V _{CC} = Min., V _{IN} = 0.0V, I _{ON} = 48 mA		5	7	Ω
		V _{CC} = Min., V _{IN} = 2.4V, I _{ON} = 15 mA		10	15	Ω
		PI5C3384		2	5	
		PI5C3384A		28	40	
		PI5C32384	20			
		PI5C3384		7	12	
		PI5C3384A		35	48	
		PI5C32384	20			

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OFF}	A/B Capacitance, Switch Off	V _{IN} = 0V		6	pF
C _{ON}	A/B Capacitance, Switch On	V _{IN} = 0V		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, TA = 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	3.0	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., A and B Pins Open $\overline{\text{BE}}1$ or $\overline{\text{BE}}2$ = GND Control Input Toggling 50% Duty Cycle				0.25	mA/ MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{CC}.
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

PI5C3384 Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	P15C3384		Unit
			Com.		
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω	—	0.25	ns
tPHL	Ax to Bx, Bx to Ax				
tPZH	Bus Enable Time		1.5	6.5	ns
tPZL	B̄Ex to Ax or Bx				
tPHZ	Bus Disable Time		1.5	5.5	ns
tPLZ	B̄Ex to Ax or Bx				

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not tested on Propagation Delays.
- The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

PI5C3384A Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PI5C3384A		Unit
			Com.		
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω	—	0.25	ns
tPHL	Ax to Bx, Bx to Ax				
trZH	Bus Enable Time		1.5	6.5	ns
trZL	B̄Ex to Ax or Bx				
trHZ	Bus Disable Time		1.5	5.5	ns
trLZ	B̄Ex to Ax or Bx				

PI5C32384 Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PI5C32384		Unit
			Com.		
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω	—	1.25	ns
tPHL	Ax to Bx, Bx to Ax				
tPZH	Bus Enable Time		1.5	7.5	ns
tPZL	B $\overline{\text{E}}$ x to Ax or Bx				
tPHZ	Bus Disable Time		1.5	5.5	ns
tPLZ	B $\overline{\text{E}}$ x to Ax or Bx				

Notes:

1. See test circuit and wave forms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

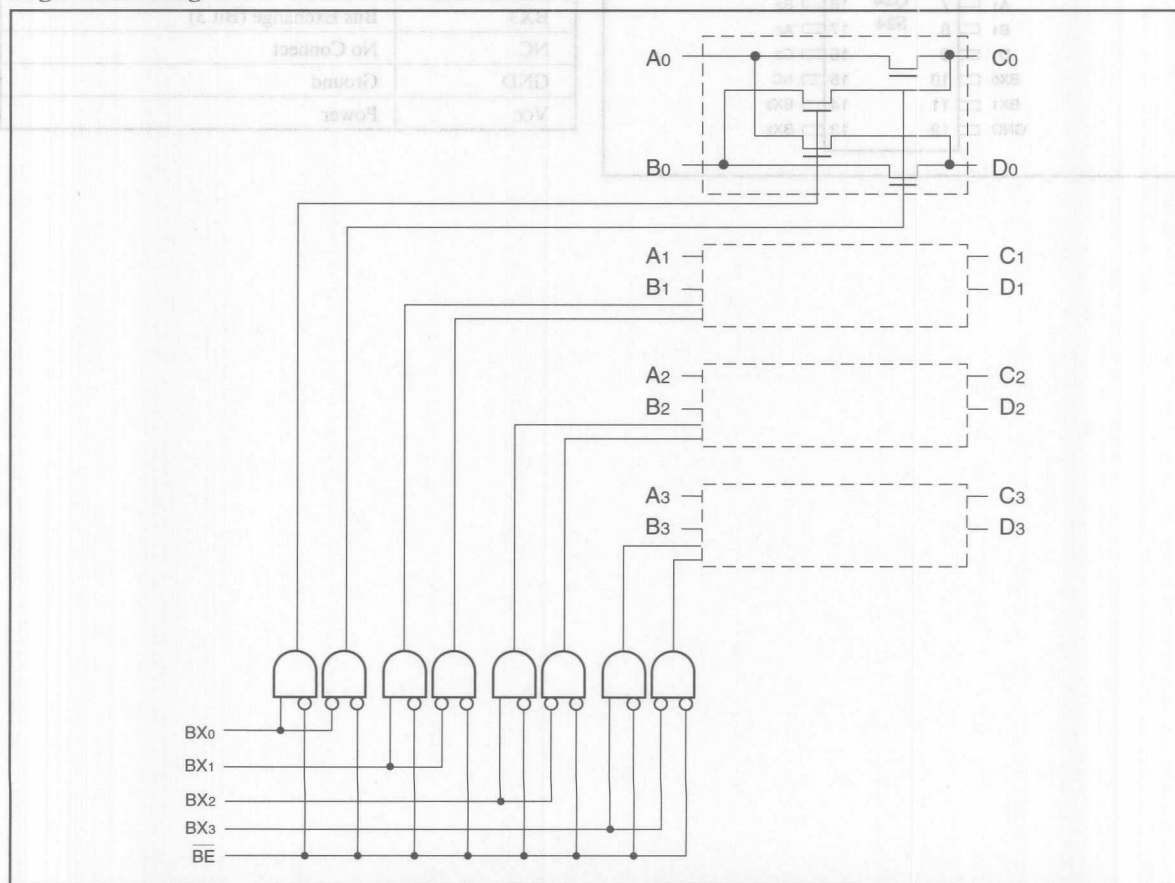
4-Bit, 4-Port Bus Switch
Product Features:

- Zero propagation delay
- Zero ground bounce in flow-through mode
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μA Typical) – Ideally suited for notebook applications
- Packages available:
 - 24-pin 300 mil wide plastic PDIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

Pericom Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3400 is a 4-bit, 4-port bus switch with individual exchanges designed with a low ON resistance (5Ω) allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or ground bounce noise. The switches are turned ON by the Bus Enable (BE) input signal, and the Bus Exchange (BX0–BX3) input signals offer individual bit swapping of the AB and CD signal pairs. This exchange configuration allows bit swapping of buses in systems.

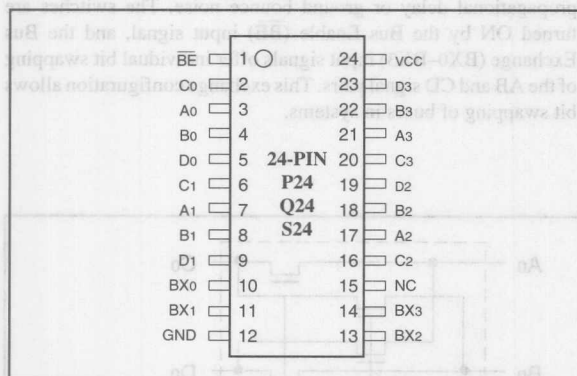
Logic Block Diagram


Truth Table⁽¹⁾

Function	BE	BX0	BX1	BX2	BX3	A0-3	B0-3
Disconnect	H	X	X	X	X	Hi-Z	Hi-Z
Connect	L	BXi = L				C0-3	D0-3
Exchange	L	BXi = H				D0-3	C0-3

NOTE: 1. H = High Voltage Level, X = Don't Care,
L = Low Voltage Level, Hi-Z = High Impedance
i = 0, 1, 2, or 3

Product Pin Configuration



Product Pin Description

Pin Name	Description
BE	Bus Enable Input (Active LOW)
Ax, Bx, Cx, Dx	Bus A, Bus B, Bus C, Bus D
BX0	Bus Exchange (Bit 0)
BX1	Bus Exchange (Bit 1)
BX2	Bus Exchange (Bit 2)
BX3	Bus Exchange (Bit 3)
NC	No Connect
GND	Ground
Vcc	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I _{IH}	Input HIGH Current	VCC = Max., V _{IN} = VCC			±1	μA
I _{IL}	Input LOW Current	VCC = Max., V _{IN} = GND			±1	μA
I _{OZH}	High Impedance Output Current	0 ≤ A, B ≤ VCC			±1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current ⁽³⁾	A (B) = 0V, B (A) = VCC	100			mA
V _H	Input Hysteresis at Control Pins			150		mV
R _{ON}	Switch On Resistance ⁽⁴⁾	VCC = Min., V _{IN} = 0.0V, I _{ON} = 48 mA VCC = Min., V _{IN} = 2.4V, I _{ON} = 15 mA		5 10	7 15	Ω

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Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OFF}	A/B Capacitance, Switch Off	V _{IN} = 0V		6	pF
C _{ON}	A/B Capacitance, Switch On	V _{IN} = 0V		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, TA = 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	3.0	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/ MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{CC}.
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PI5C3400		Unit
			Com.		
			Min	Max	
t _{PLH}	Propagation Delay ^(2,3)	C _L = 50 pF R _L = 500Ω		0.25	ns
t _{PHL}	Ax to Cx, Bx to Dx				
t _{PZH}	Bus Enable Time		1.5	6.5	ns
t _{PZL}	BE to Cx or Dx				
t _{PHZ}	Bus Disable Time		1.5	5.5	ns
t _{PLZ}	BE to Cx or Dx				
t _{BX}	Bus Exchange Time		1.5	6.5	ns
	BXx to Cx or Dx				

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not tested on Propagation Delays.
- The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

6-Bit, 3-Port Bus Switch

Product Features:

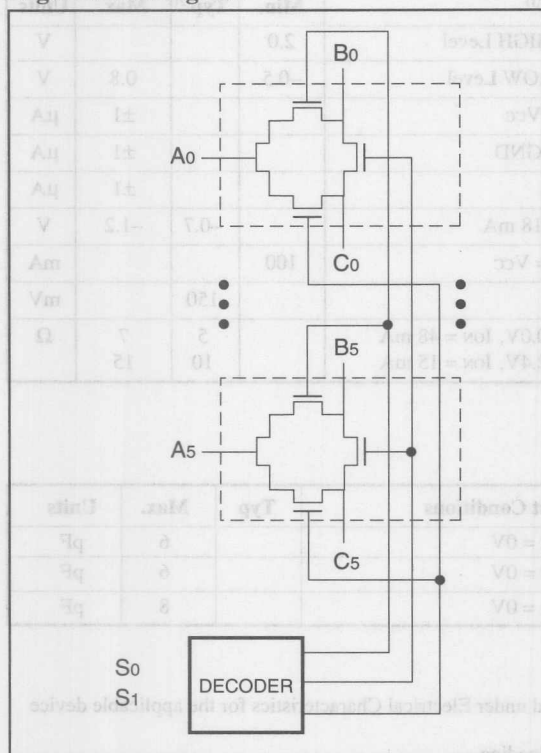
- Nero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μ A Typical) – Ideally suited for notebook applications
- Packages available:
 - 24-pin 300 mil wide plastic PDIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

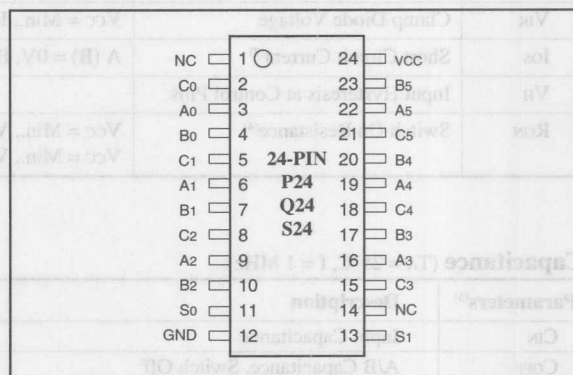
Pioneer Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3401 is a 6-bit, 3-port bus switch designed with a low ON resistance (5Ω) allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or additional ground bounce noise. The switches are turned OFF by $S0 = H$ and $S1 = H$. The A bus can be connected to B bus by $S0 = L$ and $S1 = L$. The B bus can be connected to C bus by $S0 = H$ and $S1 = L$. The C bus can be connected to A bus by $S0 = L$ and $S1 = H$.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
S0, S1	Bus Direction
A0-5	Bus A
B0-5	Bus B
C0-5	Bus C
NC	No Connect
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Function	S0	S1	A0-5	B0-5	C0-5
Disconnect	H	H	Hi-Z	Hi-Z	Hi-Z
Connect A-B	L	L	B0-5	A0-5	Hi-Z
Connect B-C	H	L	Hi-Z	C0-5	B0-5
Connect C-A	L	H	C0-5	Hi-Z	A0-5

NOTE: 1. H = High Voltage Level, L = Low Voltage Level, Hi-Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$			± 1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$			± 1	μA
I_{OZH}	High Impedance Output Current	$0 \leq A, B \leq V_{CC}$			± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current ⁽³⁾	$A (B) = 0V, B (A) = V_{CC}$	100			mA
V_H	Input Hysteresis at Control Pins			150		mV
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0V, I_{ON} = 48 \text{ mA}$ $V_{CC} = \text{Min.}, V_{IN} = 2.4V, I_{ON} = 15 \text{ mA}$		5 10	7 15	Ω

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OFF}	A/B Capacitance, Switch Off	$V_{IN} = 0V$		6	pF
C_{ON}	A/B Capacitance, Switch On	$V_{IN} = 0V$		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		0.1	3.0	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{cc}.
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	P15C3401		Unit
			Com.		
			Min	Max	
t _{PLH} t _{PHL}	Propagation Delay ^(2,3) Ax to Bx, Bx to Cx or Cx to Ax	C _L = 50 pF R _L = 500Ω		0.25	ns
t _s	Bus Direction Time Sx to Ax or Bx or Cx		1.5	6.5	ns

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not tested on Propagation Delays.
- The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

10-Bit, 2-Port Bus Switch

Product Features:

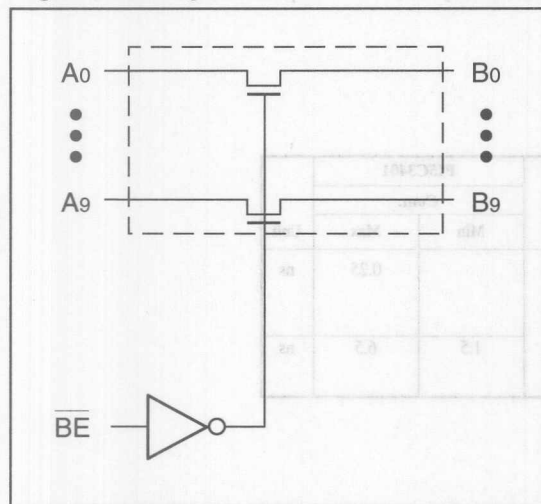
- Near zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Ultra Low Quiescent Power (0.2 μA Typical) – Ideally suited for notebook applications
- Packages available:
 - 24-pin 300 mil wide plastic PDIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

Pioneer Semiconductor's PI5C series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3861 is a 10-bit, 2-port bus switch designed with a low ON resistance (5Ω) allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or additional ground bounce noise. The switches are turned ON by the Bus Enable (BE) input signal.

Logic Block Diagram

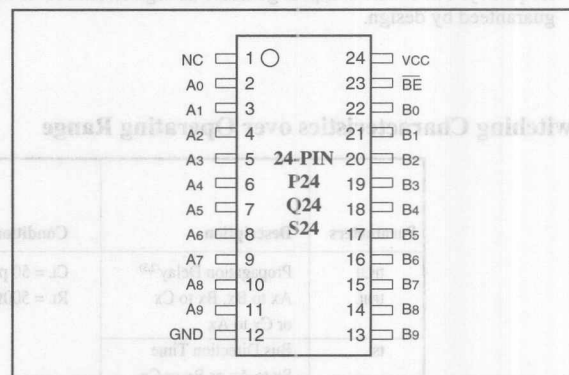


Truth Table⁽¹⁾

Function	BE	A0-9
Disconnect	H	Hi-Z
Connect	L	B0-9

NOTE: 1. H = High Voltage Level
L = Low Voltage Level
Hi-Z = High Impedance

Product Pin Configuration



Product Pin Description

Pin Name	Description
BE	Bus Enable Input (Active LOW)
A0-9	Bus A
B0-9	Bus B
GND	Ground
Vcc	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$			± 1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$			± 1	μA
I_{OZH}	High Impedance Output Current	$0 \leq A, B \leq V_{CC}$			± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current ⁽³⁾	$A (B) = 0V, B (A) = V_{CC}$	100			mA
V_H	Input Hysteresis at Control Pins			150		mV
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0.0V, I_{ON} = 48 \text{ mA}$ $V_{CC} = \text{Min.}, V_{IN} = 2.4V, I_{ON} = 15 \text{ mA}$		5 10	7 15	Ω

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Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁵⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OFF}	A/B Capacitance, Switch Off	$V_{IN} = 0V$		6	pF
C_{ON}	A/B Capacitance, Switch On	$V_{IN} = 0V$		8	pF

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., A and B Pins Open BE = GND Control Input Toggling 50% Duty Cycle				0.25	mA/MHz

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); A and B pins do not contribute to I_{cc}.
- This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	PI5C3861		Unit
			Com.		
			Min	Max	
tPLH	Propagation Delay ^(2,3)	CL = 50 pF RL = 500Ω		0.25	ns
tPHL	Ax to Bx, Bx to Ax				
tPZH	Bus Enable Time		1.5	6.5	ns
tPZL	$\overline{\text{BE}}$ to Ax or Bx				
tPHZ	Bus Disable Time		1.5	5.5	ns
tPLZ	$\overline{\text{BE}}$ to Ax or Bx				

Notes:

- See test circuit and wave forms.
- This parameter is guaranteed but not tested on Propagation Delays.
- The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

GENERAL INFORMATION

1

STANDARD AND 25Ω OUTPUT RESISTOR SERIES 5V FCT LOGIC PRODUCTS

3

DOUBLE DENSITY STANDARD 5V FCT LOGIC PRODUCTS

4

DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS

5

STANDARD 3.3V LOGIC PRODUCTS WITH 5V TOLERANT I/O

6

DOUBLE DENSITY 3.3V LOGIC PRODUCTS WITH 5V TOLERANT I/O

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PI49FCT3805	3.3V Buffer/Clock Driver	9.13
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PI6B2407	BiCMOS PLL Universal Clock Distribution Chip	9.34



PI49FCT804T

Fast CMOS Buffer/Clock Driver

Product Features:

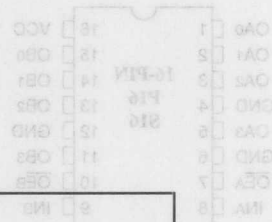
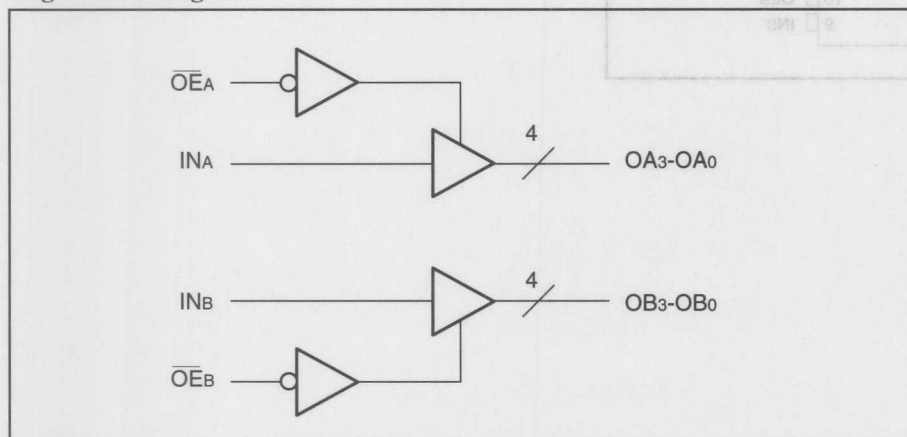
- Low output skew: 0.8 ns.
- Clock busing with 3-state control
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive, $I_{OL} = 64 \text{ mA}$
- Extremely low static power (1 mW, typ.)
- Hysteresis on all inputs
- ESD protection exceeds 2000V
- Packages available:
 - 16-pin 300 mil wide plastic DIP (P16)
 - 16-pin 300 mil wide plastic SOIC (S16)

Product Description:

Pericom Semiconductor's PI49FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI49FCT804T is a non-inverting clock driver designed with two independent groups of buffers. These buffers have 3-state OutputEnable inputs (active LOW) with a 1-in, 4-out configuration per group. Each clock driver consists of two banks of drivers, driving four outputs each from a standard TTL compatible CMOS input.

Logic Block Diagram



Product Pin Description

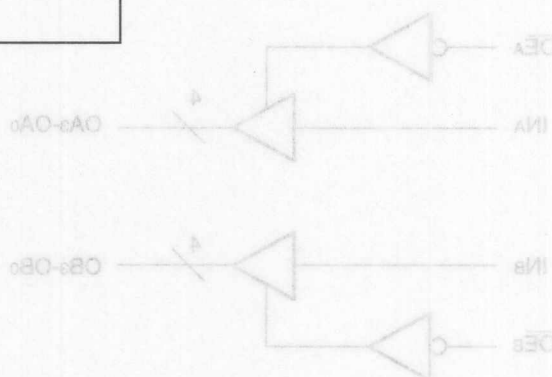
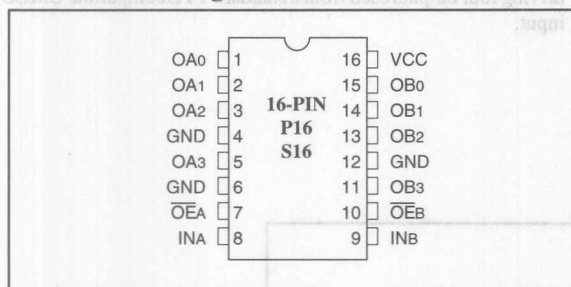
Pin Name	Description
$\overline{OE}A$, $\overline{OE}B$	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAN, OBN	Clock Outputs
GND	Ground
Vcc	Power

Truth Table⁽¹⁾

Inputs		Outputs
$\overline{OE}A$, $\overline{OE}B$	INA, INB	OAN, OBN
L	L	L
L	H	H
H	L	Z
H	H	Z

NOTE: 1. H = High Voltage Level, L = Low Voltage Level,
Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = 0°C to +70°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -24.0 mA	2.4	3.3		V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IIH	Input HIGH Current	VCC = Max., VIN = VCC			1	μA
IIL	Input LOW Current	VCC = Max., VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max., VOUT = VCC			1	μA
IOZL	Output Current	VCC = Max., VOUT = GND			-1	μA
II	Input HIGH Current	VCC = Max., VIN = VCC (Max.)			20	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120	-225	mA
VH	Input Hysteresis	VCC = 5V		200		mV

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Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		3	30	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE _A = OE _B = GND Per Output Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE _A = OE _B = GND Four Outputs Toggling	V _{IN} = V _{cc} V _{IN} = GND		6.2	11.2 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		6.4	12 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle OE _A = OE _B = GND Eight Outputs Toggling	V _{IN} = V _{cc} V _{IN} = GND		3.1	6.3 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		3.5	7.6 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_C = I_{cc} + ΔI_{cc} D_HN_T + I_{ccd} (f_{CP}/2 + f_iN_i)

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{ccd} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

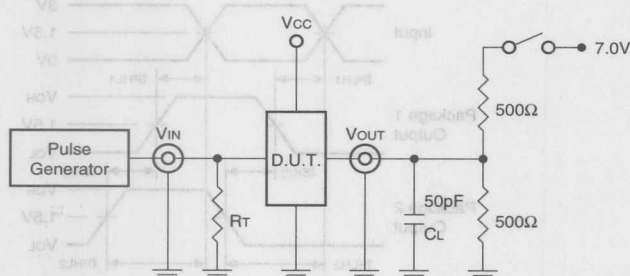
All currents are in milliamps and all frequencies are in megahertz.

PI49FCT804T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	804T		804AT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
tPLH tPHL	Propagation Delay INA to OAN, INB to OBN	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	5.8	ns
tPZH tPZL	Output Enable Time OEA to OAN, OEB to OBN		1.5	8.0	1.5	8.0	ns
tPHZ tPLZ	Output Disable Time OEA to OAN, OEB to OBN		1.5	7.0	1.5	7.0	ns
tsKEW(o) ⁽³⁾	Skew between two outputs of same package (same transition)		—	0.8	—	0.7	ns
tsKEW(p) ⁽³⁾	Skew between opposite transitions (tPHL-tPLH) of the same output		—	1.0	—	0.8	ns
tsKEW(t) ⁽³⁾	Skew between two outputs of different package at same temperature (same transition)		—	1.6	—	1.4	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).

Tests Circuits For All Outputs⁽¹⁾

Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

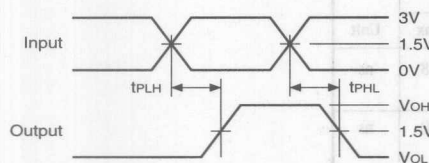
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

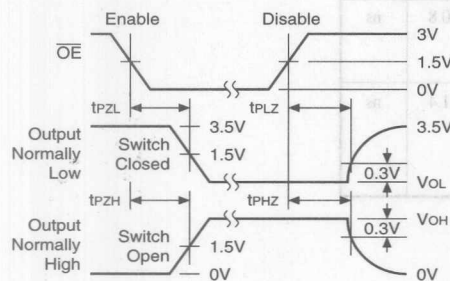
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SWITCHING WAVEFORMS

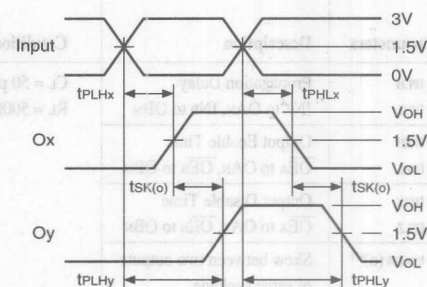
Propagation Delay



Enable and Disable Times

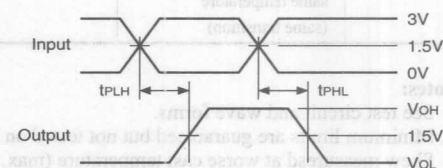


Output Skew - tsk(o)



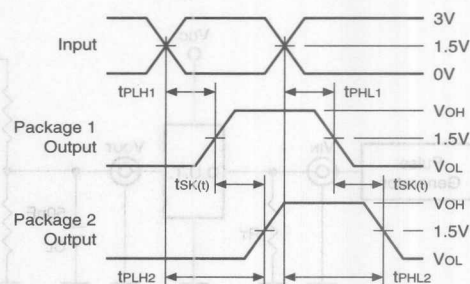
$$tsk(o) = |tPLHy - tPLHx| \text{ or } |tPHLy - tPHLx|$$

Pulse Skew - tsk(p)



$$tsk(p) = |tPHL - tPLH|$$

Package Skew - tsk(t)



$$tsk(t) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Switch	Test
Open	Open Drain
Closed	Disable LOW
	Enable LOW
Open	All Other Inputs

DEFINITIONS:
 CL = Load capacitance, includes jig and probe capacitance.
 RT = Termination resistance, should be equal to ZOUT of the Pulse Generator.



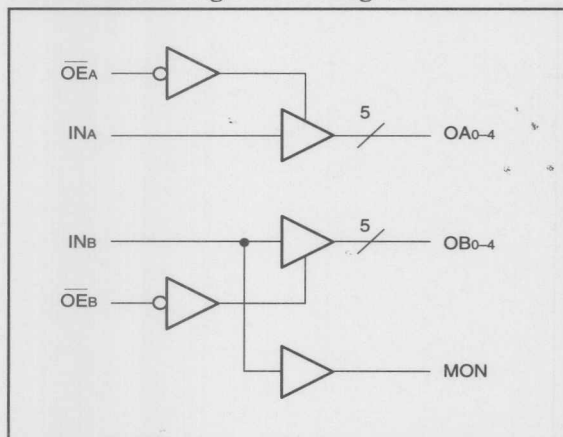
PI49FCT805T
PI49FCT806T

Fast CMOS Buffer/Clock Driver

Product Features:

- Extremely low output skew: 0.5 ns
- Monitor output pin
- Clock busing with 3-state control
- TTL input and CMOS output compatible
- Extremely low static power (1 mW, typ.)
- ESD protection exceeds 2000V
- Hysteresis on all inputs
- Packages available:
 - 20-pin 300 mil wide DIP (P20)
 - 20-pin 300 mil wide SOIC (S20)
 - 20-pin 150 mil wide QSOP (Q20)

PI49FCT805T Logic Block Diagram

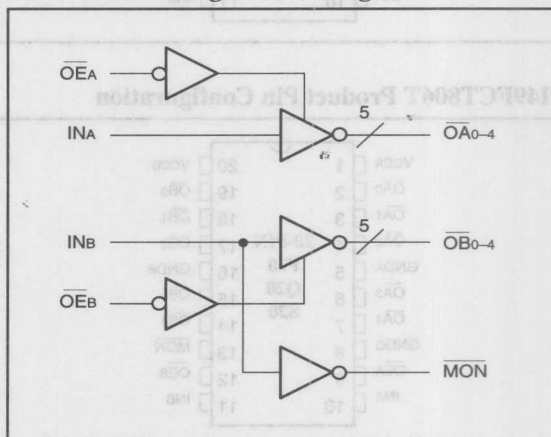


Product Description:

Pericom Semiconductor's PI49FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI49FCT805T is a non-inverting clock driver and the PI49FCT806T is an inverting clock driver designed with two independent groups of buffers. These buffers have 3-state Output Enable inputs (active LOW) with a 1-in, 5-out configuration per group. Each clock driver consists of two banks of drivers, driving five outputs each from a standard TTL compatible CMOS input.

PI49FCT806T Logic Block Diagram



Product Pin Description

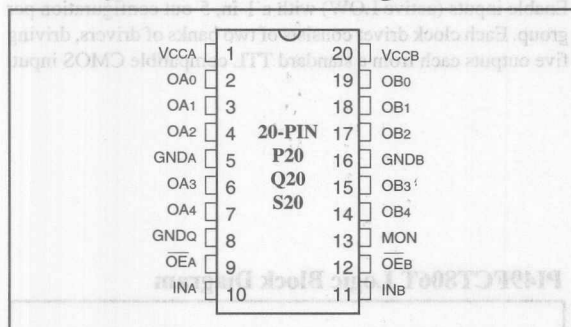
Pin Name	Description
$\overline{OE}A, \overline{OE}B$	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAN, OBN	Clock Outputs
MON	Monitor Output
GND	Ground
Vcc	Power

PI49FCT805T Truth Table⁽¹⁾

Inputs		Outputs	
$\overline{OE}A, \overline{OE}B$	INA, INB	OAN, OBN	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE: 1. H = High Voltage Level, L = Low Voltage Level,
Z = High Impedance

PI49FCT805T Product Pin Configuration

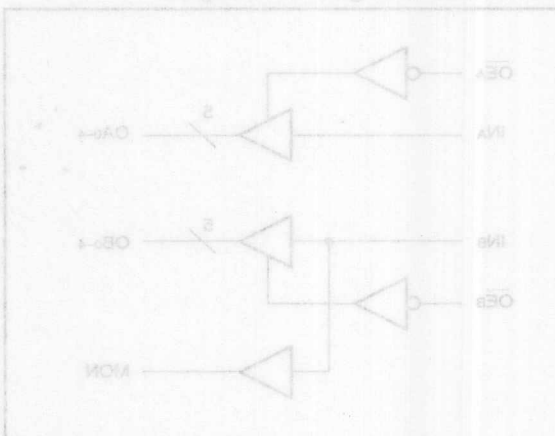
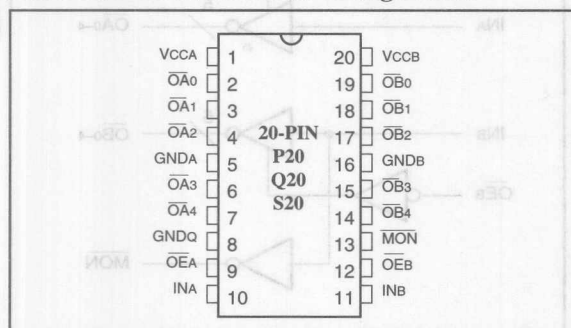


PI49FCT806T Truth Table⁽¹⁾

Inputs		Outputs	
$\overline{OE}A, \overline{OE}B$	INA, INB	$\overline{O}AN, \overline{O}BN$	\overline{MON}
L	L	H	H
L	H	L	L
H	L	Z	H
H	H	Z	L

NOTE: 1. H = High Voltage Level, L = Low Voltage Level,
Z = High Impedance

PI49FCT806T Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = 0°C to +70°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL IOH = -24.0 mA	2.4	3.3		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL IOL = 64 mA		0.3	0.55	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
IiH	Input HIGH Current	VCC = Max. VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max. VIN = GND			-1	μA
IOZH	High Impedance	VCC = Max. VOUT = VCC			1	μA
IOZL	Output Current	VCC = Max. VOUT = GND			-1	μA
Ii	Input HIGH Current	VCC = Max., VIN = VCC (Max.)			20	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND	-60	-120	-225	mA
VH	Input Hysteresis	VCC = 5 V		200		mV

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Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0 V	6	10	pF
COUT	Output Capacitance	VOUT = 0 V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{CC} = Max.	* V _{IN} = GND or V _{CC}		3	30	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open OE _A = OE _B = GND Per Output Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE _A = OE _B = GND Five Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND		7.7	14.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		8.0	15.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle OE _A = OE _B = GND Eleven Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND		4.3	8.4 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		4.8	10.4 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_t + I_{CCD} (f_{cp}/2 + f_i N_i)$$

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_t = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{cp} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

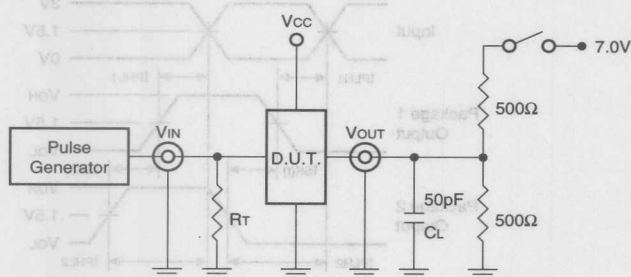
All currents are in milliamps and all frequencies are in megahertz.

PI49FCT805/806T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	805T/806T		805AT/806AT		805BT/806BT		805CT/806CT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	5.8	1.5	5.0	1.5	4.5	ns
tPHL	INA to OAN, INB to OBN										
tpZH	Output Enable Time		1.5	8.0	1.5	8.0	1.5	8.5	1.5	6.2	ns
tpZL	OEA to OAN, OEB to OBN										
tpHZ	Output Disable Time ⁽⁴⁾		1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	ns
tPLZ	OEA to OAN, OEB to OBN										
tsKEW(o) ⁽³⁾	Skew between two outputs of same package (same transition)		—	0.7	—	0.7	—	0.5	—	0.5	ns
tsKEW(p) ⁽³⁾	Skew between opposite transitions (tPHL-tPLH) of the same output		—	1.0	—	0.7	—	0.5	—	0.5	ns
tsKEW(t) ⁽³⁾	Skew between two outputs of different package at same temperature (same transition)		—	1.5	—	1.2	—	1.0	—	0.8	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. This parameter is guaranteed but not production tested.

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Tests Circuits For All Outputs⁽¹⁾

Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

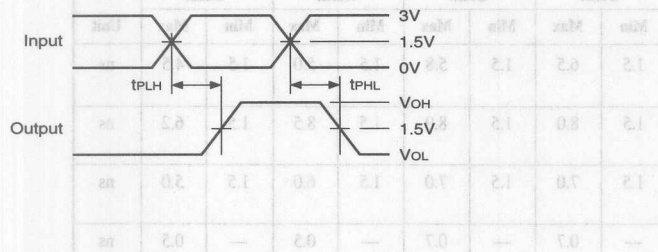
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

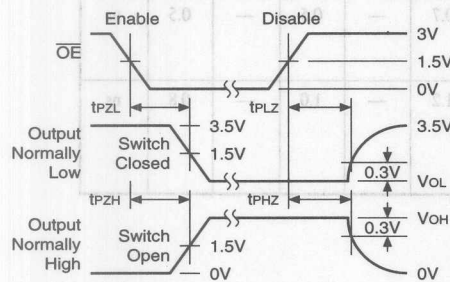
Rt = Termination resistance: should be equal to Zout of the Pulse Generator.

SWITCHING WAVEFORMS

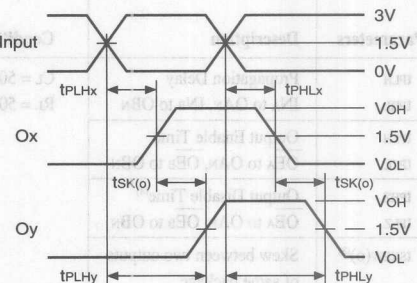
Propagation Delay



Enable and Disable Times

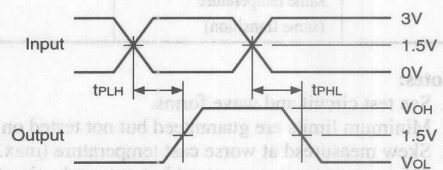


Output Skew – tsk(o)



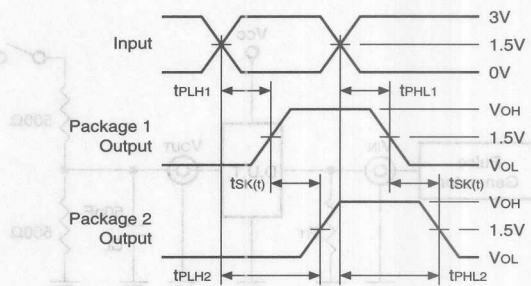
$$tsk(o) = |tPLHy - tPLHx| \text{ or } |tPHLy - tPHLx|$$

Pulse Skew – tsk(p)



$$tsk(p) = |tPLH1 - tPLH2|$$

Package Skew – tsk(t)



$$tsk(t) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Switch	Test
Open	Open Drain
Closed	Disable LOW
	Enable LOW
Open	All Other inputs

DEFINITIONS:
 CL = Load capacitance, includes jig and probe capacitance.
 RT = Termination resistance, should be equal to Zout of the Pulse Generator.



PI49FCT3805
PI49FCT3806

3.3V Fast CMOS Buffer/Clock Driver

Product Features:

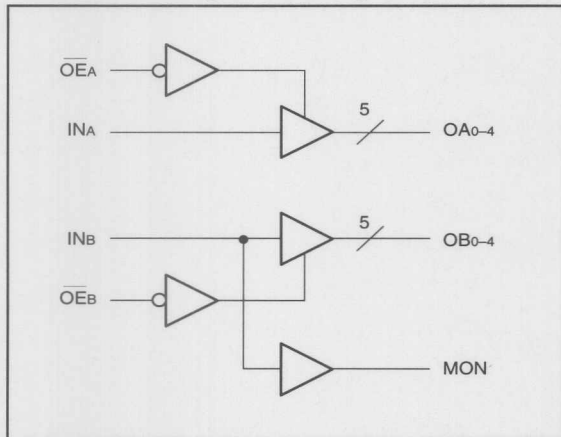
- 3.3V version of PI49FCT805/806
- Extremely low output skew: 0.5 ns
- Monitor output pin
- Clock busing with 3-state control
- TTL input and CMOS output compatible
- Extremely low static power (1 mW, typ.)
- ESD protection exceeds 2000V
- Hysteresis on all inputs
- Packages available:
 - 20-pin 300 mil wide DIP (P20)
 - 20-pin 300 mil wide SOIC (S20)
 - 20-pin 150 mil wide QSOP (Q20)

Product Description:

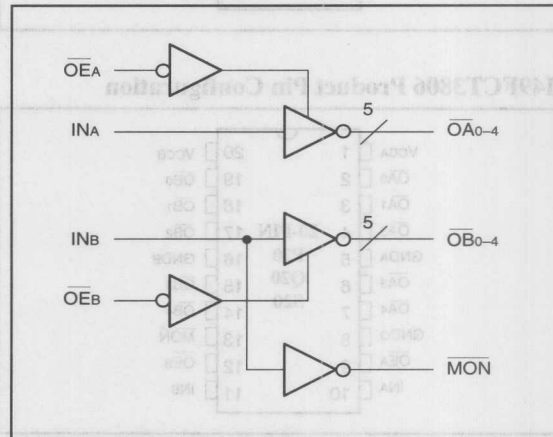
Pericom Semiconductor's PI49FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI49FCT3805 is a 3.3V non-inverting clock driver and the PI49FCT3806 is a 3.3V inverting clock driver designed with two independent groups of buffers. These buffers have 3-state Output Enable inputs (active LOW) with a 1-in, 5-out configuration per group. Each clock driver consists of two banks of drivers, driving five outputs each from a standard TTL compatible CMOS input.

PI49FCT3805 Logic Block Diagram



PI49FCT3806 Logic Block Diagram



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Parameter	Description	Test Conditions	Typ	Max	Units
C_{in}	Input Capacitance	$V_{in} = 0V$	4.5	6.0	pf
C_{out}	Output Capacitance	$V_{out} = 0V$	2.5	8.0	pf

1. This parameter is determined by device characterization but is not production tested.

Product Pin Description

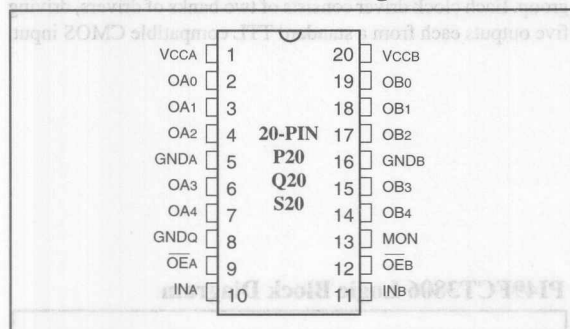
Pin Name	Description
$\overline{OE}A, \overline{OE}B$	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAN, OBN	Clock Outputs
MON	Monitor Output
GND	Ground
Vcc	Power

PI49FCT3805 Truth Table⁽¹⁾

Inputs		Outputs	
$\overline{OE}A, \overline{OE}B$	INA, INB	OAN, OBN	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE: 1. H = High Voltage Level, L = Low Voltage Level,
Z = High Impedance

PI49FCT3805 Product Pin Configuration

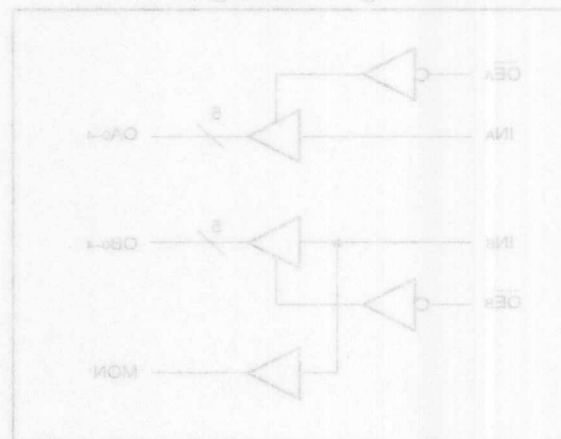
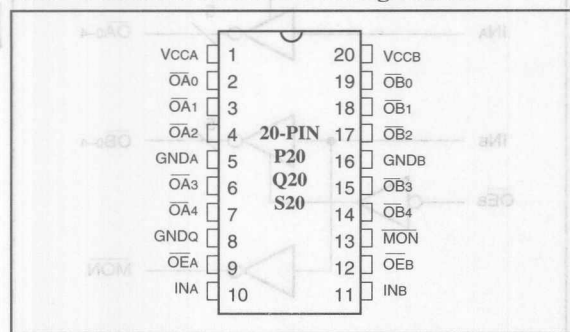


PI49FCT3806 Truth Table⁽¹⁾

Inputs		Outputs	
$\overline{OE}A, \overline{OE}B$	INA, INB	OAN, OBN	MON
L	L	H	H
L	H	L	L
H	L	Z	H
H	H	Z	L

NOTE: 1. H = High Voltage Level, L = Low Voltage Level,
Z = High Impedance

PI49FCT3806 Product Pin Configuration



Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Ambient Temperature = 0°C to +70°C
Vcc = 3.3V ± 0.3V

DC Electrical Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -0.1 mA I _{OH} = -8 mA	V _{CC} -0.2 2.4 ⁽³⁾	— 3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1 mA I _{OL} = 16 mA I _{OL} = 24 mA	— — —	— 0.2 0.3	0.2 0.4 0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	Input Pins	2.0	—	5.5	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	Input Pins	-0.5	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC} (Input Pins)		—	—	1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND (Input & I/O Pins)		—	—	-1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = V _{CC}	—	—	1	μA
I _{OZL}	Output Current	(3-State Output Pins)	V _{OUT} = GND	—	—	-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		—	-0.7	-1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽⁴⁾		-35	-60	-110	mA
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽⁴⁾		50	90	200	mA
I _{OS}	Short Circuit Current ⁽⁵⁾	V _{CC} = Max., V _{OUT} = GND ⁽⁵⁾		-60	-135	-240	mA
V _H	Input Hysteresis			—	150	—	mV

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
- V_{OH} = V_{CC} - 0.6V at rated current.
- This parameter is determined by device characterization but is not production tested.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}	—	3	30	μA
ΔI _{CC}	Supply Current per Inputs @ TTL HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾	—	2.0	300	μA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open O _{EA} or O _{EB} = GND Per Output Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.08	0.16	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _o = 10 MHz 50% Duty Cycle O _{EA} or O _{EB} = GND Mon. Output Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	3.3	9.0 ⁽⁵⁾	mA
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	3.3	10.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _o = 2.5 MHz 50% Duty Cycle O _{EA} or O _{EB} = GND Eleven Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	1.8	6.0 ⁽⁵⁾	
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	1.8	7.0 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input (V_{IN} = V_{CC} - 0.6V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_H N_T + I_{CCD} (f_o N_O)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} - 0.6V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_o = Output Frequency
N_O = Number of Outputs at f_o
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

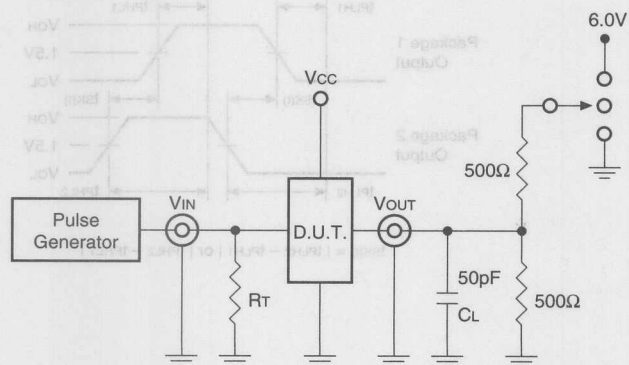
Parameters	Description	Conditions ⁽¹⁾	3805/3806		3805A/3806A		3805B/3806B		3805C/3806C		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay IN _A to OAN, IN _B to OBN	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	5.8	1.5	5.0	1.5	4.5	ns
tPZH tPZL	Output Enable Time OE _A to OAN, OE _B to OBN		1.5	8.0	1.5	8.0	1.5	6.5	1.5	6.2	ns
tpHZ tPLZ	Output Disable Time OE _A to OAN, OE _B to OBN		1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	ns
tsk(o) ⁽³⁾	Skew between two outputs of same package (same transition)		—	0.7	—	0.7	—	0.5	—	0.5	ns
tsk(p) ⁽³⁾	Skew between opposite transitions (tPHL-tPLH) of the same output		—	1.0	—	0.7	—	0.5	—	0.5	ns
tsk(t) ⁽³⁾	Skew between two outputs of different package at same temperature (same transition)		—	1.5	—	1.2	—	1.0	—	0.8	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).

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Tests Circuits For All Outputs⁽¹⁾



Switch Position

Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

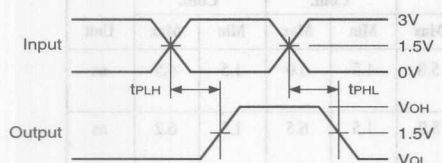
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

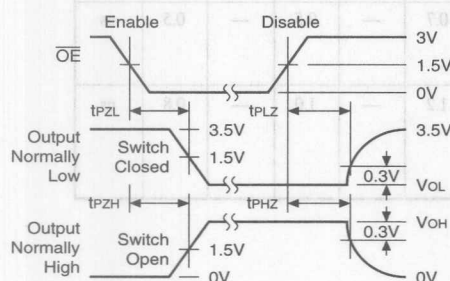
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SWITCHING WAVEFORMS

Propagation Delay



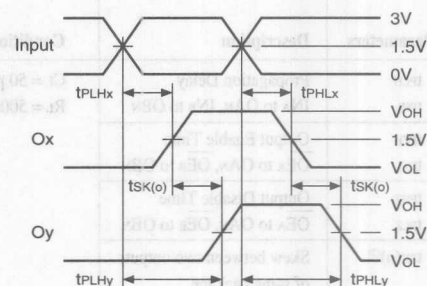
Enable and Disable Times



Test	Switch Position
Disable LOW	3V
Enable LOW	3V
Disable HIGH	GND
Enable HIGH	GND
All Other Inputs	Open

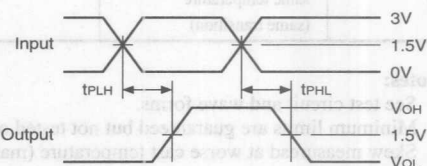
DEFINITIONS:
CL = Load capacitance, includes jig and probe capacitance.
RT = Termination resistance, should be equal to Zout of the Pulse Generator.

Output Skew – tsk(o)



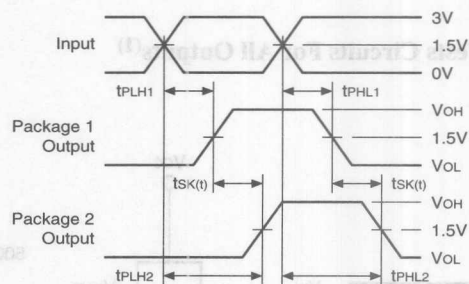
$$tsk(o) = |tPLHy - tPLHx| \text{ or } |tPHLy - tPHLx|$$

Pulse Skew – tsk(p)

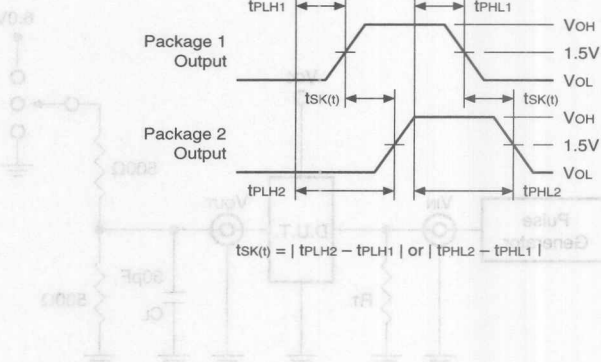


$$tsk(p) = |tPLH - tPLH|$$

Package Skew – tsk(t)



$$tsk(t) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$



Fast CMOS Clock Driver

Product Features:

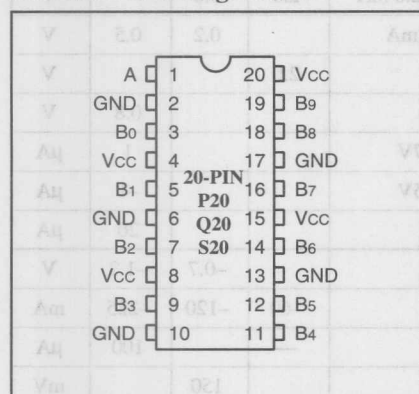
- Guaranteed low skew: 0.35 ns
- Low input capacitance
- Minimum duty cycle distortion
- 1:10 fanout
- High speed: 3.5 ns propagation delay
- TTL input and CMOS output compatible
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- Packages available:
 - 20-pin 300 mil wide DIP (P20)
 - 20-pin 300 mil wide SOIC (S20)
 - 20-pin 150 mil wide QSOP (Q20)

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

This low skew clock driver features one input and ten outputs fanout. The large fanout from a single input line reduces loading on input clock. TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

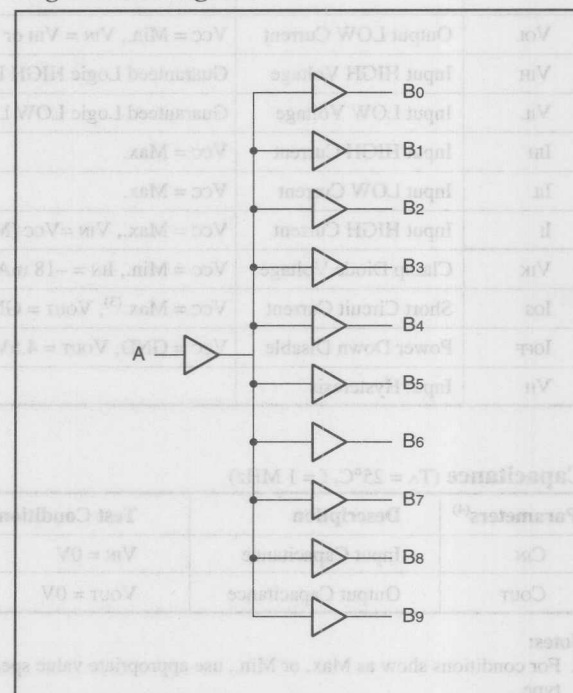
Product Pin Configuration



Product Pin Description

Pin Name	Description
A	Input
B0 – B9	Outputs
GND	Ground
Vcc	Power

Logic Block Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = 0°C to +70°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.3		V
			IOH = -32.0 mA	2.0	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 48 mA		0.2	0.5	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IiH	Input HIGH Current	VCC = Max.	VIN = 2.7V			1	μA
IiL	Input LOW Current	VCC = Max.	VIN = 0.5V			-1	μA
Ii	Input HIGH Current	VCC = Max., VIN = VCC (Max.)				20	μA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA			-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120	-225	mA
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
VH	Input Hysteresis				150		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6.0	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		3	30	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.,	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open 50% Duty Cycle, One Input Toggling	V _{IN} = V _{CC} V _{IN} = GND		0.4	0.6	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _{CP} = 50 MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		20	30 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		20.7	33 ⁽⁵⁾	

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.

2. Typical values are at V_{cc} = 5.0V, +25°C ambient.

3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_C = I_{cc} + ΔI_{cc} D_HN_T + I_{ccD} (f_{CP}/2 + f_IN_I)

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

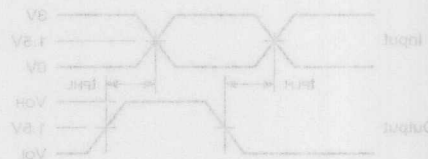
I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.


9
Switching Characteristics over Operating Range

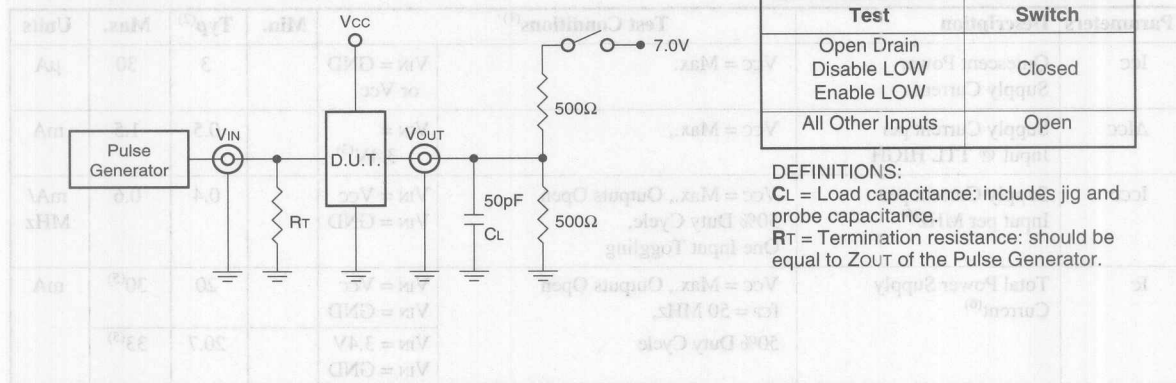
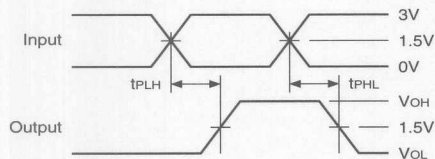
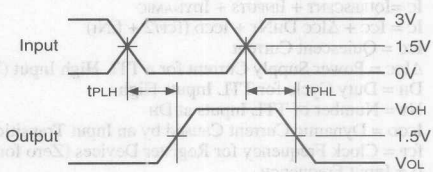
Parameters	Description	Conditions ⁽¹⁾	807T		807AT		807BT		807CT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	4.5	1.5	4.0	1.5	3.8	1.5	3.5	ns
t _{PHL}	A to B _N										
t _{SK(o)}	Skew between two outputs of same package ⁽³⁾		—	0.5	—	0.5	—	0.35	—	0.35	ns
t _{SK(p)}	Skew between opposite transitions of same output (t _{PLH} — t _{PHL}) ⁽³⁾		—	0.5	—	0.5	—	0.35	—	0.35	ns
t _{SK(i)}	Skew between outputs of different package at same power supply, temperature and speed grade ⁽³⁾		—	1.0	—	1.0	—	0.75	—	0.75	ns

Notes:

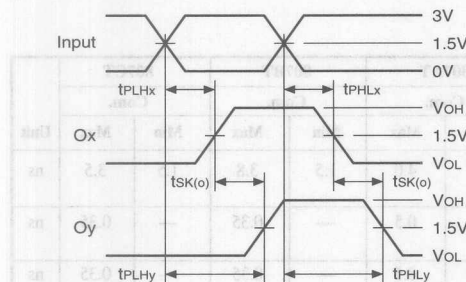
1. See test circuit and wave forms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

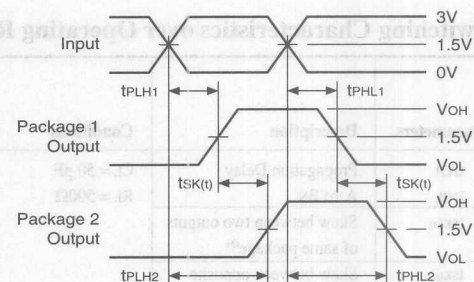
3. This parameter is guaranteed but not tested.

Tests Circuits For All Outputs⁽¹⁾

SWITCHING WAVEFORMS
Propagation Delay

Pulse Skew – tsk(p)


$$tsk(p) = |t_{PLH} - t_{PLL}|$$

Output Skew – tsk(o)


$$tsk(o) = |t_{PLHy} - t_{PLHx}| \text{ or } |t_{PHLy} - t_{PHLx}|$$

Package Skew – tsk(i)


$$tsk(i) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$



PRELIMINARY

PI49FCT3807

3.3V Fast CMOS Clock Driver

Product Features:

- 3.3V version of PI49FCT807
- Ultra low skew: 0.35 ns
- Low input capacitance
- Minimum duty cycle distortion
- 1:10 fanout
- High speed: 3.5 ns propagation delay
- TTL input and CMOS output compatible
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- Packages available:
 - 20-pin 300 mil wide DIP (P20)
 - 20-pin 300 mil wide SOIC (S20)
 - 20-pin 150 mil wde QSOP (Q20)

Product Description:

Pericom Semiconductor's PI49FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI49FCT3807 is a 3.3V 1-to-10 clock driver. This low skew clock driver features one input and ten outputs fanout. The large fanout from a single input line reduces loading on input clock. TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

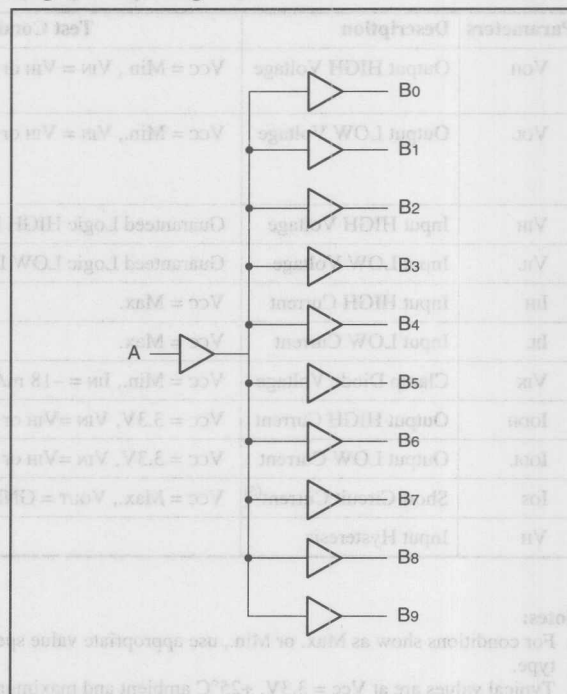
Product Pin Configuration

V	A	1	20	Vcc
GND		2	19	B9
V	B0	3	18	B8
Vcc		4	17	GND
B1	5	16	B7	
GND		6	15	Vcc
B2	7	14	B6	
Vcc		8	13	GND
B3	9	12	B5	
GND		10	11	B4

Product Pin Description

Pin Name	Description
A	Input
B0-B9	Outputs
GND	Ground
Vcc	Power

Logic Block Diagram



9

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Ambient Temperature = 0°C to +70°C
Vcc = 3.3V ± 0.3V

DC Electrical Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -0.1 mA I _{OH} = -8 mA	V _{CC} -0.2 2.4 ⁽³⁾	— 3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1 mA I _{OL} = 16 mA I _{OL} = 24 mA	— — —	— 0.2 0.3	0.2 0.4 0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level (Input Pins)		2.0	—	5.5	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level (Input Pins)		-0.5	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}	—	—	1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND	—	—	-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		—	-0.7	-1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽⁴⁾		-35	-60	-110	mA
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽⁴⁾		50	90	200	mA
I _{OS}	Short Circuit Current ⁽⁵⁾	V _{CC} = Max., V _{OUT} = GND ⁽⁵⁾		-60	-135	-240	mA
V _H	Input Hysteresis			—	150	—	mV

Notes:

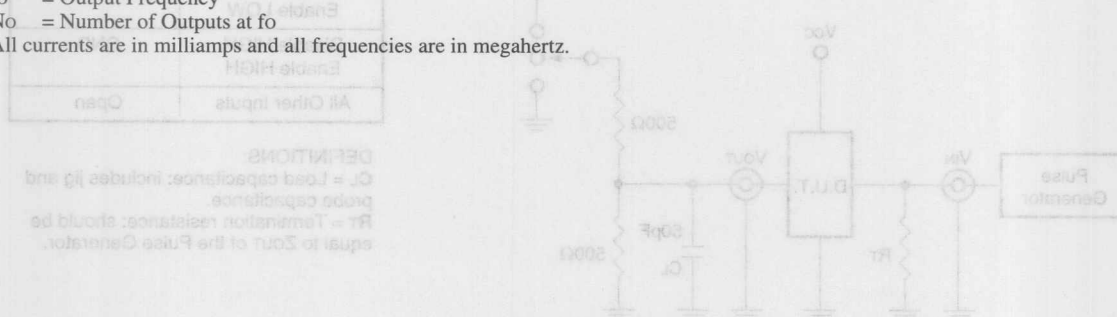
- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
- V_{OH} = V_{CC} - 0.6V at rated current.
- This parameter is determined by device characterization but is not production tested.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}	—	3	30	μA
ΔI _{CC}	Supply Current per Inputs @ TTL HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾	—	2.0	300	μA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open Per Output Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—			mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open fo = 10 MHz 50% Duty Cycle Mon. Output Toggling	V _{IN} = V _{CC} V _{IN} = GND	—			mA
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—			
		V _{CC} = Max., Outputs Open fo = 2.5 MHz 50% Duty Cycle Eleven Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND	—			
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—			

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
 - Typical values are at V_{CC} = 3.3V, +25°C ambient.
 - Per TTL driven input (V_{IN} = V_{CC} - 0.6V); all other inputs at V_{CC} or GND.
 - This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
 - Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (foNo)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} - 0.6V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
fo = Output Frequency
No = Number of Outputs at fo
All currents are in milliamps and all frequencies are in megahertz.



Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

1. This parameter is determined by device characterization but is not production tested.

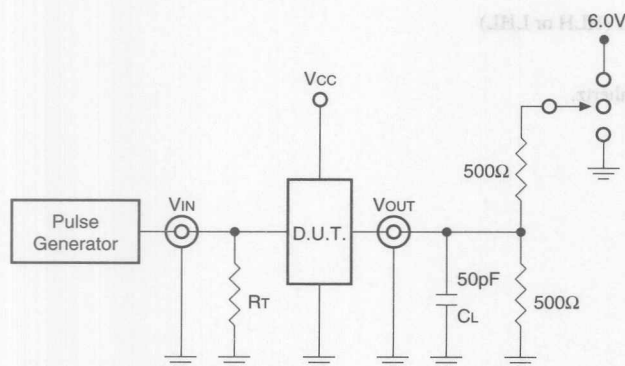
Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	3807T		3807AT		3807BT		3807CT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	C _L = 50 pF R _L = 500Ω	1.5	4.5	1.5	4.0	1.5	3.8	1.5	3.5	ns
tPHL	A TO B _N		—	—	—	—	—	—	—	—	—
tSK(o)	Skew between two outputs of same package ⁽³⁾		—	0.5	—	0.5	—	0.35	—	0.35	ns
tSK(p)	Skew between opposite transitions of same output (tPLH — tPHL) ⁽³⁾		—	0.5	—	0.5	—	0.35	—	0.35	ns
tSK(i)	Skew between outputs of different package at same power supply, temperature and speed grade ⁽³⁾		—	1.0	—	1.0	—	0.75	—	0.75	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Tests Circuits For All Outputs⁽¹⁾



Switch Position

Test	Switch
Disable LOW	6V
Enable LOW	6V
Disable HIGH	GND
Enable HIGH	GND
All Other Inputs	Open

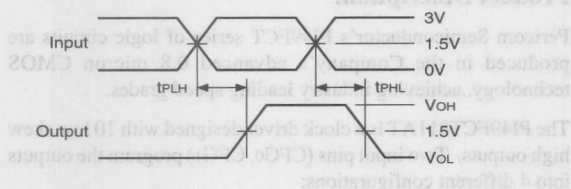
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

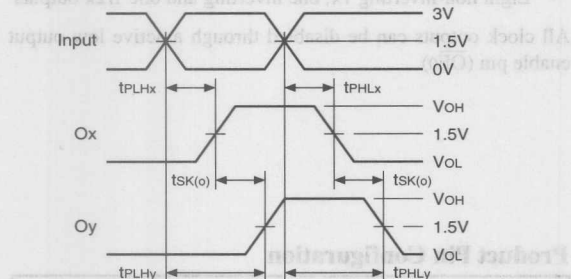
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SWITCHING WAVEFORMS

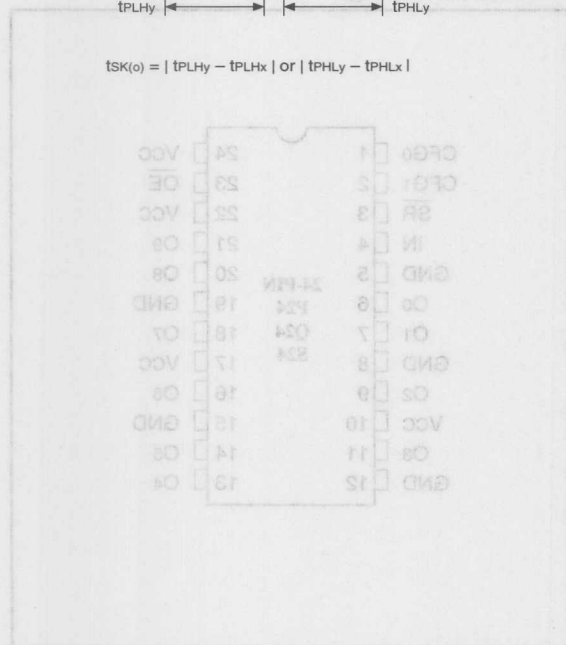
Propagation Delay



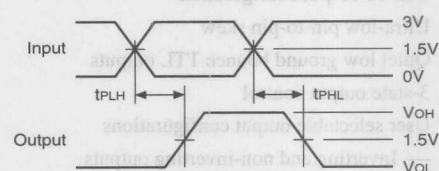
Output Skew – tsk(o)



$$tsk(o) = |tPLHy - tPLHx| \text{ or } |tPHLy - tPHLx|$$

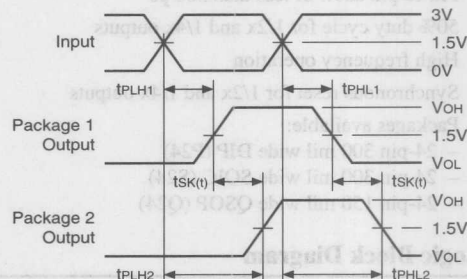


Pulse Skew – tsk(p)

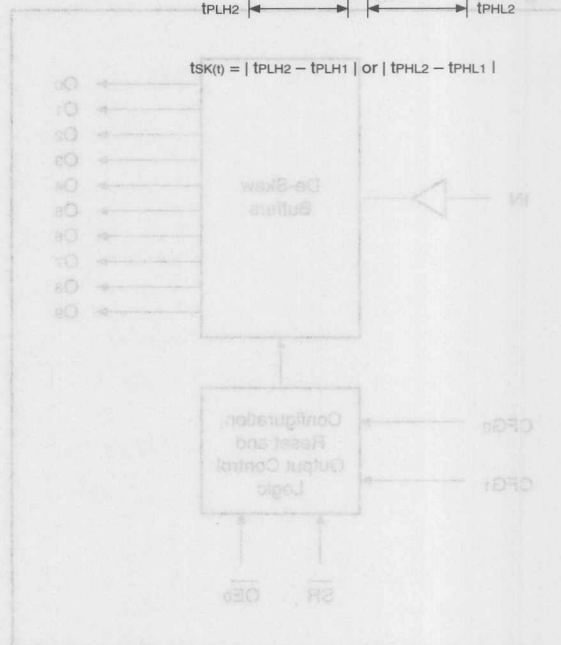


$$tsk(p) = |tPHL - tPLH|$$

Package Skew – tsk(t)



$$tsk(t) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

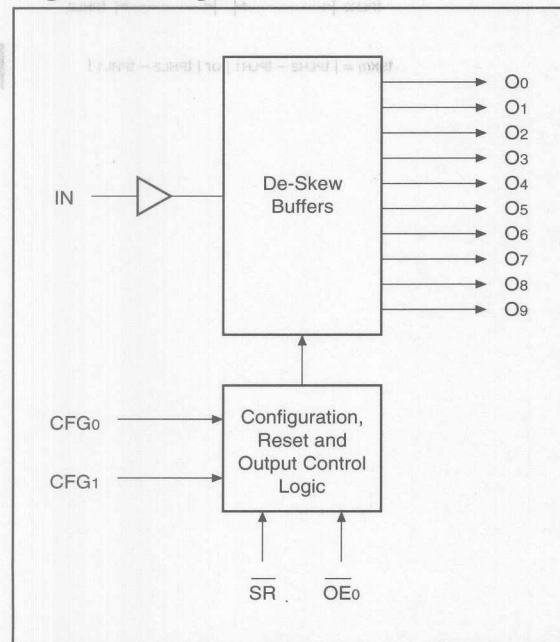


Fast CMOS Programmable Buffer/Clock Driver

Product Features:

- 1-in-10 output configuration
- Ultra-low pin-to-pin skew
- Quiet low ground bounce TTL outputs
- 3-state output control
- User selectable output configurations
 - Inverting and non-inverting outputs
 - 1x, 1/2x and 1/4x outputs
- Low operating current
- High-performance: compatible with the Pentium™ and Power PC™ class of processors
- Pin-to-pin skew of less than 500 ps
- 50% duty cycle for 1/2x and 1/4x outputs
- High frequency operation
- Synchronous reset for 1/2x and 1/4x outputs
- Packages available:
 - 24-pin 300 mil wide DIP (P24)
 - 24-pin 300 mil wide SOIC (S24)
 - 24-pin 150 mil wide QSOP (Q24)

Logic Block Diagram



Product Description:

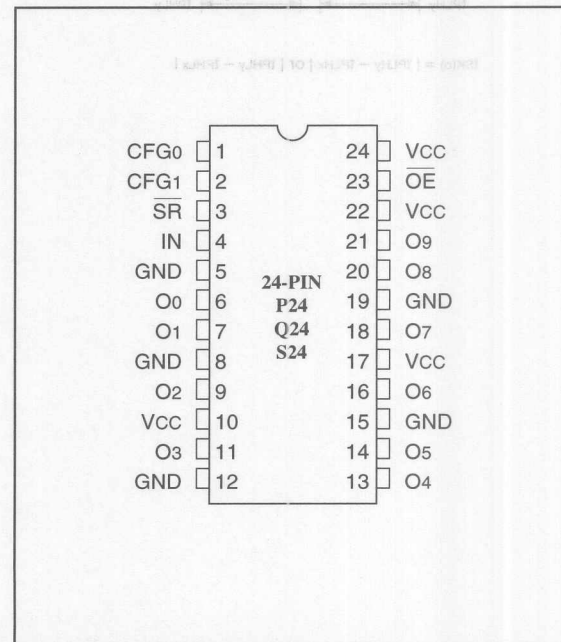
Pericom Semiconductor's PI49FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI49FCT8111AT is a clock driver designed with 10 low skew high outputs. Two input pins (CFG0, CFG1) program the outputs into 4 different configurations:

- Ten non-inverting 1x clock outputs
- Eight non-inverting 1x, two inverting 1x outputs
- Eight non-inverting 1x, one 1/2x and one 1/4x outputs
- Eight non-inverting 1x, one inverting and one 1/2x outputs

All clock outputs can be disabled through a active low output enable pin ($\overline{OE0}$).

Product Pin Configuration



Product Pin Description

Pin Name	Description
CFG0, CFG1	Configuration Pins, see configuration mode truth table for details
SR	Synchronous Reset for 1/2x and 1/4x outputs with respect to the rising edge of clock input (IN). Active LOW
OE0	Output Enable, Active LOW; Outputs become 3-state when OE0 = HIGH
IN	Clock Input
O9-O0	Clock Outputs
GND	Ground
Vcc	Power

Output Configuration Modes

CFG0	CFG1	Output Modes
0	0	Outputs O9-O0 all configure as non-inverting 1x clock outputs
0	1	Outputs O7-O0 are configured as non-inverting 1x clock outputs; Output O8 is configured as inverting 1x; Output O9 is configured as inverting 1x
1	1	Outputs O7-O0 are configured as non-inverting 1x clock outputs; Output O8 is configured as 1/2x; Output O9 is configured as 1/4x
1	0	Outputs O7-O0 are configured as non-inverting 1x clock outputs; Output O9 is configured as inverting 1/2x; Output O8 is configured as non-inverting 1x

9

Parameter ⁽¹⁾	Description	Test Conditions	Typ	Max	Units
C _{in}	Input Capacitance	V _{in} = 0V	6	10	pF
C _{out}	Output Capacitance	V _{out} = 0V	8	12	pF

Notes:
 1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical values are at V_{CC} = 2.0V, +25°C ambient and maximum loading.
 3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
 4. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W
ESD protection	>2000V

NOTE:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -24.0 \text{ mA}$	2.4	3.3		V
V_{OL}	Output LOW Current	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 64 \text{ mA}$		0.3	0.55	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC}$			1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$			-1	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$ $V_{OUT} = V_{CC}$			1	μA
I_{OZL}	Output Current	$V_{OUT} = \text{GND}$			-1	μA
I_I	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC} (\text{Max.})$			20	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_{OUT} = \text{GND}$	-60	-120	-225	mA
V_H	Input Hysteresis	$V_{CC} = 5\text{V}$		200		mV

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{cc} = Max.	V _{IN} = GND or V _{cc}		3	30	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{cc} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{ccD}	Supply Current per Input per MHz ⁽⁴⁾	V _{cc} = Max., Outputs Open OE _A = OE _B = GND Per Output Toggling 50% Duty Cycle	V _{IN} = V _{cc} V _{IN} = GND		0.15	0.25	mA/MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{cc} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle OE _A = OE _B = GND Five Outputs Toggling	V _{IN} = V _{cc} V _{IN} = GND		7.7	14.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		8.0	15.0 ⁽⁵⁾	
		V _{cc} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle OE _A = OE _B = GND Eleven Outputs Toggling	V _{IN} = V _{cc} V _{IN} = GND		4.3	8.4 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		4.8	10.4 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{cc} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{cc} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.
- I_c = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccD} (f_{CP}/2 + f_i N_i)$$

I_{cc} = Quiescent Current
ΔI_{cc} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{ccD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

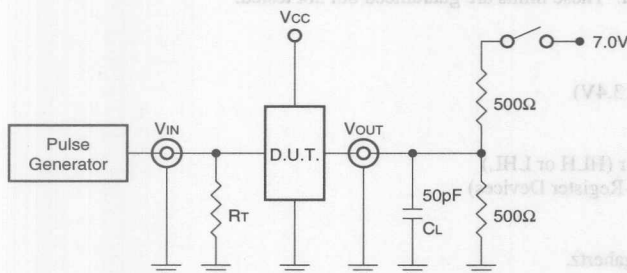
Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	811T		811AT		811BT		Unit
			Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.0	1.5	5.0	ns
tPHL									
tpZH	Output Enable Time		1.5	9.0	1.5	8.0	1.5	7.0	ns
tpZL									
tpHZ	Output Disable Time		1.5	8.0	1.5	7.0	1.5	6.0	ns
tpLZ									
tsU	SR to IN Setup Time		3.0	—	3.0	—	3.0	—	ns
th	SR to IN Hold Time		2.5	—	2.5	—	2.5	—	ns
tsKEW(o) ⁽³⁾	Skew between two outputs of same package (same transition)		—	0.5	—	0.5	—	0.5	ns
tsKEW(p) ⁽³⁾	Skew between opposite transitions (tPHL-tPLH) of the same output		—	0.5	—	0.5	—	0.35	ns
tsKEW(t) ⁽³⁾	Skew between two outputs of different package at same temperature (same transition)		—	1.0	—	1.0	—	1.0	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).

Tests Circuits For All Outputs⁽¹⁾



Switch Position

Test	Switch
Open Drain	Closed
Disable LOW	
Enable LOW	Open
All Other Inputs	

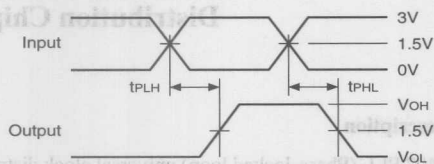
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

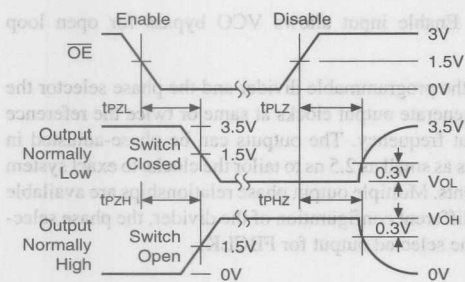
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SWITCHING WAVEFORMS

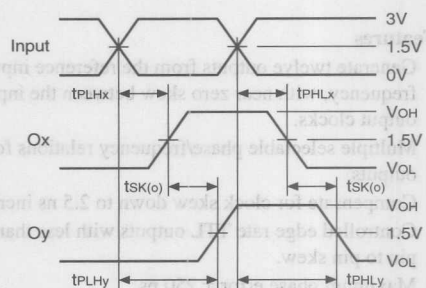
Propagation Delay



Enable and Disable Times

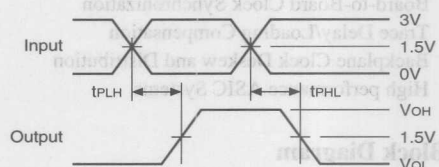


Output Skew - $t_{sk(o)}$



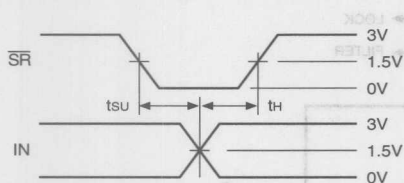
$$t_{sk(o)} = |t_{PLHy} - t_{PLHx}| \text{ or } |t_{PHLy} - t_{PHLx}|$$

Pulse Skew - $t_{sk(p)}$

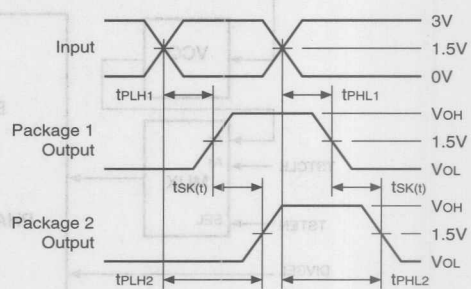


$$t_{sk(p)} = |t_{PHL} - t_{PLH}|$$

Synchronous Reset, Setup and Hold Times



Package Skew - $t_{sk(i)}$



$$t_{sk(i)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

BiCMOS PLL Universal Clock Distribution Chip

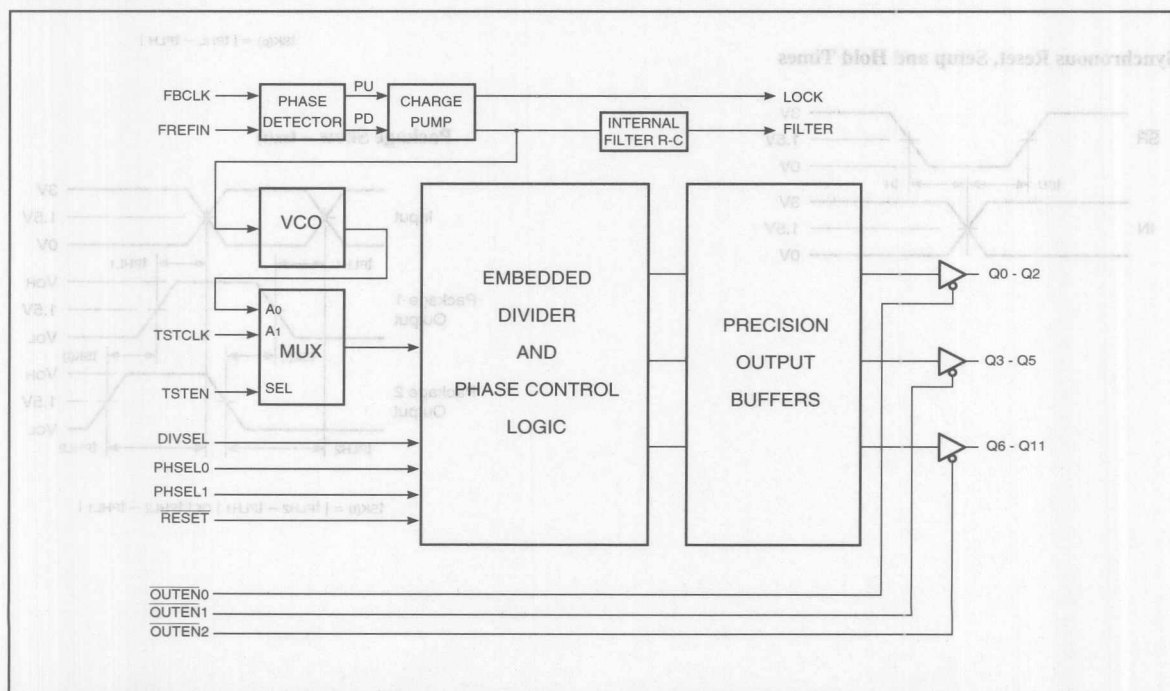
Features

- Generate twelve outputs from the reference input clock frequency, with near zero skew between the input and output clocks.
- Multiple selectable phase/frequency relations for the clock outputs.
- Compensate for clock skew down to 2.5 ns increments.
- Controlled edge rate TTL outputs with less than ± 250 ps pin to pin skew.
- Maximum phase error ± 250 ps.
- Proven 0.8-micron BiCMOS technology.
- Single +5V power supply operation
- 44 pin PLCC package.

Applications

- High-speed Microprocessor Systems
- Board-to-Board Clock Synchronization
- Trace Delay/Loading Compensation
- Backplane Clock Deskew and Distribution
- High performance ASIC Systems

Block Diagram



Functional Description

The PI6B2407 clock generator provides multiple outputs synchronized both in frequency and phase to a periodic clock signal input that is synthesized on the chip. An external feedback of a PLL and two select pins allow the user to phase-adjust the twelve outputs relative to the input clock.

PIN DESCRIPTIONS

Input Signals

FREFIN. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the Q0-Q11 outputs.

FBCLK. Feedback clock that, along with the FREFIN input, determines the frequency of the Q0-Q11 outputs. One output is selected to feed back to this input.

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by eight. When DIVSEL is high, the VCO frequency is divided by 16.

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q0-Q2

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q3-Q5

OUTEN2. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q6-Q11

RESET. Active Low. Initializes internal states for test purposes.

TSTCLK. Replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

TSTEN. Active High. Allows TSTCLK to drive the divider and phase adjust circuitry.

The phase selection inputs PHSEL0 and PHSEL1 allow the user to select different phase relations among the 12 TTL clock outputs.

For more information, contact factory.

Output Signals

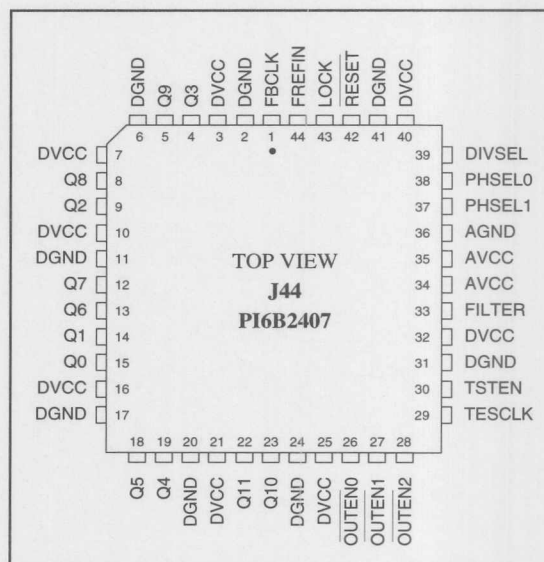
FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and two capacitors) to be included in the PLL.

Q0 - Q2. 1X Clock outputs.

Q3 - Q5. 1X or 2X Clock outputs.

Q6 - Q11. 1X or 2X Clock outputs.

LOCK. Goes high when FREFIN and FBCLK are in steady-state phase and frequency lock, demonstrating that the PLL is in lock.



Functional Description

The PI6B2407 clock generator provides multiple outputs synchronized both in frequency and phase to a periodic clock signal input that is synchronized on the chip. An external feedback of a PLL and two select pins allow the user to phase-adjust the twelve outputs relative to the input clock.

PIN DESCRIPTIONS

Input Signals

FRETN. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the Q0-Q11 outputs.

FBCLK. Feedback clock that, along with the FRETN input, determines the frequency of the Q0-Q11 outputs. One output is selected to feed back to this input.

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by eight. When DIVSEL is high, the VCO frequency is divided by 16.

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q0-Q3.

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q3-Q5.

OUTEN2. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q6-Q11.

RESET. Active Low. Initializes internal states for test purposes.

TESTCLK. Replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

TSTEN. Active High. Allows TESTCLK to drive the divider and phase adjust circuitry.

The phase selection inputs PHSEL0 and PHSEL1 allow the user to select different phase relations among the 12 TTL clock outputs.

For more information, contact factory.

Output Signals

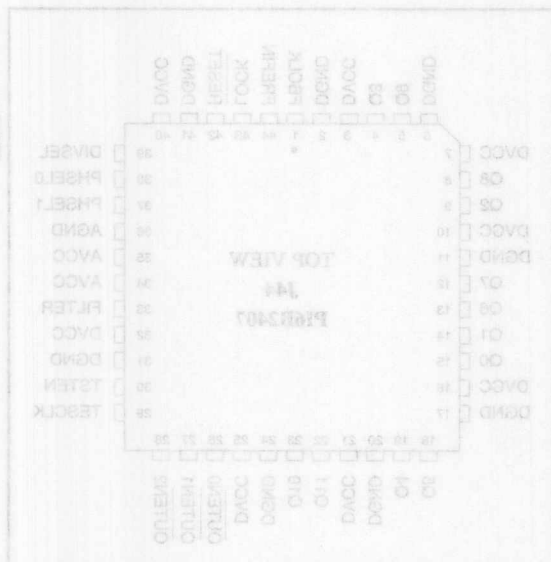
FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and two capacitors) to be included in the PLL.

Q0-Q3. 1X Clock outputs.

Q3-Q5. 1X or 2X Clock outputs.

Q6-Q11. 1X or 2X Clock outputs.

LOCK. Goes high when FRETN and FBCLK are in steady-state phase and frequency lock, demonstrating that the PLL is in lock.



GENERAL INFORMATION**1****STANDARD AND 25Ω OUTPUT RESISTOR SERIES
5V FCT LOGIC PRODUCTS****2****DOUBLE DENSITY STANDARD
5V FCT LOGIC PRODUCTS****3****DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS****4****STANDARD 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****5****DOUBLE DENSITY 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****6****SPECIALTY LOGIC PRODUCTS****7****BUS SWITCH PRODUCTS****8****CLOCK DISTRIBUTION PRODUCTS****9****CLOCK GENERATOR PRODUCTS****10****NETWORKING PRODUCTS****11****APPLICATION NOTES****12****QUALITY AND RELIABILITY INFORMATION****13****PACKAGE MECHANICAL OUTLINES****14****SALES AND DISTRIBUTION LOCATIONS****15**

CLOCK GENERATOR**PRODUCTS****TABLE OF CONTENTS**

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PI6C9108-05	Low Cost 3V 8-Pin CPU Frequency Generator	10.5
PI6C9155U-01	20-Pin CPU Frequency Generator	10.11
PI6C9155U-02	20-Pin CPU Frequency Generator	10.11
PI6C9155U-03	20-Pin CPU Frequency Generator	10.11
PI6C9155W-01	20-Pin CPU Frequency Generator	10.11
PI6C9155W-02	20-Pin CPU Frequency Generator	10.11
PI6C9155W-03	20-Pin CPU Frequency Generator	10.11
PI6C9156U-01	3V 20-Pin CPU Frequency Generator	10.22
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PI6C462	28-Pin Motherboard Clock Generator	10.29
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PI6C471	28-Pin Motherboard Clock Generator	10.44

Low Cost CPU Frequency Generator

Features

- Pin compatible with Avasem AV9107-03
- Generate popular 12 CPU clocks and the reference clock 14.318 MHz
- Generate all the CPU Clocks for 286, 386, 486, and Pentium CPU
- Replace two crystal oscillators, for cost savings and board space savings
- On-chip loop filter — no external loop filter circuit
- Low power CMOS technology
- ESD protection exceeds 2000V
- Single +5V power supply operation
- Packages available:
 - 14-pin 300 mil wide plastic DIP (P14)
 - 14-pin 150 mil wide plastic SOIC (W14)

General Description

The PI6C9107U CPU clock generator provides a small footprint solution for generating two simultaneous clocks. The first clock CLK1 is user selectable from one of the four popular CPU frequencies, by selecting two selection signals FS1 and FS0. The second clock REFCLK is a fixed clock frequency, identical to the input reference clock.

The device includes on-chip loop filter circuit, for simplifying the board design. An external loop filter circuit is no longer needed. The output drive characteristics are also improved.

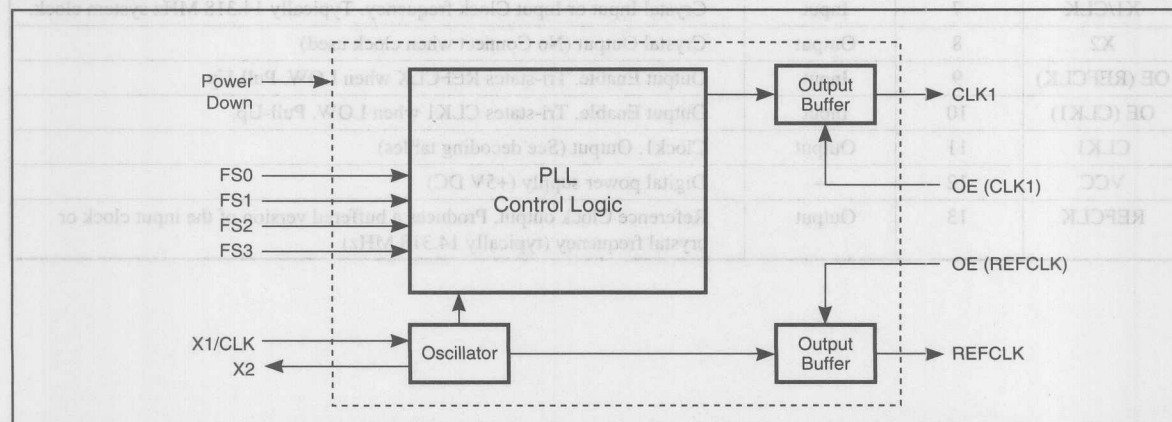
Enhanced versions with customized frequencies and features are also available. Contact factory for the enhanced versions.

Applications

CPU — The PI6C9107U is an ideal substitute for metal-can oscillators, for cost savings and board space savings. It offers additional features of reducing the operating clock speeds for saving power of the entire computer while the computer is idling. This feature cannot be accomplished by metal-can oscillators. A smooth, jitter-free frequency transition is provided for the CPU clock during slow down and speed up. The frequency transition rates are meeting the specifications of all 386DX, 386SX, 486DX, 486DX2, 486DX4 and 486SX.

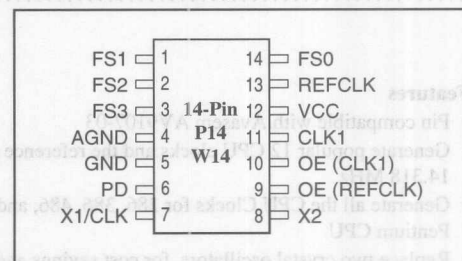
Peripherals — The device is also an ideal substitute for metal-can oscillators on disk drive controllers, laser printer controllers, and other peripherals controllers. Contact factory for the custom frequencies required.

Block Diagram

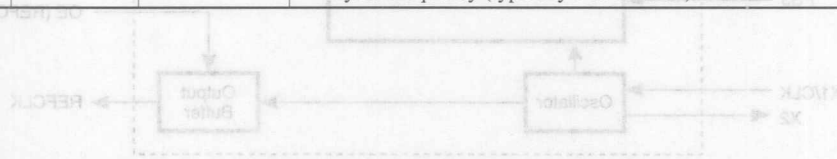


Decoding Table (14.318 MHz Input)

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16 MHz
0	0	0	1	40 MHz
0	0	1	0	50 MHz
0	0	1	1	80 MHz
0	1	0	0	66.66 MHz
0	1	0	1	100 MHz
0	1	1	0	8 MHz
0	1	1	1	4 MHz
1	0	0	0	8 MHz
1	0	0	1	20 MHz
1	0	1	0	25 MHz
1	0	1	1	40 MHz
1	1	0	0	33.33 MHz
1	1	0	1	50 MHz
1	1	1	0	4 MHz
1	1	1	1	2 MHz

Product Pin Configuration

Product Pin Description

Pin Name	Pin No.	Pin Type	Description
FS0	14	Input	Frequency Select 0 for CLK1 (with Pull-Up)
FS1	1	Input	Frequency Select 1 for CLK1 (with Pull-Up)
FS2	2	Input	Frequency Select 2 for CLK1 (with Pull-Up)
FS3	3	Input	Frequency Select 3 for CLK1 (with Pull-Up)
AGND	4	—	Analog Ground
GND	5	—	Digital Ground
PD	6	Input	Power Down. Shuts off chip when LOW. Internal Pull-Up.
X1/CLK	7	Input	Crystal Input or Input Clock frequency. Typically 14.318 MHz system clock.
X2	8	Output	Crystal Output (No Connect when clock used)
OE (REFCLK)	9	Input	Output Enable. Tri-states REFCLK when LOW. Pull-Up.
OE (CLK1)	10	Input	Output Enable. Tri-states CLK1 when LOW. Pull-Up.
CLK1	11	Output	Clock1. Output (See decoding tables)
VCC	12	—	Digital power supply (+5V DC)
REFCLK	13	Output	Reference Clock output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Output Current	120 mA
Operating Range: Ambient Temperature	0°C to +70°C
Operating Range: Vcc	5V ±5%
Power Dissipation	0.5W
ESD protection	>2000V

NOTE:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics at 5V (Operating Range, Vcc = +4.5V to +5.5V, Temperature 0°C to +70°C)

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage	Vcc = Min., VIN = VIH or VIL	IOH = -4 mA	2.4			V
VOL	Output LOW Voltage	Vcc = Min., VIN = VIH or VIL	IOL = 8 mA			0.4	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	Vcc = 5V	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level	Vcc = 5V			0.8	V
IIH	Input HIGH Current	Vcc = Max., VIN = Vcc				5	μA
IIL	Input LOW Current	Vcc = Max., VIN = 0V				-5	μA
Icc	Supply Current ⁽¹⁾				10	20	mA
Icc2	Standby Supply Current ⁽²⁾				25		μA
Fd	Output Freq. Change ⁽³⁾	With Respect to Typical Frequency			0.002	0.01	%
CI	Input Capacitance	Except X1, X2				10	pF
CL	Load Capacitance	Pins X1, X2			20		pF

Notes:

1. PI6C9107U-03 with no load, with 14.318 MHz crystal input and CLK1 running at 40 MHz.
Power supply current varies with frequency. Consult factory for actual current at different frequencies.
2. PI6C9107U-03 with power down pin LOW (active).
3. Over Supply and Temperature.

AC Electrical Characteristics at 5V (Operating Range, Vcc = +4.5V to +5.5V, Temperature 0°C to +70°C)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
fo	Output Frequency		2		120	MHz
fi	Input Frequency		2	14.318	32	MHz
ICLK _R	Input Clock Rise Time				20	ns
ICLK _F	Input Clock Fall Time				20	ns
tr	Output Rise Time, 0.8 to 2.0V	25 pF Load			2	ns
tr	Rise Time, 20% to 80% Vcc	25 pF Load		2	4	ns
tf	Output Fall Time, 2.0 to 0.8V	25 pF Load			2	ns
tf	Fall Time, 80% to 20% Vcc	25 pF Load			4	ns
dt	Duty Cycle, CPU	15 pF Load	40	50/50	60	%
T _{JIS}	Jitter, 1 Sigma	All Frequencies		±0.5	±2	%
T _{JABS}	Jitter, Absolute	All Frequencies		±3	±5	%
t _{FT}	Frequency Transition Time	From 50 to 4 MHz			20	ms
t _{PU}	Power Up Time	From Off to 100 MHz			2	ms

ACTUAL FREQUENCIES
PI6C9107U-03 Decoding Table (14.318 MHz Input)

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	39.99 MHz
0	0	1	0	50.11 MHz
0	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	8.02 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.00 MHz
1	0	1	0	25.06 MHz
1	0	1	1	40.01 MHz
1	1	0	0	33.29 MHz
1	1	0	1	50.11 MHz
1	1	1	0	4.01 MHz
1	1	1	1	2.05 MHz



PI6C9107U-05

Low Cost CPU Frequency Generator

Features

- Pin compatible with Avasec AV9107-05.
- Generate popular CPU clocks — 40, 50, 66.6, 80 MHz and the reference clock 14.318 MHz
- Generate all the CPU Clocks for 286, 386, 486, and Pentium CPU
- Replace two crystal oscillators, for cost savings and board space savings
- On-chip loop filter — no external loop filter circuit
- Low power CMOS technology
- ESD protection exceeds 2000V
- Single +5V power supply operation
- Packages available:
 - 8-pin 300 mil wide plastic DIP (P8)
 - 8-pin 150 mil wide plastic SOIC (W8)

General Description

The PI6C9107U CPU clock generator provides a small footprint solution for generating two simultaneous clocks. The first clock CLK1 is user selectable from one of the four popular CPU frequencies, by selecting two selection signals FS1 and FS0. The second clock REFCLK is a fixed clock frequency, identical to the input reference clock.

The device includes on-chip loop filter circuit, for simplifying the board design. An external loop filter circuit is no longer needed. The output drive characteristics are also improved.

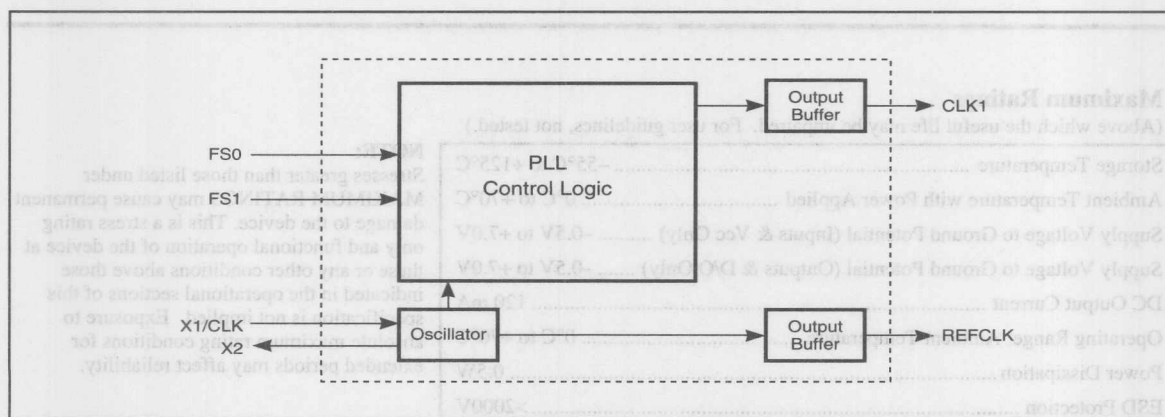
Enhanced versions with customized frequencies and features are also available. Contact factory for the enhanced versions.

Applications

CPU — The PI6C9107U is an ideal substitute for metal-can oscillators, for cost savings and board space savings. It offers additional features of reducing the operating clock speeds for saving power of the entire computer while the computer is idling. This feature cannot be accomplished by metal-can oscillators. A smooth, jitter-free frequency transition is provided for the CPU clock during slow down and speed up. The frequency transition rates are meeting the specifications of all 386DX, 386SX, 486DX, 486DX2, and 486SX.

Peripherals — The device is also an ideal substitute for metal-can oscillators on disk drive controllers, laser printer controllers, and other peripherals controllers. Contact factory for the custom frequencies required.

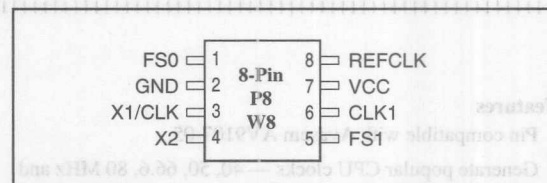
Block Diagram



PI6C9107U-05 Decoding Table (14.318 MHz Input)

FS1	FS0	CLK1
0	0	40 MHz
0	1	50 MHz
1	0	66.6 MHz
1	1	80 MHz

PI6C9107U-05 Product Pin Configuration



PI6C9107U-05 Product Pin Description

Pin Name	Pin No.	Pin Type	Description
FS0	1	Input	Frequency Select 0 for CLK1
GND	2	—	Digital Ground
X1/CLK	3	Input	Crystal Input or Input Clock frequency. Typically 14.318 MHz system clock
X2	4	Output	Crystal Output (No Connect when clock used)
FS1	5	Input	Frequency Select 1 for CLK1
CLK1	6	Output	Clock1 Output (see matrix tables)
VCC	7	—	Digital power supply (+5V DC)
REFCLK	8	Output	Reference Clock output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz)

ACTUAL FREQUENCIES

PI6C9107U-05 Decoding Table (14.318 MHz Input)

FS1	FS0	CLK1
0	0	40.09 MHz
0	1	50.11 MHz
1	0	66.82 MHz
1	1	80.18 MHz

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Output Current	120 mA
Operating Range: Ambient Temperature	0°C to +70°C
Power Dissipation	0.5W
ESD Protection	>2000V

NOTE:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics at 5V (Operating Range, $V_{CC} = +4.5V$ to $+5.5V$, Temperature $0^{\circ}C$ to $+70^{\circ}C$)

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8 \text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 8 \text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	$V_{CC} = 5V$	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	$V_{CC} = 5V$			0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$				5	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = 0V$				-5	μA
I_{CC}	Supply Current ⁽¹⁾				10	20	mA
F_D	Output Freq. Change ⁽²⁾	With Respect to Typical Frequency			0.002	0.01	%
C_i	Input Capacitance	Except X1, X2				10	pF
C_L	Load Capacitance	Pins X1, X2			20		pF

Notes:

- PI6C9107U-05 with no load, with 14.318 MHz crystal input and CLK1 running at 40 MHz.
Power supply current varies with frequency. Consult factory for actual current at different frequencies.
- Over Supply and Temperature.

AC Electrical Characteristics at 5V (Operating Range, $V_{CC} = +4.5V$ to $+5.5V$, Temperature $0^{\circ}C$ to $+70^{\circ}C$)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
ICL_{KR}	Input Clock Rise Time				20	ns
ICL_{KF}	Input Clock Fall Time				20	ns
t_r	Output Rise Time, 0.8 to 2.0V	25 pF Load			2	ns
t_R	Rise Time, 20% to 80% V_{CC}	25 pF Load		2	4	ns
t_f	Output Fall Time, 2.0 to 0.8V	25 pF Load			2	ns
t_F	Fall Time, 80% to 20% V_{CC}	25 pF Load			4	ns
d_T	Duty Cycle, CPU	15 pF Load	40	50/50	60	%
T_{JIS}	Jitter, 1 Sigma	All Frequencies		± 0.5	± 2	%
T_{JABS}	Jitter, Absolute	All Frequencies		± 3	± 5	%
t_{FT}	Frequency Transition Time ⁽¹⁾				20	ms
t_{PU}	Power Up Time ⁽¹⁾				2	ms

Note:

- Guaranteed by design only.

Low Cost 3V 8-Pin CPU Frequency Generator

Features

- 3V version of PI6C9107U-05
- Generate popular CPU clocks — 40, 50, 66.6, 80 MHz, and the reference clock 14.318 MHz
- Generate all the CPU Clocks for 286, 386, 486, and Pentium CPU
- Replace two crystal oscillators, for cost savings and board space savings
- On-chip loop filter — no external loop filter circuit.
- Low power CMOS technology
- ESD protection exceeds 2000V
- Package available:
 - 8-pin 300 mil wide DIP (P8)
 - 8-pin 150 mil wide SOIC (W8)

General Description

The PI6C9108-05 CPU clock generator provides a small foot-print solution for generating two simultaneous clocks. The first clock CLK1 is user selectable from one of the four popular CPU frequencies, by selecting two selection signals FS1 and FS0. The second clock REFCLK is a fixed clock frequency, identical to the input reference clock.

The device includes on-chip loop filter circuit, for simplifying the board design. An external loop filter circuit is no longer needed. The output drive characteristics are also improved.

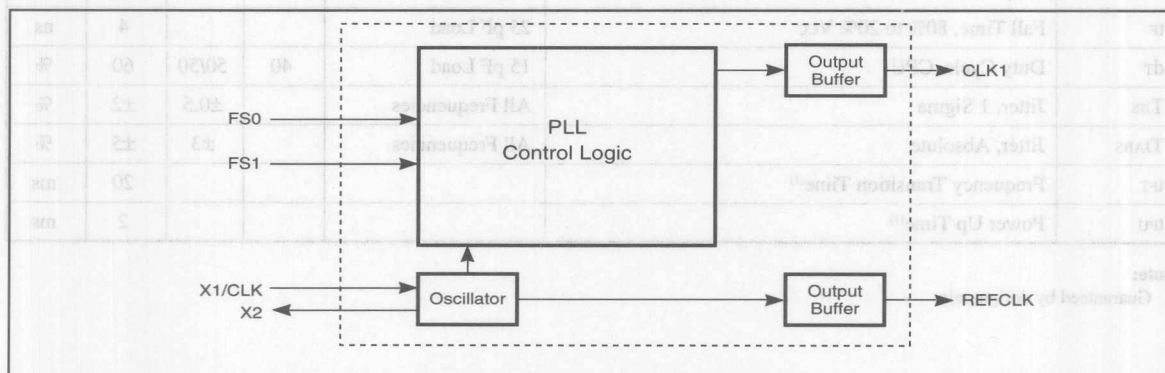
Enhanced versions with customized frequencies and features are also available. Contact factory for the enhanced versions.

Applications

CPU — The PI6C9108-05 is an ideal substitute for metal-can oscillators, for cost savings and board space savings. It offers additional features of reducing the operating clock speeds for saving power of the entire computer while the computer is idling. This feature cannot be accomplished by metal-can oscillators. A smooth, jitter-free frequency transition is provided for the CPU clock during slow down and speed up. The frequency transition rates are meeting the specifications of all 386DX, 386SX, 486DX, 486DX2, and 486SX.

Peripherals — The device is also an ideal substitute for metal-can oscillators on disk drive controllers, laser printer controllers, and other peripherals controllers. Contact factory for the custom frequencies required.

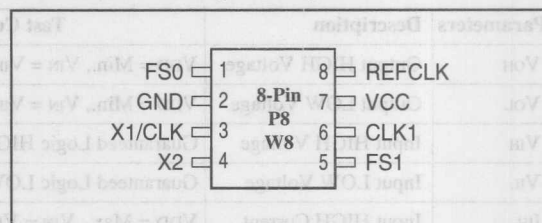
Block Diagram



**PI6C9108-05 Decoding Table,
14.318 MHz Input**

FS1	FS0	CLK1
0	0	40 MHz
0	1	50 MHz
1	0	66.6 MHz
1	1	80 MHz

Product Pin Configuration, PI6C9108-05



PI6C9108-05 Product Pin Description

Pin Name	Pin Number	Pin Type	Description
FS0	1	Input	Frequency Select 0 for CLK1
FS1	5	Input	Frequency Select 1 for CLK1
GND	2	—	Digital Ground
X1/CLK	3	Input	Crystal Input or Input Clock frequency. Typically 14.318 MHz system clock
X2	4	Output	Crystal Output (No Connect when clock used)
CLK1	6	Output	Clock1 Output (see matrix tables)
VDD	7	—	Digital power supply (+3V DC)
REFCLK	8	Output	Reference Clock output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & VDD Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Output Current	120 mA
Operating Range: Ambient Temperature	0°C to +70°C
Power Dissipation	0.5W

NOTE:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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ACTUAL FREQUENCIES

**PI6C9108-05 Decoding Table,
14.318 MHz Input**

FS1	FS0	CLK1
0	0	40.01 MHz
0	1	50.11 MHz
1	0	66.82 MHz
1	1	80.01 MHz

DC Electrical Characteristics at 3.3V (Operating Range, $V_{DD} = +3.3V \pm 0.3V$, Temperature $0^{\circ}C$ to $+70^{\circ}C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -4 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 8 \text{ mA}$		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level,	$V_{DD} = 3.3V$	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	$V_{DD} = 3.3V$		0.8	V
I_{IH}	Input HIGH Current	$V_{DD} = \text{Max.}, V_{IN} = V_{DD}$			5	μA
I_{IL}	Input LOW Current	$V_{DD} = \text{Max.}, V_{IN} = 0V$			-5	μA
I_{CC}	Supply Current ⁽¹⁾			10	20	mA
F_D	Output Freq. Change ⁽²⁾	With Respect to Typical Frequency		0.002	0.01	%
C_I	Input Capacitance	Except X1, X2			10	pF
C_L	Load Capacitance	Pins X1, X2		20		pF

Notes:

- PI6C9108-05 with no load, with 14.318 MHz crystal input and CLK1 running at 40 MHz.
Power supply current varies with frequency. Consult factory for actual current at different frequencies.
- Over Supply and Temperature.

AC Electrical Characteristics at 3.3V (Operating Range, $V_{DD} = +3.3V \pm 0.3V$, Temperature $0^{\circ}C$ to $+70^{\circ}C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
ICLK _R	Input Clock Rise Time				20	ns
ICLK _F	Input Clock Fall Time				20	ns
t_R	Output Rise Time, 0.8V to 2.0V	15 pF Load			2	ns
t_R	Rise Time, 20% to 80% V_{CC}	15 pF Load		2	4	ns
t_F	Output Fall Time, 2.0V to 0.8V	15 pF Load			2	ns
t_F	Fall Time, 80% to 20% V_{CC}	15 pF Load			4	ns
d_T	Duty Cycle, CPU	15 pF Load	40	50/50	60	%
T_{JIS}	Jitter, 1 Sigma	All Frequencies		± 0.5	± 2	%
T_{JABS}	Jitter, Absolute	Above 16 MHz		± 3	± 5	%
t_{FT}	Frequency Transition Time ⁽¹⁾				20	ms
t_{PU}	Power Up Time ⁽¹⁾				2	ms

Note:

- Guaranteed by design only.



PI6C9155U-01 PI6C9155W-01
PI6C9155U-02 PI6C9155W-02
PI6C9155U-03 PI6C9155W-03

Features

- Pin-to-Pin compatible with Avasem AV9155
- A new **Frequency Acceleration** feature for frequency margin tests
- A single-line soft power-down feature simplifying Green-PC power saving logic (PI6C9155W only)
- Generates most essential clock signals for CPU boards
- Generates five simultaneous clock signals for most peripheral controllers
- Replaces six crystal oscillators, for cost savings and board space savings
- On-chip loop filters — no external loop filter circuit
- Smooth jitter-free transition between two CPU frequencies for power savings
- Duty cycle of 50%
- Single low cost (14.318 MHz) crystal as reference input frequency
- Low power 0.8 micron CMOS technology
- Packages available:
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 300 mil wide plastic SOIC (S20)

General Description

The PI6C9155 clock generator provides a low cost solution for generating most of the necessary clock frequencies for motherboards, for tremendous cost and board savings.

The two main clock outputs CPU and 2XCPU can be set by the user to one of several popular processor clock frequencies. It also offers four simultaneous clocks for popular peripherals, plus two reference clock outputs which are identical to the reference input crystal frequency.

The device has an advanced feature of **Frequency Acceleration** as described in the following section.

CPU Frequency Generator

The device has other advanced features which include on-chip filter circuits, for simplifying the board design, and hard power-down capacity for power savings. Enhanced versions with customized frequencies and features are also available. Contact the factory for the enhanced versions.

The CPU and 2XCPU clocks offer an additional feature of reducing the operating clock speeds for saving power of the entire computer while the computer is at idle. This feature cannot be accomplished by metal-can oscillators. A smooth, jitter-free frequency transition is provided for the CPU and 2XCPU clocks during the transition of slow down and speed up. The frequency transition rates meet the specifications of all x86 microprocessors to within 0.1% frequency change per clock period.

With the added frequency acceleration feature, the PI6C9155U-01/02/03 still maintain the pin-to-pin compatibility with Avasem AV9155-01/02/03 devices. The PI6C9155W-01/02/03 replace the hard power-down PD at pin 12 with a single line soft power-down SPD.

Frequency Acceleration

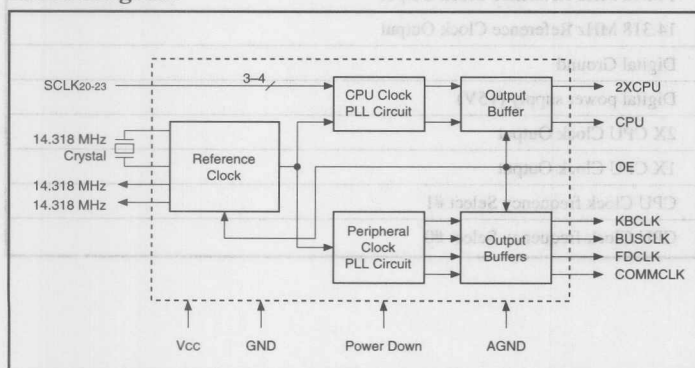
Pericom has been working closely with many customers to add advanced features while maintaining the compatibility with the industry standard frequency generators.

One of the advanced features is to provide the powerful frequency margin tests to all the production motherboards at no additional cost, to minimize production board burn-in time, and reduce manufacturing costs. This feature increases the selected CPU frequency by a small margin. A motherboard design engineer also finds frequency acceleration a useful tool to thoroughly evaluate the margins of his/her design.

Frequency margin test features are provided in Pericom's PI6C9155U and PI6C9155W. Please contact the factory for a detailed description.

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Block Diagram



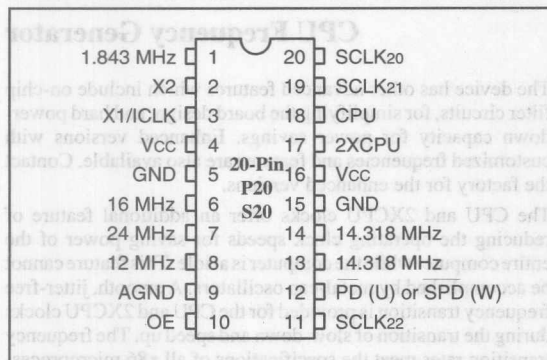
Clock Table (MHz)

Clock	PI6C9155U/W-01	PI6C9155U/W-02
KBCLK	12	12
BUSCLK	16	32
FDCLK	24	24
COMMCLK	1.84	1.84
14.318 (2)	14.318	14.318
CPUCCLK	4, 8, 16, 20, 25, 33.3, 40, or 50	
2XCPUCCLK	8, 16, 32, 40, 50, 66.6, 80, or 100	

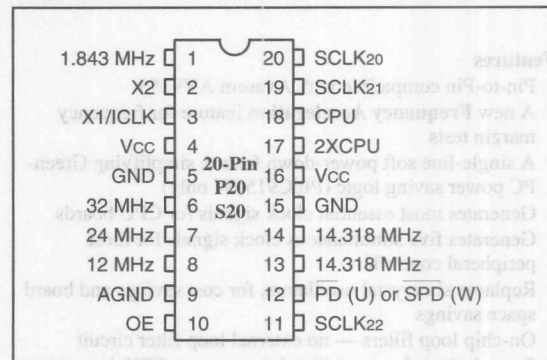


PI6C9155U-01 PI6C9155W-01
PI6C9155U-02 PI6C9155W-02
PI6C9155U-03 PI6C9155W-03
CPU FREQUENCY GENERATOR

Product Pin Configuration, PI6C9155U/W-01



Product Pin Configuration, PI6C9155U/W-02



PI6C9155U/W-01, PI6C9155U/W-02 Product Pin Description

Pin Name	Pin Number	Pin Type	Description
1.843 MHz	1	Output	1.84 MHz Clock Output
X2	2	Output	Crystal connection. Leave as NC for clock input
X1/ICLK	3	Input	Crystal connection/Input Clock
Vcc	4	—	Digital power supply (+5V)
GND	5	—	Digital Ground
16 MHz/32 MHz	6	Output	16 MHz (PI6C9155-01) or 32 MHz (PI6C9155-02) Clock Output
24 MHz	7	Output	24 MHz Floppy disk/Combination I/O Clock Output
12 MHz	8	Output	12 MHz Keyboard Clock Output
AGND	9	—	Analog Ground (Original version)
OE	10	Input	OE = 1: Output Enable. OE = 0: Tri-states all outputs when low.
SCLK22	11	Input	CPU Clock frequency Select #2
PD	12	Input	Hard Power-Down. Shuts off entire chip when low (9155U-01/02/03)
SPD	12	Input	Soft Power-Down when LOW (9155W-01/02/03 version)
14.318 MHz	13	Output	14.318 MHz Reference Clock Output
14.318 MHz	14	Output	14.318 MHz Reference Clock Output
GND	15	—	Digital Ground
Vcc	16	—	Digital power supply (+5V)
2XCPU	17	Output	2X CPU Clock Output
CPU	18	Output	1X CPU Clock Output
SCLK21	19	Input	CPU Clock frequency Select #1
SCLK20	20	Input	CPU Clock frequency Select #0



PI6C9155U-01 PI6C9155W-01
PI6C9155U-02 PI6C9155W-02
PI6C9155U-03 PI6C9155W-03
CPU FREQUENCY GENERATOR

PI6C9155U/W-01 Decoding and Clock Tables
(14.318 MHz Input. All frequencies in MHz)

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17) Pin 10 = 1	CPU (Pin 18) Pin 10 = 1
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100	50

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

PI6C9155U/W-02 Decoding and Clock Tables
(14.318 MHz Input. All frequencies in MHz)

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17) Pin 10 = 1	CPU (Pin 18) Pin 10 = 1
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100	50

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	32	24	12

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

"U" Version:

PI6C9155U-01/02/03 are pin-to-pin compatible with Avasem
AV9155-01/02/03 (U version and non-U version).

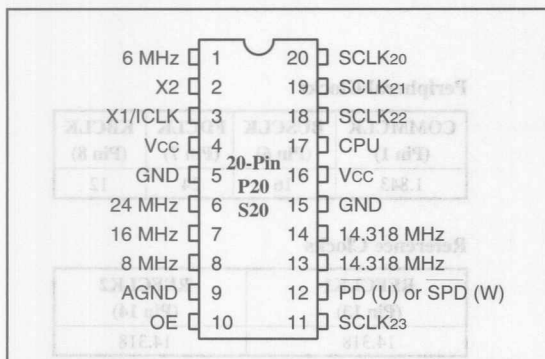
"W" Version:

PI6C9155W-01/02/03 are pin-to-pin compatible with Avasem
AV9155-01/02/03 with the exception of pin 12:

	Pin 12	Description of Power-Down
PI6C9155U	Hard Power-Down PD	Shuts off the entire chip when LOW.
PI6C9155W	Soft Power Down SPD	When LOW, CPU will have a smooth frequency transition to 8 MHz. 2XCPU will transit to 16 MHz.



Product Pin Configuration, PI6C9155U/W-03



CPU	SCLK23	SCLK22	SCLK21	SCLK20
(Pin 17)	(Pin 18)	(Pin 19)	(Pin 20)	(Pin 18)
0	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	0	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0
8	0	0	0	0
9	0	0	0	0
10	0	0	0	0
11	0	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	0	0	0	0
16	0	0	0	0
17	0	0	0	0
18	0	0	0	0
19	0	0	0	0
20	0	0	0	0

PI6C9155U/W-03 Product Pin Description

Pin Name	Pin Number	Pin Type	Description
6 MHz	1	Output	6 MHz Clock Output
X2	2	Output	Crystal connection. Leave as NC for clock input
X1/ICLK	3	Input	Crystal connection/Input Clock
Vcc	4	—	Digital power supply (+5V)
GND	5	—	Digital Ground
24 MHz	6	Output	24 MHz Floppy disk/Combination I/O Clock Output
16 MHz	7	Output	16 MHz Bus Clock
8 MHz	8	Output	8 MHz Keyboard Clock Output
AGND	9	—	Analog Ground (Original version)
OE	10	Input	OE = 1: Output Enable. OE = 0: Tri-states all outputs when low.
SCLK23	11	Input	CPU Clock frequency Select #3
PD	12	Input	Hard Power-Down. Shuts off entire chip when low (9155U-03)
SPD	12	Input	Soft Power-Down when LOW (9155W-03 version)
14.318 MHz	13	Output	14.318 MHz Reference Clock Output
14.318 MHz	14	Output	14.318 MHz Reference Clock Output
GND	15	—	Digital Ground
Vcc	16	—	Digital power supply (+5V)
CPU	17	Output	CPU Clock Output
SCLK22	18	Input	CPU Clock frequency Select #2
SCLK21	19	Input	CPU Clock frequency Select #1
SCLK20	20	Input	CPU Clock frequency Select #0



PI6C9155U/W-03 Decoding and Clock Tables (14.318 MHz Input. All frequencies in MHz)

CPU Clock

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17) Pin 10 = 1
0	0	0	0	16
0	0	0	1	40
0	0	1	0	50
0	0	1	1	80
0	1	0	0	66.66
0	1	0	1	100
0	1	1	0	8
0	1	1	1	4
1	0	0	0	8
1	0	0	1	20
1	0	1	0	25
1	0	1	1	40
1	1	0	0	33.3
1	1	0	1	50
1	1	1	0	4
1	1	1	1	2

To guarantee smooth, glitch-free frequency transitions, the state of SCLK23 (pin 11) must remain unchanged (smooth transitions are guaranteed in either the top or bottom half of the frequency decode table).

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
6	16	24	8

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



DC Electrical Characteristics at 5V (Operating Range, VCC = +5V ±10%, Temperature 0°C to +70°C)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -1 mA, VCC = 5V	VCC-0.4			V
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -4 mA, VCC = 5V	VCC-0.8			V
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -12 mA	2.4			V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL	IOL = 8 mA			0.4	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	VCC = 5V	2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level	VCC = 5V			0.8	V
IDD	Supply Current	No Load ⁽¹⁾			40		mA
Fd	Output Freq. Change ⁽²⁾	With Respect to Typical Frequency			0.002	0.01	%
ISC	Short Circuit Current	Each Output Clock			40		mA
RPU	Pull-up Resistor Value	Pins 10 and 12			200		kΩ
Ci	Input Capacitance	Except X1, X2				10	pF
CL	Load Capacitance	Pins X1, X2			20		pF

Notes:

1. PI6C9155 clocks running at the highest possible frequencies.
2. Over Supply and Temperature.

AC Electrical Characteristics at 5V (Operating Range, VCC = +5V ±10%, Temperature 0°C to 70°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
tCr	Input Clock Rise Time				20	ns
tCf	Input Clock Fall Time				20	ns
tr	Output Rise Time, 0.8 to 2.0V	25 pF Load for CPU and 2XCPU			2	ns
		25 pF Load for Peripherals			3	ns
tf	Output Fall Time, 2.0 to 0.8V	25 pF Load for CPU and 2XCPU			2	ns
		25 pF Load for Peripherals			3	ns
dt	Duty Cycle, CPU and 2XCPU	25 pF Load	40/60	48/52	60/40	%
dt	Duty Cycle, Other Clocks	25 pF Load	40/60	43/57	60/40	%
Tjis	Jitter, 1 Sigma	As Compared with Clock Period		0.8	2.5	%
Tjab	Jitter, Absolute			2	5	%
Tjab	Jitter, Absolute	16-100 MHz Clocks			700	ps
fi	Input Frequency			14.318		MHz
Tsk	Clock Skew between CPU & 2XCPU outputs	(1.0 ns max. for "U" version)		1	1.5	ns
tft	Frequency Transition Time	8 to 100 MHz			20	ms



ACTUAL OUTPUT FREQUENCIES
(14.318 MHz Input. All frequencies in MHz)

PI6C9155U/W-01 and PI6C9155U/W-02

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17) Pin 10 = 1	CPU (Pin 18) Pin 10 = 1
0	0	0	8.18	4.1
0	0	1	16.36	8.2
0	1	0	32.22	16.11
0	1	1	40.09	20.05
1	0	0	50.11	25.06
1	0	1	66.82	33.41
1	1	0	80.18	40.09
1	1	1	100.23	50.11

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	32.00 or 16.00	24.00	12.00

PI6C9155U/W-03

CPU Clock

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17) Pin 10 = 1
0	0	0	0	16.36
0	0	0	1	40.09
0	0	1	0	50.11
0	0	1	1	80.18
0	1	0	0	66.82
0	1	0	1	100.23
0	1	1	0	8.18
0	1	1	1	4.09
1	0	0	0	8.18
1	0	0	1	20.05
1	0	1	0	25.06
1	0	1	1	40.09
1	1	0	0	33.41
1	1	0	1	50.11
1	1	1	0	4.09
1	1	1	1	2.1

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
6.00	24.00	16.00	8.00

Supplement of PI6C9155 CPU Frequency Generator

PI6C9155 FREQUENCY ACCELERATION Feature

Pericom has been working closely with many customers to add advanced features while maintaining the compatibility with the standard frequency generators.

One of the advanced features is to provide the powerful frequency margin tests to all the production motherboards at no additional cost, to minimize production board burn-in time, and reduce manufacturing costs.

The Output Enable (OE) pin at pin 10 of PI6C9155U and PI6C9155W is modified as:

- OE = 1: Output Enable when logic high, compatible with Avasem AV9155 and AV9155U.
- OE = 0: Tri-states all outputs when logic low, compatible with Avasem AV9155 and AV9155U.
- OE = Floats: Enables CPU, 2XCPU Frequency Acceleration, Pericom's proprietary feature.

By floating the OE pin at pin 10, the CPU clock output frequency will be increased by approximately 2 MHz, if the CPU clock output is 25 MHz or greater. Assume the CPU frequency is selected at 33.33 MHz, for example, the CPU frequency will be increased to 35.33 MHz and 2XCPU will be increased to 70.66 MHz.

A motherboard design engineer also finds this feature a useful tool to thoroughly evaluate the margins of his/her design.

With the added frequency acceleration feature, the PI6C9155U-01/02/03 still maintain the pin-to-pin compatibility with Avasem AV9155-01/02/03 and AV9155U-01/02/03 devices.

The clock frequencies and actual output frequencies are described in the following tables.

COMMON CLK (Pin 1)	BUSCLK (Pin 6)	PDCLK (Pin 7)	KBCLK (Pin 8)
6.00	24.00	18.00	3.00

CPU (Pin 17)	2XCPU (Pin 20)	SC1620 (Pin 19)	SC1622 (Pin 18)	SC1623 (Pin 11)
16.38	0	0	0	0
40.00	1	0	0	0
50.11	0	1	0	0
80.18	1	1	0	0
88.37	0	0	1	0
100.23	1	0	1	0
8.18	0	1	1	0
4.00	1	1	1	0
8.18	0	0	0	1
20.00	1	0	0	1
22.00	0	1	0	1
40.00	1	1	0	1
33.33	0	0	1	1
50.11	1	0	1	1
40.00	0	1	1	1
3.1	1	1	1	1

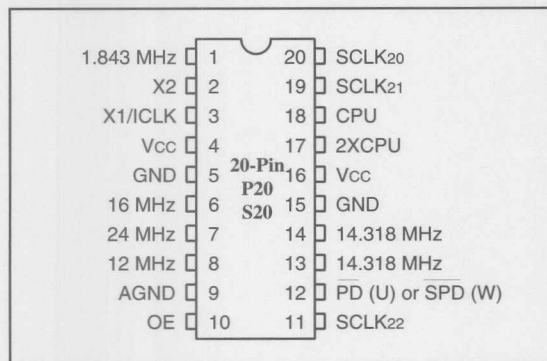


PI6C9155U-01
PI6C9155U-02
PI6C9155U-03
PI6C9155W-01
PI6C9155W-02
PI6C9155W-03

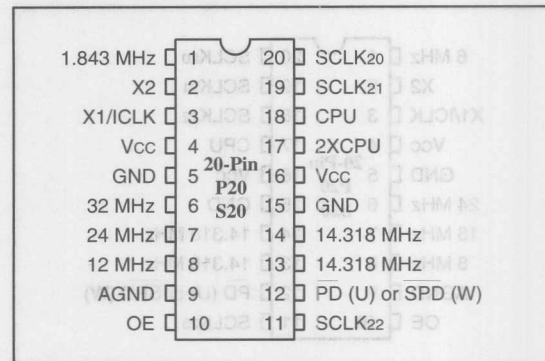
FREQUENCY ACCELERATION FEATURE OF PI6C9155

PI6C9155 SUPPLEMENT

Product Pin Configuration, PI6C9155U/W-01



Product Pin Configuration, PI6C9155U/W-02



PI6C9155U/W-01 Decoding and Clock Tables (14.318 MHz Input. All frequencies in MHz)

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)		CPU (Pin 18)	
			Pin 10 = 1	Pin 10 = Floats	Pin 10 = 1	Pin 10 = Floats
0	0	0	8	8	4	4
0	0	1	16	16	8	8
0	1	0	32	32	16	16
0	1	1	40	40	20	20
1	0	0	50	54	25	27
1	0	1	66.66	70.66	33.33	35.33
1	1	0	80	84	40	42
1	1	1	100	104	50	52

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

PI6C9155U/W-02 Decoding and Clock Tables (14.318 MHz Input. All frequencies in MHz)

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)		CPU (Pin 18)	
			Pin 10 = 1	Pin 10 = Floats	Pin 10 = 1	Pin 10 = Floats
0	0	0	8	8	4	4
0	0	1	16	16	8	8
0	1	0	32	32	16	16
0	1	1	40	40	20	20
1	0	0	50	54	25	27
1	0	1	66.66	70.66	33.33	35.33
1	1	0	80	84	40	42
1	1	1	100	104	50	52

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	32	24	12

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

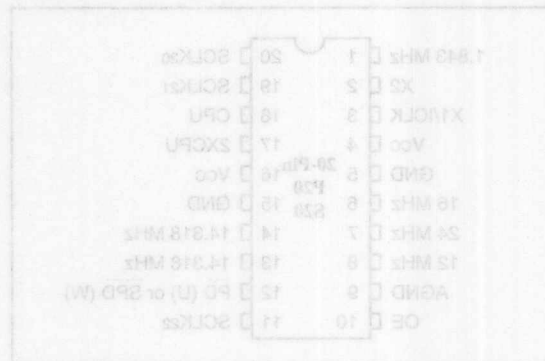
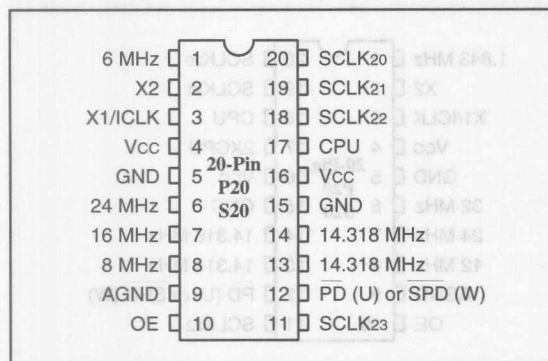


PI6C9155U-01 PI6C9155W-01
PI6C9155U-02 PI6C9155W-02
PI6C9155U-03 PI6C9155W-03

FREQUENCY ACCELERATION FEATURE OF PI6C9155

PI6C9155 SUPPLEMENT

Product Pin Configuration, PI6C9155U/W-03



PI6C9155U/W-03 Decoding and Clock Tables (14.318 MHz Input. All frequencies in MHz)

CPU Clock

CPU (Pin 17)				Pin 10 = 1 Pin 10 = Floats	
SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	Pin 10 = 1	Pin 10 = Floats
0	0	0	0	16	16
0	0	0	1	40	40
0	0	1	0	50	54
0	0	1	1	80	84
0	1	0	0	66.66	70.66
0	1	0	1	100	104
0	1	1	0	8	8
0	1	1	1	4	4
1	0	0	0	8	8
1	0	0	1	20	20
1	0	1	0	25	27
1	0	1	1	40	42
1	1	0	0	33.3	35.33
1	1	0	1	50	52
1	1	1	0	4	4
1	1	1	1	2	2

To guarantee smooth, glitch-free frequency transitions, the state of SCLK23 (pin 11) must remain unchanged (smooth transitions are guaranteed in either the top or bottom half of the frequency decode table).

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
6	16	24	8

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318



PI6C9155U-01 PI6C9155W-01
 PI6C9155U-02 PI6C9155W-02
 PI6C9155U-03 PI6C9155W-03

FREQUENCY ACCELERATION FEATURE OF PI6C9155

PI6C9155 SUPPLEMENT

ACTUAL OUTPUT FREQUENCIES

(14.318 MHz Input. All frequencies in MHz)

PI6C9155U/W-01 and PI6C9155U/W-02

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)		CPU (Pin 18)	
			Pin 10 = 1	Pin 10 = Floats	Pin 10 = 1	Pin 10 = Floats
0	0	0	8.18	8.18	4.1	4.1
0	0	1	16.36	16.36	8.2	8.2
0	1	0	32.22	32.22	16.11	16.11
0	1	1	40.09	40.09	20.05	20.05
1	0	0	50.11	53.7	25.06	26.9
1	0	1	66.82	69.8	33.41	34.9
1	1	0	80.18	83.9	40.09	41.9
1	1	1	100.23	103.8	50.11	51.9

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	32.00 or 16.00	24.00	12.00

PI6C9155U/W-03

CPU Clock

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17)	
				Pin 10 = 1	Pin 10 = Floats
0	0	0	0	16.36	16.36
0	0	0	1	40.09	40.09
0	0	1	0	50.11	53.7
0	0	1	1	80.18	83.9
0	1	0	0	66.82	69.8
0	1	0	1	100.23	103.8
0	1	1	0	8.18	8.18
0	1	1	1	4.09	4.09
1	0	0	0	8.18	8.18
1	0	0	1	20.05	20.05
1	0	1	0	25.06	26.9
1	0	1	1	40.09	41.9
1	1	0	0	33.41	34.9
1	1	0	1	50.11	51.9
1	1	1	0	4.09	4.09
1	1	1	1	2.1	2.1

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
6.00	24.00	16.00	8.00

10

3.3V CPU Frequency Generator

Features

- 3.3V version of PI6C9155U-01/02/03
- Generates most essential clock signals for CPU boards
- Generates five simultaneous clock signals for most peripheral controllers
- Replaces six crystal oscillators, for cost savings and board space savings
- On-chip loop filters — no external loop filter circuit
- Smooth jitter-free transition between two CPU frequencies for power savings
- Single low cost (14.318 MHz) crystal as reference input frequency
- Low power 0.8 micron CMOS technology
- ESD protection exceeds 2000V
- Packages available:
 - 20-pin 300 mil wide plastic DIP (P20)
 - 20-pin 300 mil wide plastic SOIC (S20)

Clock Table (MHz)

Clock	PI6C9156U-01	PI6C9156U-02
KBCLK	12	12
BUSCLK	16	32
FDCLK	24	24
COMMCLK	1.84	1.84
14.318 (2)	14.318	14.318
CPUCLK	4, 8, 16, 20, 25, 33.3, 40, or 50	
2XCPUCLK	8, 16, 32, 40, 50, or 66.6	

General Description

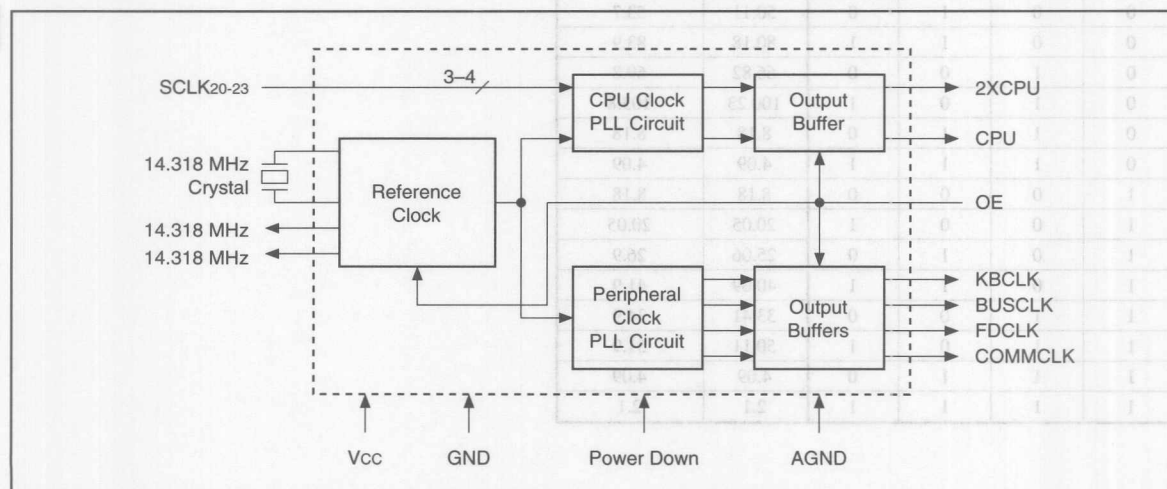
The PI6C9156 clock generator provides a low cost solution for generating most of the necessary clock frequencies for motherboards with 3V power supply, for tremendous cost and board savings.

The two main clock outputs CPU and 2XCPU can be set by the user to one of several popular processor clock frequencies. It also offers four simultaneous clocks for popular peripherals, plus two reference clock outputs which are identical to the reference input crystal frequency.

The device has other advanced features which include on-chip filter circuits, for simplifying the board design, and hard power-down capacity for power savings. Enhanced versions with customized frequencies and features are also available. Contact the factory for the enhanced versions.

The CPU and 2XCPU clocks offer an additional feature of reducing the operating clock speeds for saving power of the entire computer while the computer is at idle. This feature cannot be accomplished by metal-can oscillators. A smooth, jitter-free frequency transition is provided for the CPU and 2XCPU clocks during the transition of slow down and speed up. The frequency transition rates meet the specifications of all x86 microprocessors to within 0.1% frequency change per clock period.

Block Diagram

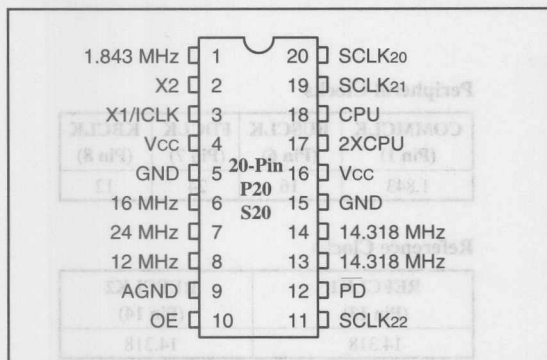


Pericom Semiconductor Corporation

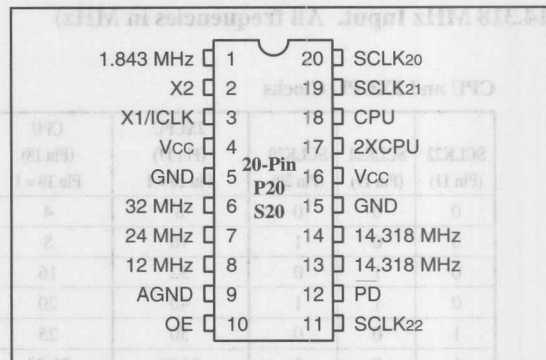
2380 Bering Drive • San Jose, CA 95131 • Tel: 408 435-0800 • Fax: 408 321-0933



Product Pin Configuration, PI6C9156U-01



Product Pin Configuration, PI6C9156U-02



PI6C9156U-01, PI6C9156U-02 Product Pin Description

Pin Name	Pin Number	Pin Type	Description
1.843 MHz	1	Output	1.84 MHz Clock Output
X2	2	Output	Crystal connection. Leave as NC for clock input
X1/ICLK	3	Input	Crystal connection/Input Clock
Vcc	4	—	Digital power supply (+3.3V)
GND	5	—	Digital Ground
16 MHz/32 MHz	6	Output	16 MHz (PI6C9156U-01) or 32 MHz (PI6C9156U-02) Clock Output
24 MHz	7	Output	24 MHz Floppy disk/Combination I/O Clock Output
12 MHz	8	Output	12 MHz Keyboard Clock Output
AGND	9	—	Analog Ground (Original version)
OE	10	Input	Output Enable. Tri-states all outputs when low.
SCLK22	11	Input	CPU Clock frequency Select #2
PD	12	Input	Hard Power-Down. Shuts off entire chip when low
14.318 MHz	13	Output	14.318 MHz Reference Clock Output
14.318 MHz	14	Output	14.318 MHz Reference Clock Output
GND	15	—	Digital Ground
Vcc	16	—	Digital power supply (+3.3V)
2XCPU	17	Output	2X CPU Clock Output
CPU	18	Output	1X CPU Clock Output
SCLK21	19	Input	CPU Clock frequency Select #1
SCLK20	20	Input	CPU Clock frequency Select #0



PI6C9156U-01
PI6C9156U-02
PI6C9156U-03
3.3V CPU FREQUENCY GENERATOR

PI6C9156U-01 Decoding and Clock Tables
(14.318 MHz Input. All frequencies in MHz)

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17) Pin 10 = 1	CPU (Pin 18) Pin 10 = 1
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

PI6C9156U-02 Decoding and Clock Tables
(14.318 MHz Input. All frequencies in MHz)

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17) Pin 10 = 1	CPU (Pin 18) Pin 10 = 1
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33

Peripheral Clocks

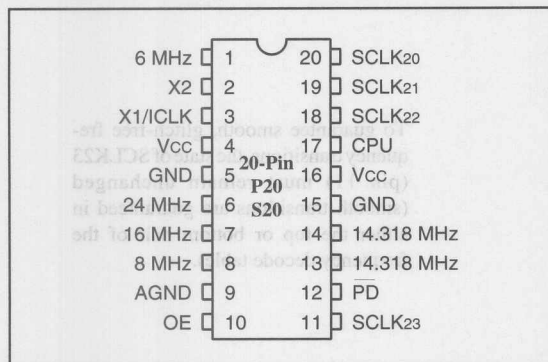
COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	32	24	12

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318



Product Pin Configuration, PI6C9156U-03



PI6C9156U-03 Product Pin Description

Pin Name	Pin Number	Pin Type	Description
6 MHz	1	Output	6 MHz Clock Output
X2	2	Output	Crystal connection. Leave as NC for clock input
X1/CLK	3	Input	Crystal connection/Input Clock
Vcc	4	—	Digital power supply (+3.3V)
GND	5	—	Digital Ground
24 MHz	6	Output	24 MHz Floppy disk/Combination I/O Clock Output
16 MHz	7	Output	16 MHz Bus Clock
8 MHz	8	Output	8 MHz Keyboard Clock Output
AGND	9	—	Analog Ground (Original version)
OE	10	Input	Output Enable. Tri-states all outputs when low.
SCLK23	11	Input	CPU Clock frequency Select #3
PD	12	Input	Hard Power-Down. Shuts off entire chip when low (9156U-03)
14.318 MHz	13	Output	14.318 MHz Reference Clock Output
14.318 MHz	14	Output	14.318 MHz Reference Clock Output
GND	15	—	Digital Ground
Vcc	16	—	Digital power supply (+3.3V)
CPU	17	Output	CPU Clock Output
SCLK22	18	Input	CPU Clock frequency Select #2
SCLK21	19	Input	CPU Clock frequency Select #1
SCLK20	20	Input	CPU Clock frequency Select #0

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CPU Clock

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17) Pin 10 = 1
0	0	0	0	16
0	0	0	1	40
0	0	1	0	50
0	1	0	0	66.66
0	1	1	0	8
0	1	1	1	4
1	0	0	0	8
1	0	0	1	20
1	0	1	0	25
1	1	0	0	33.3
1	1	1	0	4
1	1	1	1	2

To guarantee smooth, glitch-free frequency transitions, the state of SCLK23 (pin 11) must remain unchanged (smooth transitions are guaranteed in either the top or bottom half of the frequency decode table).

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
6	16	24	8

Reference Clocks

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics at 3V (Operating Range, VCC = +3.0V to 3.6V, Temperature 0°C to +70°C)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
V _{OH}	Output HIGH Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -4 mA	2.4			V
V _{OL}	Output LOW Voltage	VCC = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 8 mA			0.4	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{DD}	Supply Current	No Load, Runing at Highest Possible Frequencies			40		mA
F _d	Output Freq. Change ⁽¹⁾	With Respect to Typical Frequency			0.002	0.01	%
I _{SC}	Short Circuit Current	Each Output Clock		25	40		mA
R _{PU}	Pull-up Resistor Value	Pins 10 and 12			680		kΩ
C _i	Input Capacitance	Except X1, X2				10	pF
C _L	Load Capacitance	Pins X1, X2			20		pF

Notes:

1. Over Supply and Temperature.

AC Electrical Characteristics at 3V (Operating Range, VCC = +3.0V to 3.6V, Temperature 0°C to +70°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t _{icr}	Input Clock Rise Time				20	ns
t _{icf}	Input Clock Fall Time				20	ns
t _r	Output Rise Time, 0.8 to 2.0V	25 pF Load for CPU and 2XCPU			2	ns
		25 pF Load for Peripherals			3	ns
t _f	Output Fall Time, 2.0 to 0.8V	25 pF Load for CPU and 2XCPU			2	ns
		25 pF Load for Peripherals			3	ns
d _t	Duty Cycle, CPU and 2XCPU	25 pF Load	40/60		60/40	%
		25 pF Load	40/60		60/40	%
T _{jis}	Jitter, 1 Sigma	As Compared with Clock Period		0.8	2.5	%
T _{jab}	Jitter, Absolute	As Compared with Clock Period		2	5	%
f _i	Input Frequency			14.318		MHz
T _{sk}	Clock Skew between CPU & 2XCPU outputs			1	1.5	ns
t _{ft}	Frequency Transition Time				20	ms



ACTUAL OUTPUT FREQUENCIES
(14.318 MHz Input. All frequencies in MHz)

PI6C9156U-01 and PI6C9156U-02

CPU and 2XCPU Clocks

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17) Pin 10 = 1	CPU (Pin 18) Pin 10 = 1
0	0	0	8.18	4.1
0	0	1	16.36	8.2
0	1	0	32.22	16.11
0	1	1	40.09	20.05
1	0	0	50.11	25.06
1	0	1	66.82	33.41

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	32.00 or 16.00	24.00	12.00

PI6C9156U-03

CPU Clock

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17) Pin 10 = 1
0	0	0	0	16.36
0	0	0	1	40.09
0	0	1	0	50.11
0	1	0	0	66.82
0	1	1	0	8.18
0	1	1	1	4.09
1	0	0	0	8.18
1	0	0	1	20.05
1	0	1	0	25.06
1	1	0	0	33.41
1	1	1	0	4.09
1	1	1	1	2.1

Peripheral Clocks

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
6.00	24.00	16.00	8.00

Pericom Semiconductor Corporation

2380 Bering Drive • San Jose, CA 95131 • Tel: 408 435-0800 • Fax: 408 321-0933



PI6C462

Motherboard Clock Generator

Product Features:

- Pin-to-Pin compatible with IMISC462 clock generator
- Generates all essential clock signals for Intel microprocessor based motherboard design, including 486-SL Enhanced deep green PC design
- Integrates CPU clock, Keyboard clock, Reference clock
- Integrates a clock buffer to generate four low-skew clock outputs from a single clock input, for motherboard cost reduction
- Power down mode for low power consumption, with selectable DOZE mode, and RESUME# output for SL-Enhanced type processor compatibility
- Smooth and glitch-free frequency transition from one CPU clock to another CPU clock—meeting Intel microprocessor spec
- 50% duty cycle
- Uses a low cost 14.318 MHz crystal as reference frequency
- Very low short and long term jitter
- Packages available:
 - 28-pin 300 mil wide plastic PDIP (P28)
 - 28-pin 209 mil wide plastic SSOP (H28)

Product Description:

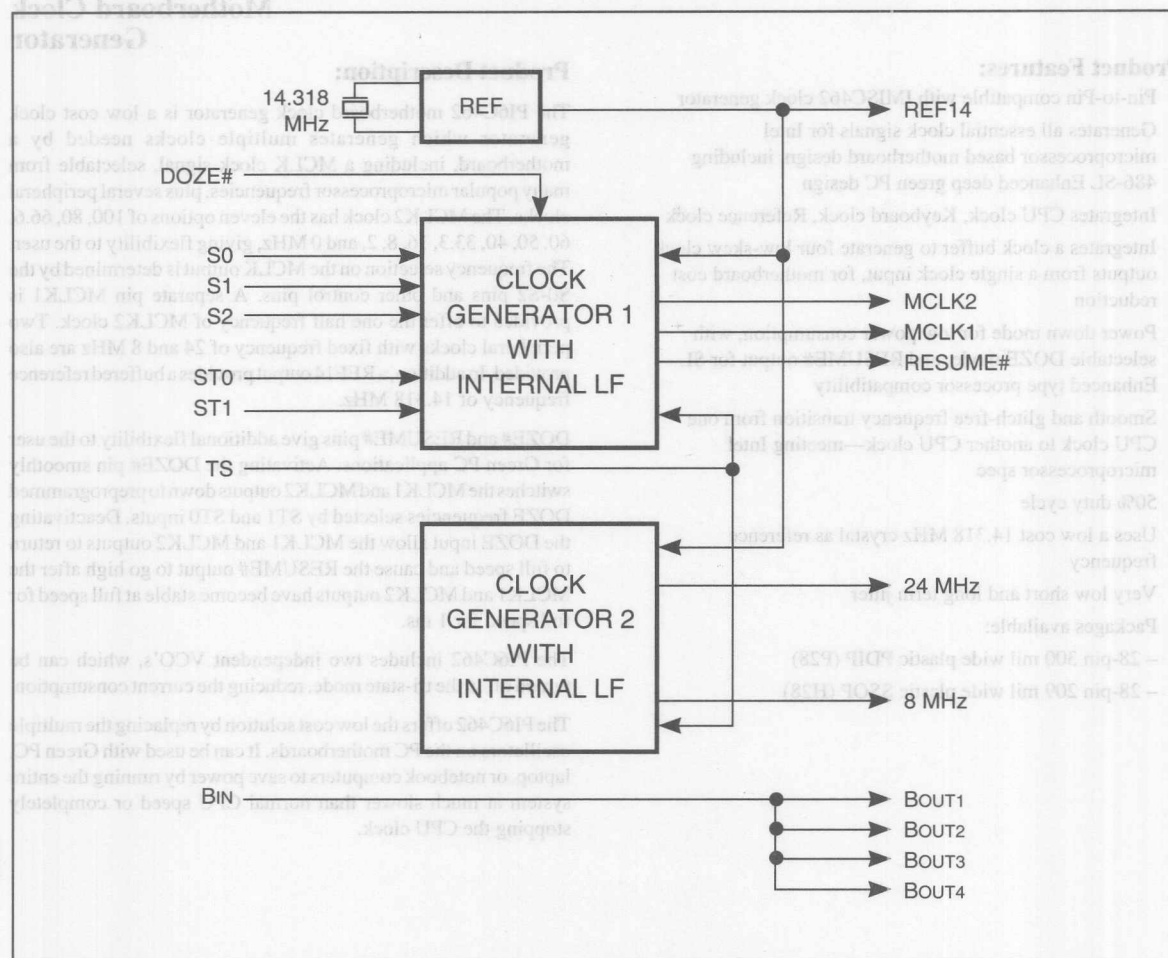
The PI6C462 motherboard clock generator is a low cost clock generator which generates multiple clocks needed by a motherboard, including a MCLK clock signal, selectable from many popular microprocessor frequencies, plus several peripheral clocks. The MCLK2 clock has the eleven options of 100, 80, 66.6, 60, 50, 40, 33.3, 16, 8, 2, and 0 MHz, giving flexibility to the user. The frequency selection on the MCLK output is determined by the S0-S2 pins and other control pins. A separate pin MCLK1 is provided to offer the one half frequency of MCLK2 clock. Two peripheral clocks with fixed frequency of 24 and 8 MHz are also provided. In addition, a REF14 output provides a buffered reference frequency of 14.318 MHz.

DOZE# and RESUME# pins give additional flexibility to the user for Green PC applications. Activating the DOZE# pin smoothly switches the MCLK1 and MCLK2 outputs down to preprogrammed DOZE frequencies selected by ST1 and ST0 inputs. Deactivating the DOZE input allow the MCLK1 and MCLK2 outputs to return to full speed and cause the RESUME# output to go high after the MCLK1 and MCLK2 outputs have become stable at full speed for full speed for 1 ms.

The PI6C462 includes two independent VCO's, which can be turned off in the tri-state mode, reducing the current consumption.

The PI6C462 offers the low cost solution by replacing the multiple oscillators on the PC motherboards. It can be used with Green PC, laptop, or notebook computers to save power by running the entire system at much slower than normal CPU speed or completely stopping the CPU clock.

PI6C462 Block Diagram



Product Pin Configuration

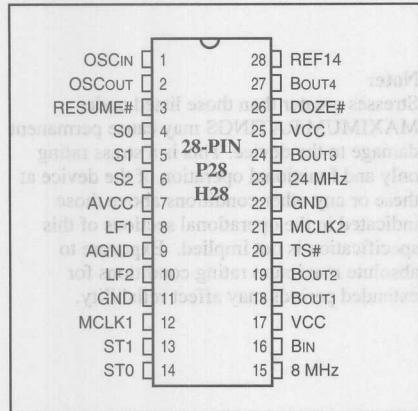


Table 1. Frequency Selection

Inputs						MCLK Outputs (MHz)	
DOZE#	S2	S1	S0	ST1	ST0	MCLK2	MCLK1
0	X	X	X	0	0	0	0
0	X	X	X	0	1	2	1
0	X	X	X	1	0	8	4
0	X	X	X	1	1	16	8
1	0	0	0	X	X	100	50
1	0	0	1	X	X	80	40
1	0	1	0	X	X	66.6	33.3
1	0	1	1	X	X	60	30
1	1	0	0	X	X	50	25
1	1	0	1	X	X	40	20
1	1	1	0	X	X	33.3	16.7
1	1	1	1	X	X	TEST	TEST

Product Pin Description

Pin Name	Description
OSCIN, OSCOUT	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCIN may also serve as input for an externally generated reference signal.
S0, S1, S2	Standard frequency select inputs. These inputs control the high-speed MCLK frequency selection. S2-S0 inputs control the CPU clock frequencies. All these inputs have internal pull-ups. Table 1 shows the output frequency selection conditions.
MCLK1, MCLK2	Master clock outputs. Programmable output frequencies can be selected using S2-S0 inputs shown in Table 1.
DOZE#	DOZE control pin. When DOZE# is HIGH, the clock chip operates in the standard mode. When this pin goes LOW, output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occur smoothly to allow tracking by 486 CPU internal PLL. This pin has an internal pull-up.
BIN	On-chip buffer input. This pins has an internal pull-up.
BOUT1-BOUT4	Buffer output pins of BIN. These buffers are capable of sink or source 12 mA. They can be used to buffer critical clock lines for PCI or VESA applications.
24 MHz	24 MHz floppy drive clock output.
8 MHz	8 MHz clock output.
REF14	14.318 MHz output. Buffered outputs for the on-chip reference oscillator or externally provided reference.
LF1, LF2	Connect to an external capacitor.
ST0, ST1	DOZE frequency selection shown in Table 1. Both inputs have internal pull-ups.
TS#	Tri-state control pin. When TS# is LOW, all outputs except BOUT pins are tri-stated and VCO's are turned off. This pin has an internal pull-up.
GND	Circuit ground.
AGND	Analog circuit ground.
Vcc	Positive power supply.
AVcc	Analog positive power supply.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Vcc = 5V ±10%, TA = 0°C to +70°C)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	S2-S0 Inputs, B _{IN}	2.0	—	—	V
V _{IL}	Input LOW Voltage	S2-S0 Inputs, B _{IN}	—	—	0.8	V
I _{IH}	Input HIGH Current with Pull-up or Pull-down	S2-S0 Inputs, B _{IN}	—	—	5 ±50	µA
I _{IL}	Input LOW Current with Pull-up or Pull-down	S2-S0 Inputs, B _{IN}	—	—	5 ±50	µA
V _{OH}	Output HIGH Voltage	All Outputs, I _{OH} = -12 mA, including B _{OUT1} , B _{OUT2} , B _{OUT3} , B _{OUT4}	2.4	—	—	V
V _{OL}	Output LOW Voltage	All Outputs, I _{OL} = 12 mA, including B _{OUT1} , B _{OUT2} , B _{OUT3} , B _{OUT4}	—	—	0.4	V
I _{OS}	Short Circuit Current	Vcc = 5.25V ⁽³⁾ , V _{OUT} = GND	25	—	—	mA
I _{CC}	Static Supply Current	Vcc = 5.0V, OSC _{IN} = 0, TS# = 0	—	—	10	µA
I _C	Dynamic Supply Current	Vcc = 5.0V, MCLK = 50 MHz	—	—	35	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate values specified under Electrical Characteristics for the appropriate device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of test should not exceed one second.

Switching Characteristics (GND = 5V \pm 10%, T_A = 0°C to +70°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t _{PLH} t _{PHL}	Output Rise (0.8V to 2.0V) Fall Time (2.0V to 0.8V) MCLK and REF14 Outputs	30 pF Load	—	—	2	ns
dt	Duty Cycle MCLK and REF14		—	50/50	45/55	%
t _{PLH} t _{PHL}	Propagation Delay BIN to BOUT	15 pF Load, Measured at 1.4V	2.0	—	6.5	ns
t _{SKW}	Buffer Out Skew BOUT1-BOUT4	15 pF Load, Measured at 1.4V	—	—	0.75	ns
T _{JIS}	Jitter One Sigma MCLK and REF14	As Compared with Clock Period	—	—	\pm 2	%
T _{JAB}	Jitter Absolute MCLK and REF14	As Compared with Clock Period	—	—	\pm 5	%



PRELIMINARY

PI6C464

Motherboard Clock Generator

Product Features:

- Pin-to-Pin compatible with IMISC464 clock generator
- Generates all essential clock signals for Intel microprocessor based motherboard design, including 486-SL Enhanced deep green PC design
- Integrates CPU clock, Keyboard clock, Reference clock
- Integrates a clock buffer to generate four low-skew clock outputs from a single clock input, for motherboard cost reduction
- Power down mode for low power consumption, with selectable DOZE mode for SL-Enhanced type processor compatibility
- Smooth and glitch-free frequency transition from one CPU clock to another CPU clock—meeting Intel microprocessor spec
- 50% duty cycle
- Uses a low cost 14.318 MHz crystal as reference frequency
- Very low short and long term jitter
- Packages available:
 - 28-pin 300 mil wide plastic PDIP (P28)
 - 28-pin 209 mil wide plastic SSOP (H28)

Product Description:

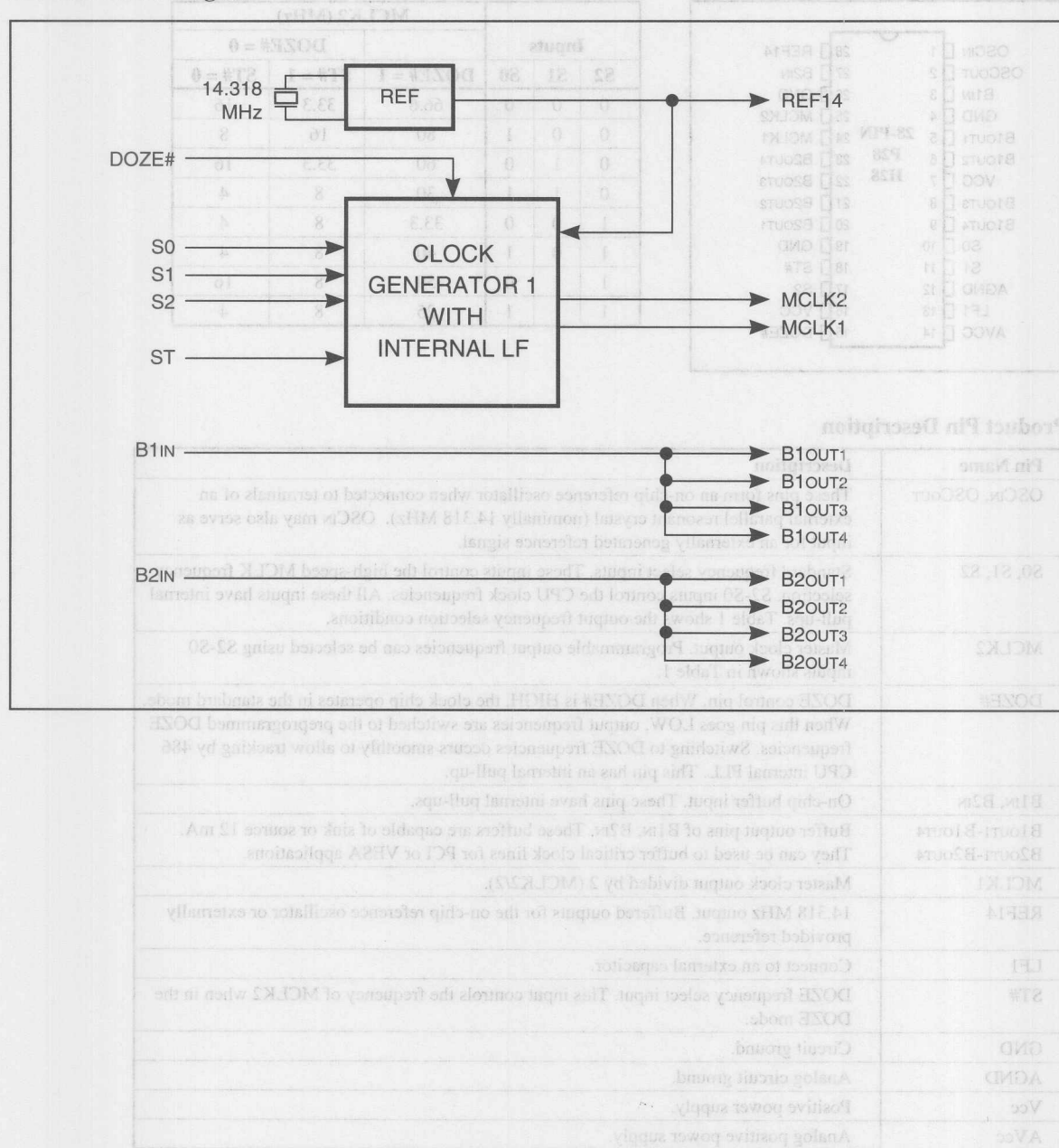
The PI6C464 motherboard clock generator is a low cost clock generator which generates multiple clocks needed by a motherboard, including a MCLK clock signal, selectable from many popular microprocessor frequencies, plus several peripheral clocks. The MCLK2 clock has the eleven options of 80, 66.6, 60, 50, 40, 33.3, 30, and 25 MHz, giving flexibility to the user. The frequency selection on the MCLK output is determined by the S0-S2 pins and other control pins. A separate pin MCLK1 is provided to offer the one half frequency of MCLK2 clock. In addition, a REF14 output provides a buffered reference frequency of 14.318 MHz.

DOZE# pin gives additional flexibility to the user for Green PC applications. Activating the DOZE# pin smoothly switches the MCLK1 and MCLK2 outputs down to preprogrammed DOZE frequencies selected by ST1 and ST0 inputs. Deactivating the DOZE# input allows the MCLK1 and MCLK2 outputs to return to full speed.

The PI6C464 includes two independent VCO's, which can be turned off in the tri-state mode, reducing the current consumption.

The PI6C464 offers the low cost solution by replacing the multiple oscillators on the PC motherboards. It can be used with Green PC, laptop, or notebook computers to save power by running the entire system at much slower than normal CPU speed or completely stopping the CPU clock.

PI6C464 Block Diagram



Product Pin Configuration

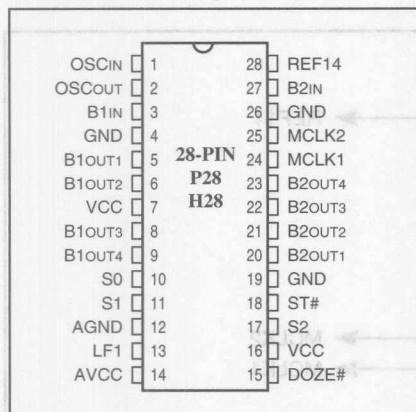


Table 1. Frequency Selection

Inputs			MCLK2 (MHz)		
			DOZE# = 0		
S2	S1	S0	DOZE# = 1	ST# = 1	ST# = 0
0	0	0	66.6	33.3	16
0	0	1	80	16	8
0	1	0	60	33.3	16
0	1	1	30	8	4
1	0	0	33.3	8	4
1	0	1	40	8	4
1	1	0	50	8	16
1	1	1	25	8	4

Product Pin Description

Pin Name	Description
OSCIN, OSCOUT	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCIN may also serve as input for an externally generated reference signal.
S0, S1, S2	Standard frequency select inputs. These inputs control the high-speed MCLK frequency selection. S2-S0 inputs control the CPU clock frequencies. All these inputs have internal pull-ups. Table 1 shows the output frequency selection conditions.
MCLK2	Master clock output. Programmable output frequencies can be selected using S2-S0 inputs shown in Table 1.
DOZE#	DOZE control pin. When DOZE# is HIGH, the clock chip operates in the standard mode. When this pin goes LOW, output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occurs smoothly to allow tracking by 486 CPU internal PLL. This pin has an internal pull-up.
B1IN, B2IN	On-chip buffer input. These pins have internal pull-ups.
B1OUT1-B1OUT4 B2OUT1-B2OUT4	Buffer output pins of B1IN, B2IN. These buffers are capable of sink or source 12 mA. They can be used to buffer critical clock lines for PCI or VESA applications.
MCLK1	Master clock output divided by 2 (MCLK2/2).
REF14	14.318 MHz output. Buffered outputs for the on-chip reference oscillator or externally provided reference.
LF1	Connect to an external capacitor.
ST#	DOZE frequency select input. This input controls the frequency of MCLK2 when in the DOZE mode.
GND	Circuit ground.
AGND	Analog circuit ground.
Vcc	Positive power supply.
AVcc	Analog positive power supply.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Vcc = 5V ±10%, TA = 0°C to +70°C)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	S2-S0 Inputs, B1 _{IN} , B2 _{IN} Inputs	2.0	—	—	V
V _{IL}	Input LOW Voltage	S2-S0 Inputs, B1 _{IN} , B2 _{IN} Inputs	—	—	0.8	V
I _{IH}	Input HIGH Current with Pull-up or Pull-down	S2-S0 Inputs, B1 _{IN} , B2 _{IN} Inputs	—	—	5 ±50	μA
I _{IL}	Input LOW Current with Pull-up or Pull-down	S2-S0 Inputs, B1 _{IN} , B2 _{IN} Inputs	—	—	5 ±50	μA
V _{OH}	Output HIGH Voltage	All Outputs, I _{OH} = -12 mA, including B1 _{OUTX} , B2 _{OUTX}	2.4	—	—	V
V _{OL}	Output LOW Voltage	All Outputs, I _{OL} = 12 mA, including B1 _{OUTX} , B2 _{OUTX}	—	—	0.4	V
I _{OS}	Short Circuit Current	Vcc = 5.25V ⁽³⁾ , V _{OUT} = GND	25	—	—	mA
I _{CC}	Static Supply Current	Vcc = 5.0V, OSC _{IN} = 0, TS# = 0	—	—	10	μA
I _C	Dynamic Supply Current	Vcc = 5.0V, MCLK = 50 MHz	—	—	35	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate values specified under Electrical Characteristics for the appropriate device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of test should not exceed one second.

Switching Characteristics (GND = 5V ±10%, TA = 0°C to +70°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
tPLH tPHL	Output Rise (0.8V to 2.0V) Fall Time (2.0V to 0.8V) MCLK and REF14 Outputs	30 pF Load	—	—	2	ns
dt	Duty Cycle MCLK and REF14		—	50/50	45/55	%
tPLH tPHL	Propagation Delay Bin to Bout	15 pF Load, Measured at 1.4V	2.0	—	6.5	ns
tsKEW	Buffer Out Skew B1OUT1-B1OUT4	15 pF Load, Measured at 1.4V	—	—	0.75	ns
TJIS	Jitter One Sigma MCLK and REF14	As Compared with Clock Period	—	—	±2	%
TJAB	Jitter Absolute MCLK and REF14	As Compared with Clock Period	—	—	±5	%

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
Vin	Input HIGH Voltage	2.0 to 2.5 V, B1, B2, B3, B4	2.0	—	—	V
VIL	Input LOW Voltage	2.0 to 2.5 V, B1, B2, B3, B4	—	—	0.8	V
Iin	Input HIGH Current with Pull-up or Pull-down	2.0 to 2.5 V, B1, B2, B3, B4	—	—	2	µA
Iin	Input LOW Current with Pull-up or Pull-down	2.0 to 2.5 V, B1, B2, B3, B4	—	—	2	µA
Vout	Output HIGH Voltage	All Outputs, IOL = 12 mA, including B1OUT, B2OUT, B3OUT, B4OUT	2.4	—	—	V
VOL	Output LOW Voltage	All Outputs, IOH = 12 mA, including B1OUT, B2OUT, B3OUT, B4OUT	—	—	0.4	V
Ios	Short Circuit Current	VCC = 2.5 V, VOUT = GND	25	—	—	mA
Icc	Static Supply Current	VCC = 2.0 V, OSCIN = 0, IOL = 0	—	—	10	µA
ic	Dynamic Supply Current	VCC = 2.0 V, MCLK = 50 MHz	—	—	35	mA

NOTES:
1. For conditions shown as Min. or Max., use appropriate values specified under Electrical Characteristics for the appropriate device type.
2. Typical values are at VCC = 2.0 V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of test should not exceed one second.

Motherboard Clock Generator
Product Features:

- Pin-to-Pin compatible with IMISC468 clock generator
- Generates all essential clock signals for Intel microprocessor based motherboard design, including 486-SL Enhanced deep green PC design
- Integrates CPU clock, 24 and 8 MHz peripheral clocks, and Reference clock
- Integrates two clock buffers to generate two banks of one clock input and four low-skew clock outputs, for cost reduction in PCI, VESA, and ISA bus-based motherboards.
- Power down mode for low power consumption
- Smooth and glitch-free frequency transition from one CPU clock to another CPU clock—meeting Intel microprocessor spec
- 50% duty cycle.
- Uses a low cost 14.318 MHz crystal as reference frequency
- Very low short and long term jitter
- Packages available:
 - 28-pin 300 mil wide plastic PDIP (P28)
 - 28 pin 209 mil wide plastic SSOP (H28)

Product Description:

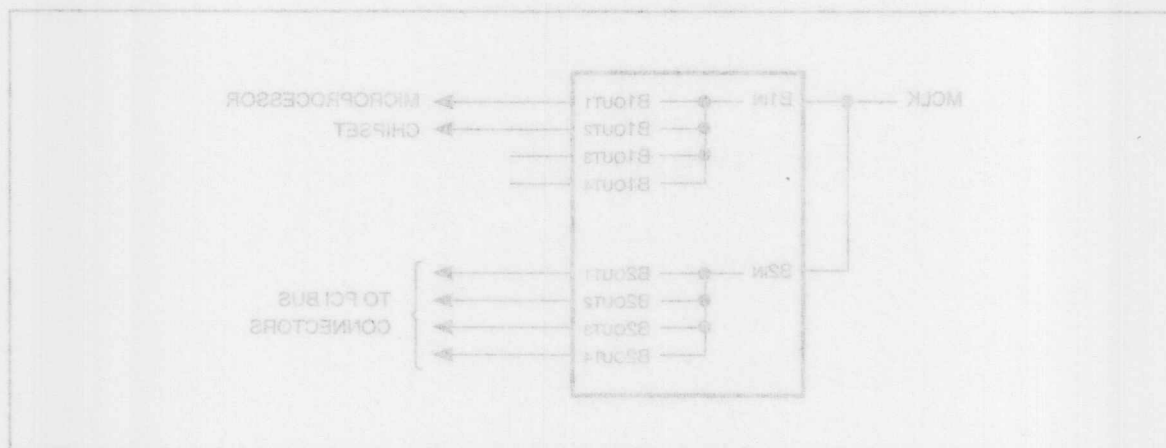
The PI6C468 motherboard clock generator is a low cost clock generator which generates multiple clocks needed by a motherboard, including a MCLK clock signal, selectable from many popular microprocessor frequencies, plus several peripheral clocks. The MCLK clock has the eleven options of 80, 66.6, 60, 50, 40, 33.3, 30, and 25 MHz, giving flexibility to the user. The frequency selection on the MCLK output is determined by the S0-S2 pins and other control pins. Two peripheral clocks with fixed frequency of 24 and 8 MHz are also provided. In addition, a REF14 output provides a buffered reference frequency of 14.318 MHz.

DOZE# pin gives additional flexibility to the user for Green PC applications. Activating the DOZE# pin smoothly switches the MCLK output down to preprogrammed DOZE frequency. Deactivating the DOZE input allow the MCLK output to return to full speed. The PI6C462 includes two independent VCO's.

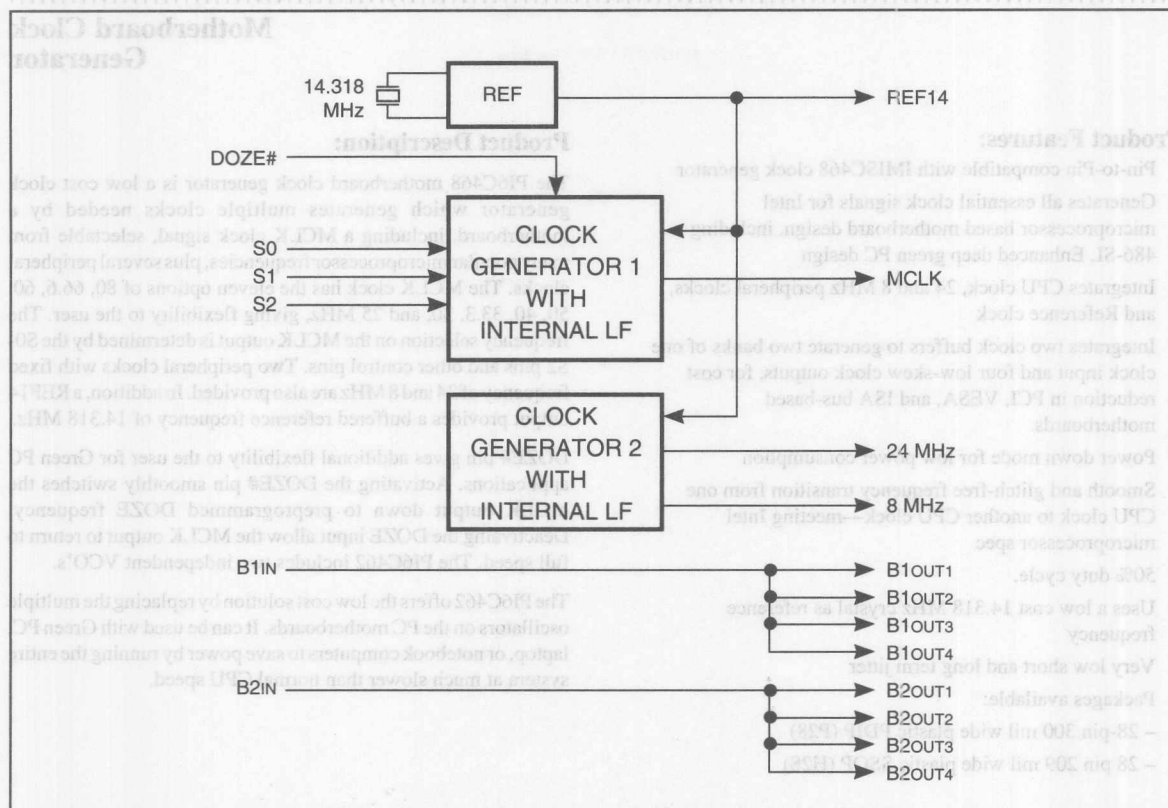
The PI6C462 offers the low cost solution by replacing the multiple oscillators on the PC motherboards. It can be used with Green PC, laptop, or notebook computers to save power by running the entire system at much slower than normal CPU speed.

Example of PCI Bus Based Board Design

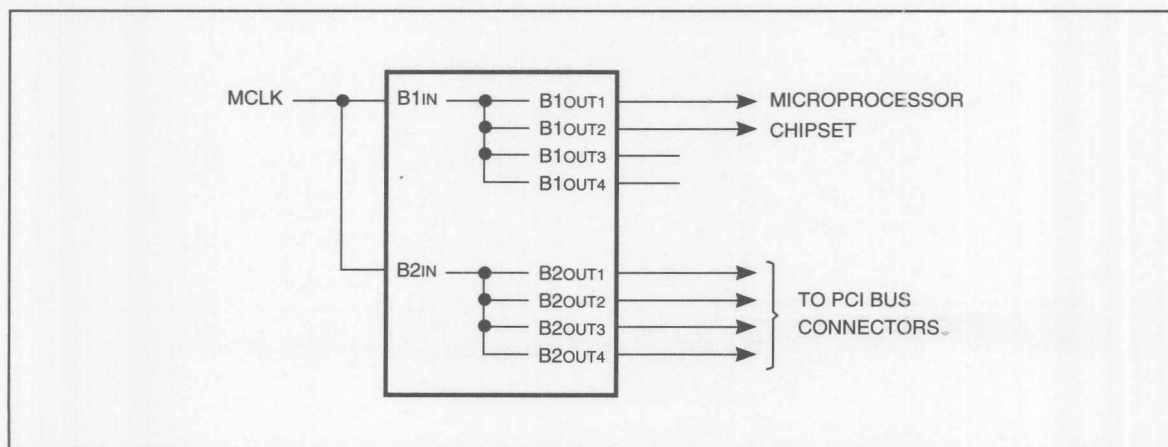
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PI6C468 Block Diagram



Example of PCI-Bus Based Board Design



Product Pin Configuration

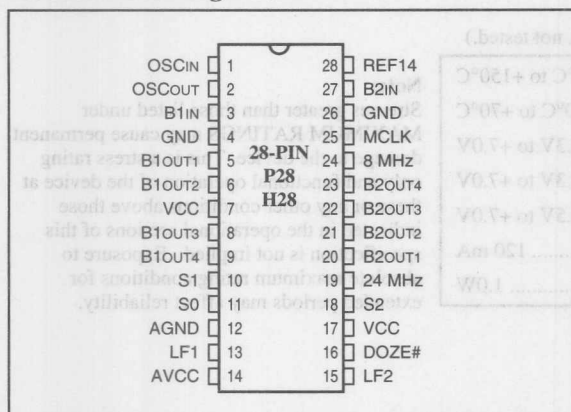


Table 1. Frequency Selection

Inputs			MCLK Outputs (MHz)	
S2	S1	S0	DOZE# = 1	DOZE# = 0
0	0	0	66.6	16
0	0	1	80	16
0	1	0	60	33.3
0	1	1	30	8
1	0	0	33.3	8
1	0	1	40	8
1	1	0	50	16
1	1	1	25	8

Product Pin Description

Pin Name	Description
OSCin, OSCout	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as input for an externally generated reference signal.
S0, S1, S2	Standard frequency select inputs. These inputs control the high-speed MCLK frequency selection. S2-S0 inputs control the CPU clock frequencies. All these inputs have internal pull-ups. Table 1 shows the output frequency selection conditions.
MCLK	Master clock outputs. Programmable output frequencies can be selected using S2-S0 inputs shown in Table 1.
DOZE#	DOZE control pin. When DOZE# is HIGH, the clock chip operates in the standard mode. When this pin goes LOW, output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occur smoothly to allow tracking by 486 CPU internal PLL. This pin has an internal pull-up.
B1in, B2in	On-chip buffer input. These pins have an internal pull-up.
B1OUT1 – B1OUT4 B2OUT1 – B2OUT4	Buffer output pins of B1in. These buffers are capable of sink or source 12 mA. They can be used to buffer critical clock lines for PCI or VESA applications.
24 MHz	24 MHz floppy drive clock output.
8 MHz	8 MHz clock output.
REF14	14.318 MHz output. Buffered outputs for the on-chip reference oscillator or externally provided reference.
LF1, LF2	Connect to an external capacitor.
GND	Circuit ground.
AGND	Analog circuit ground.
Vcc	Positive power supply.
AVcc	Analog positive power supply.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Vcc = 5V ±10%, TA = 0°C to +70°C)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	S2-S0 Inputs, B1IN, B2IN Inputs	2.0	—	—	V
V _{IL}	Input LOW Voltage	S2-S0 Inputs, B1IN, B2IN Inputs	—	—	0.8	V
I _{IH}	Input HIGH Current with Pull-up or Pull-down	S2-S0 Inputs, B1IN, B2IN Inputs	—	—	5 ±50	μA
I _{IL}	Input LOW Current with Pull-up or Pull-down	S2-S0 Inputs, B1IN, B2IN Inputs	—	—	5 ±50	μA
V _{OH}	Output HIGH Voltage	All Outputs, I _{OH} = -12 mA, including B1OUTX, B2OUTX	2.4	—	—	V
V _{OL}	Output LOW Voltage	All Outputs, I _{OL} = 12 mA, including B1OUTX, B2OUTX	—	—	0.4	V
I _{OS}	Short Circuit Current	Vcc = 5.25V ⁽³⁾ , V _{OUT} = GND	25	—	—	mA
I _C	Dynamic Supply Current	Vcc = 5.0V, MCLK = 50 MHz	—	—	35	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate values specified under Electrical Characteristics for the appropriate device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of test should not exceed one second.

Switching Characteristics (GND = 5V \pm 10%, T_A = 0°C to +70°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t _{PLH} t _{PHL}	Output Rise (0.8V to 2.0V) Fall Time (2.0V to 0.8V) MCLK and REF14 Outputs	30 pF Load	—	—	2	ns
d _T	Duty Cycle MCLK and REF14		—	50/50	45/55	%
t _{PLH} t _{PHL}	Propagation Delay BIN to BOUT	15 pF Load, Measured at 1.4V	2.0	—	6.5	ns
t _{SKW}	Buffer Out Skew B1OUT1-B1OUT4 or B2OUT1-B2OUT4	15 pF Load, Measured at 1.4V	—	—	0.75	ns
T _{JIS}	Jitter One Sigma MCLK and REF14	As Compared with Clock Period	—	—	\pm 2	%
T _{JAB}	Jitter Absolute MCLK and REF14	As Compared with Clock Period	—	—	\pm 5	%

Motherboard Clock Generator

Product Features:

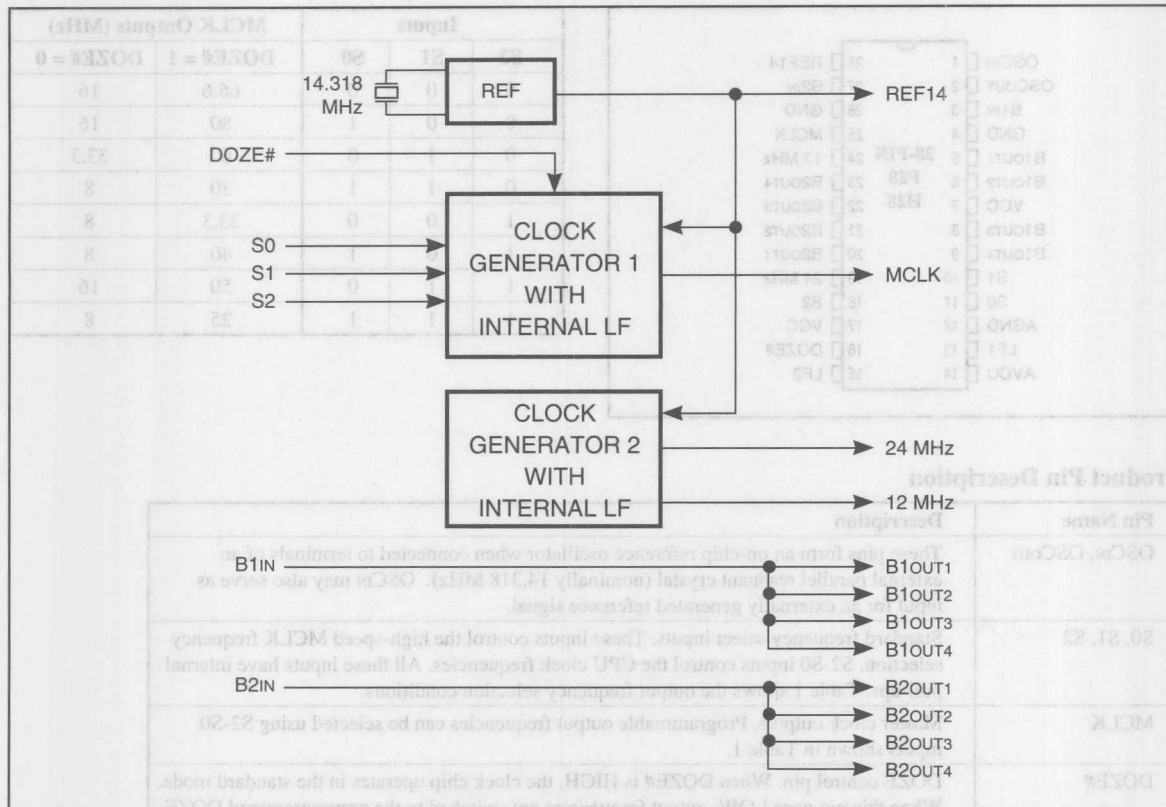
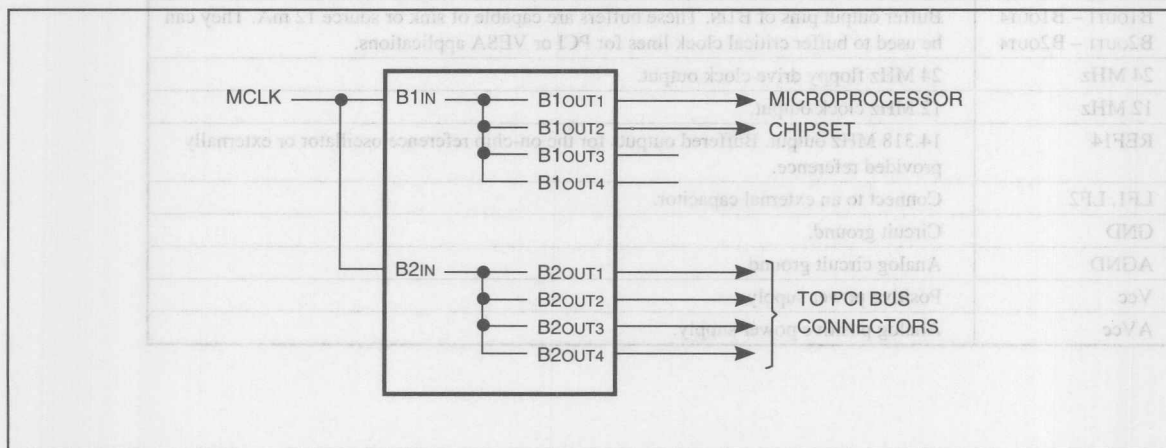
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- Generates all essential clock signals for Intel microprocessor based motherboard design, including 486-SL Enhanced deep green PC design and Pentium™ based designs
- Integrates CPU clock, 24 and 12 MHz peripheral clocks, and Reference clock
- Integrates two clock buffers to generate two banks of one clock input and four low-skew clock outputs, for cost reduction in PCI, VESA, and ISA bus-based motherboards.
- Power down mode for low power consumption
- Smooth and glitch-free frequency transition from one CPU clock to another CPU clock—meeting Intel microprocessor spec
- 50% duty cycle.
- Uses a low cost 14.318 MHz crystal as reference frequency
- Very low short and long term jitter
- Packages available:
 - 28-pin 300 mil wide plastic PDIP (P28)
 - 28 pin 209 mil wide plastic SSOP (H28)

Product Description:

The PI6C471 motherboard clock generator is a low cost clock generator which generates multiple clocks needed by a motherboard, including a MCLK clock signal, selectable from many popular microprocessor frequencies, plus several peripheral clocks. The MCLK clock has the eleven options of 80, 66.6, 60, 50, 40, 33.3, 30, and 25 MHz, giving flexibility to the user. The frequency selection on the MCLK output is determined by the S0-S2 pins and other control pins. Two peripheral clocks with fixed frequency of 24 and 12 MHz are also provided. In addition, a REF14 output provides a buffered reference frequency of 14.318 MHz.

DOZE# pin gives additional flexibility to the user for Green PC applications. Activating the DOZE# pin smoothly switches the MCLK output down to preprogrammed DOZE frequency. Deactivating the DOZE input allow the MCLK output to return to full speed. The PI6C462 includes two independent VCO's.

The PI6C462 offers the low cost solution by replacing the multiple oscillators on the PC motherboards. It can be used with Green PC, laptop, or notebook computers to save power by running the entire system at much slower than normal CPU speed.

PI6C471 Block Diagram

Example of PCI-Bus Based Board Design


Product Pin Configuration

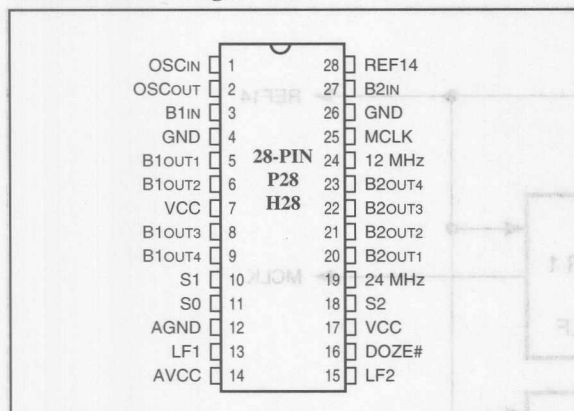


Table 1. Frequency Selection

Inputs			MCLK Outputs (MHz)	
S2	S1	S0	DOZE# = 1	DOZE# = 0
0	0	0	66.6	16
0	0	1	80	16
0	1	0	60	33.3
0	1	1	30	8
1	0	0	33.3	8
1	0	1	40	8
1	1	0	50	16
1	1	1	25	8

Product Pin Description

Pin Name	Description
OSCIN, OSCOUT	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCIN may also serve as input for an externally generated reference signal.
S0, S1, S2	Standard frequency select inputs. These inputs control the high-speed MCLK frequency selection. S2-S0 inputs control the CPU clock frequencies. All these inputs have internal pull-ups. Table 1 shows the output frequency selection conditions.
MCLK	Master clock outputs. Programmable output frequencies can be selected using S2-S0 inputs shown in Table 1.
DOZE#	DOZE control pin. When DOZE# is HIGH, the clock chip operates in the standard mode. When this pin goes LOW, output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occur smoothly to allow tracking by 486 CPU internal PLL. This pin has an internal pull-up.
B1IN, B2IN	On-chip buffer input. These pins have an internal pull-up.
B1OUT1 – B1OUT4 B2OUT1 – B2OUT4	Buffer output pins of B1IN. These buffers are capable of sink or source 12 mA. They can be used to buffer critical clock lines for PCI or VESA applications.
24 MHz	24 MHz floppy drive clock output.
12 MHz	12 MHz clock output.
REF14	14.318 MHz output. Buffered outputs for the on-chip reference oscillator or externally provided reference.
LF1, LF2	Connect to an external capacitor.
GND	Circuit ground.
AGND	Analog circuit ground.
Vcc	Positive power supply.
AVcc	Analog positive power supply.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Vcc = 5V ±10%, TA = 0°C to +70°C)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	S2-S0 Inputs, B1IN, B2IN Inputs	2.0	—	—	V
V _{IL}	Input LOW Voltage	S2-S0 Inputs, B1IN, B2IN Inputs	—	—	0.8	V
I _{IH}	Input HIGH Current with Pull-up or Pull-down	S2-S0 Inputs, B1IN, B2IN Inputs	—	—	5 ±50	μA
I _{IL}	Input LOW Current with Pull-up or Pull-down	S2-S0 Inputs, B1IN, B2IN Inputs	—	—	5 ±50	μA
V _{OH}	Output HIGH Voltage	All Outputs, I _{OH} = -12 mA, including B1OUTX, B2OUTX	2.4	—	—	V
V _{OL}	Output LOW Voltage	All Outputs, I _{OL} = 12 mA, including B1OUTX, B2OUTX	—	—	0.4	V
I _{OS}	Short Circuit Current	Vcc = 5.25V ⁽³⁾ , V _{OUT} = GND	25	—	—	mA
I _C	Dynamic Supply Current	Vcc = 5.0V, MCLK = 50 MHz	—	—	35	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate values specified under Electrical Characteristics for the appropriate device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of test should not exceed one second.

Switching Characteristics (GND = 5V \pm 10%, T_A = 0°C to +70°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t _{PLH} t _{PHL}	Output Rise (0.8V to 2.0V) Fall Time (2.0V to 0.8V) MCLK and REF14 Outputs	30 pF Load	—	—	2	ns
d _T	Duty Cycle MCLK and REF14		—	50/50	45/55	%
t _{PLH} t _{PHL}	Propagation Delay BIN to BOUT	15 pF Load, Measured at 1.4V	2.0	—	6.5	ns
t _{SKEW}	Buffer Out Skew B1OUT1-B1OUT4 or B2OUT1-B2OUT4	15 pF Load, Measured at 1.4V	—	—	0.75	ns
T _{JIS}	Jitter One Sigma MCLK and REF14	As Compared with Clock Period	—	—	\pm 2	%
T _{JAB}	Jitter Absolute MCLK and REF14	As Compared with Clock Period	—	—	\pm 5	%

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V _{IN}	Input HIGH Voltage	2.5-2.0 Input, B1in, B2in Inputs	—	2.0	—	V
V _{IL}	Input LOW Voltage	2.5-2.0 Input, B1in, B2in Inputs	—	—	0.8	V
I _{IN}	Input HIGH Current with Pull-up or Pull-down	2.5-2.0 Input, B1in, B2in Inputs	—	—	3 \pm 10	μ A
I _{IL}	Input LOW Current with Pull-up or Pull-down	2.5-2.0 Input, B1in, B2in Inputs	—	—	3 \pm 10	μ A
V _{OH}	Output HIGH Voltage	All Outputs, I _{OH} = -12 mA, including B1out, B2out	—	2.4	—	V
V _{OL}	Output LOW Voltage	All Outputs, I _{OL} = 12 mA, including B1out, B2out	—	—	0.4	V
I _{OS}	Short Circuit Current	V _{CC} = 3.3V, V _{OUT} = GND	—	35	—	mA
I _C	Dynamic Supply Current	V _{CC} = 3.0V, MCLK = 50 MHz	—	—	35	mA

NOTES:

1. For conditions not shown as Min. or Max., use appropriate values specified under Electrical Characteristics for the appropriate device type.
2. Typical values are at V_{CC} = 3.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of test should not exceed one second.

GENERAL INFORMATION**1****STANDARD AND 25Ω OUTPUT RESISTOR SERIES
5V FCT LOGIC PRODUCTS****2****DOUBLE DENSITY STANDARD
5V FCT LOGIC PRODUCTS****3****DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS****4****STANDARD 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****5****DOUBLE DENSITY 3.3V LOGIC PRODUCTS
WITH 5V TOLERANT I/O****6****SPECIALTY LOGIC PRODUCTS****7****BUS SWITCH PRODUCTS****8****CLOCK DISTRIBUTION PRODUCTS****9****CLOCK GENERATOR PRODUCTS****10****NETWORKING PRODUCTS****11****APPLICATION NOTES****12****QUALITY AND RELIABILITY INFORMATION****13****PACKAGE MECHANICAL OUTLINES****14****SALES AND DISTRIBUTION LOCATIONS****15**

**FREQUENCY SYNTHESIS
PRODUCTS**

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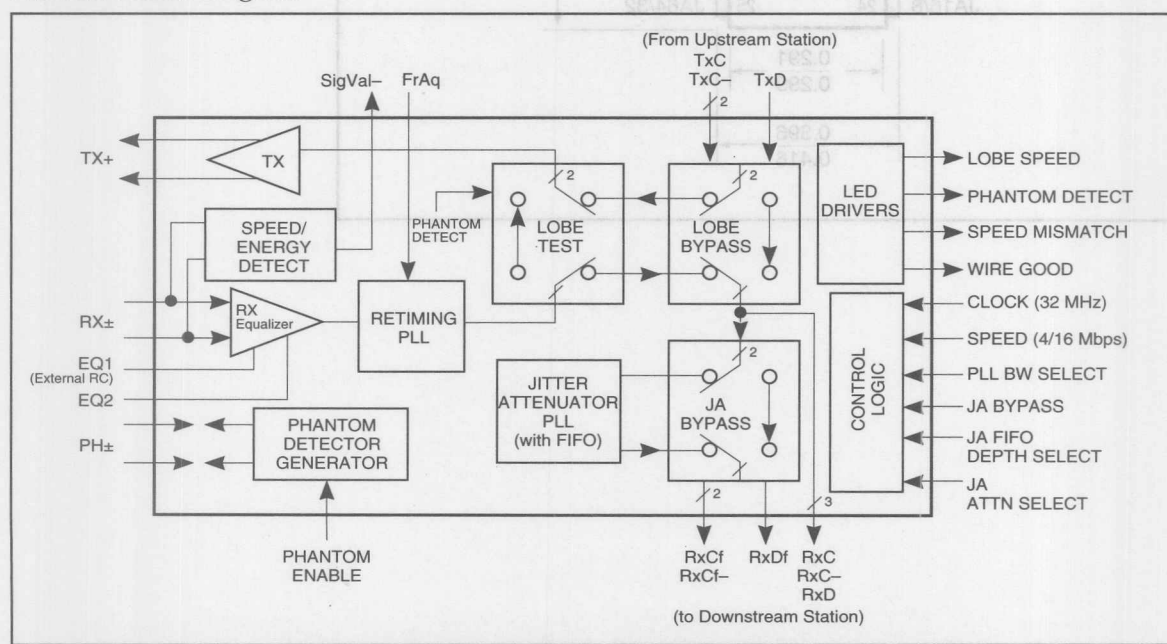
Part Number	Description	Page No.
PI6C3000	Token Ring Active Retiming Hub Interface Chip	11.1

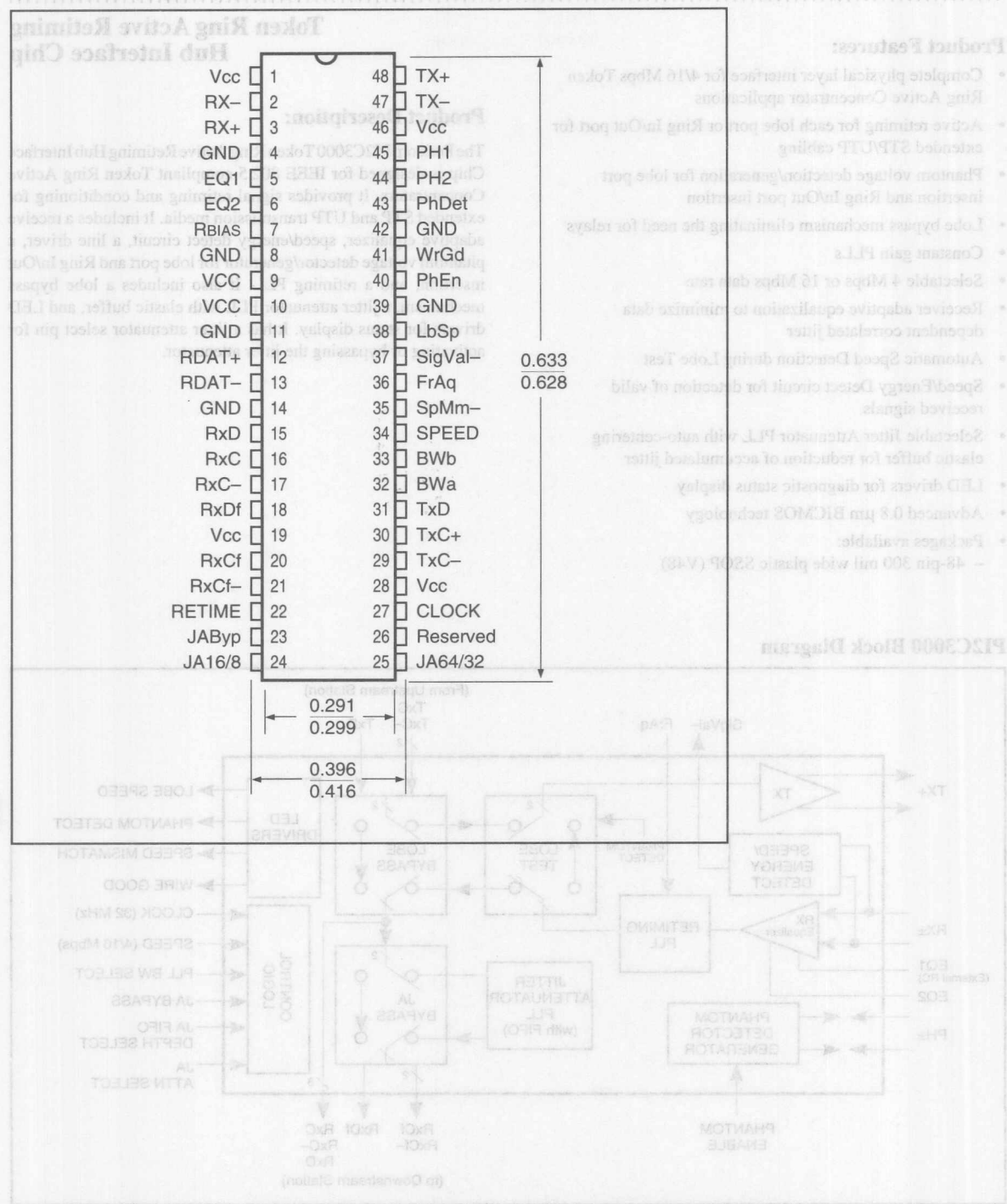
Product Features:

- Complete physical layer interface for 4/16 Mbps Token Ring Active Concentrator applications
- Active retiming for each lobe port or Ring In/Out port for extended STP/UTP cabling
- Phantom voltage detection/generation for lobe port insertion and Ring In/Out port insertion
- Lobe bypass mechanism eliminating the need for relays
- Constant gain PLLs
- Selectable 4 Mbps or 16 Mbps data rate
- Receiver adaptive equalization to minimize data dependent correlated jitter
- Automatic Speed Detection during Lobe Test
- Speed/Energy Detect circuit for detection of valid received signals
- Selectable Jitter Attenuator PLL with auto-centering elastic buffer for reduction of accumulated jitter
- LED drivers for diagnostic status display
- Advanced 0.8 μ m BICMOS technology
- Packages available:
 - 48-pin 300 mil wide plastic SSOP (V48)

Token Ring Active Retiming Hub Interface Chip
Product Description:

The Pericom PI2C3000 Token Ring Active Retiming Hub Interface Chip is designed for IEEE 802.5 compliant Token Ring Active Concentrators. It provides signal retiming and conditioning for extended STP and UTP transmission media. It includes a receive adaptive equalizer, speed/energy detect circuit, a line driver, a phantom voltage detector/generator for lobe port and Ring In/Out insertion, and a retiming PLL. It also includes a lobe bypass mechanism, a jitter attenuator PLL with elastic buffer, and LED drivers for status display. It has a jitter attenuator select pin for activating or bypassing the jitter attenuator.

PI2C3000 Block Diagram


Product Pin Configuration


ARCHITECTURE

Receiver Section

The receiver section consists of the receiver equalizer, the energy detect circuit, and the retiming PLL. The receiver equalizer is a two-state amplitude adaptive equalizer. It uses the same equalizer for either 4 or 16 Mbps. It operates in nonlinear region for large signals (short cable) thereby effectively disabling the equalization, and it operates in linear region for small signals (long cable) providing amplification for higher frequency signal components. External RC components are required to set the filtering characteristics of the equalizer. The Energy/Speed Detect Circuit checks for the transition density of the incoming signal. When the required transition density is met in accordance with the speed configuration (4/16 Mbps) selected, a Signal Valid indication is given to the Retiming PLL so that the PLL can lock on to the incoming signal. The Retiming PLL is frequency-locked to the local crystal in the absence of valid received signal. The presence of valid received signal configures the retiming PLL to phase lock to the incoming signal (via the external connection from SigVal- to FrAq). The Retiming PLL is a constant gain PLL; no external loop filter is required. The PLL bandwidth is determined by the BWa and BWb control pins; it can be set to the maximum bandwidth when the jitter attenuator is activated.

Phantom Detector/Generator and Lobe Bypass

The phantom detector senses for the DC phantom voltage generated by the lobe station. The phantom voltage generated by the station is an indication to the concentrator that the station wants to be inserted in the ring. In the absence of phantom voltage, the lobe bypass circuit is in the lobe bypass state and the retiming PLL output is routed to the line driver for lobe test purposes. Upon receipt of the phantom voltage, transmit clock and data (TxC and TxD) of the upstream station are routed to the line driver, and the received clock and data (RxC and RxD) of the lobe station are routed to the downstream station.

For hub interconnection, the Ring-In port of the second hub generates the phantom voltage and the Ring-Out port of the first hub detects the phantom voltage in a similar manner that a lobe station is inserted in the ring. A "wire good" indication is provided in the Ring-In port of the second hub, and a "phantom detect" indication is provided in the Ring-Out port of the first hub to validate the integrity of the connection.

Transmitter

The line driver takes the transmit clock and differential Manchester data of the upstream station and drives the cable in the normal lobe-insert state. It takes the received clock and data from the upstream previous station during lobe test (prior to lobe insertion). The line driver is idle (no data transitions) in the absence of valid received signal or phantom voltage. The Line Driver is a current output requiring a step-down (2:1) isolation transformer. The drive current is 25 mA.

Jitter Attenuator PLL

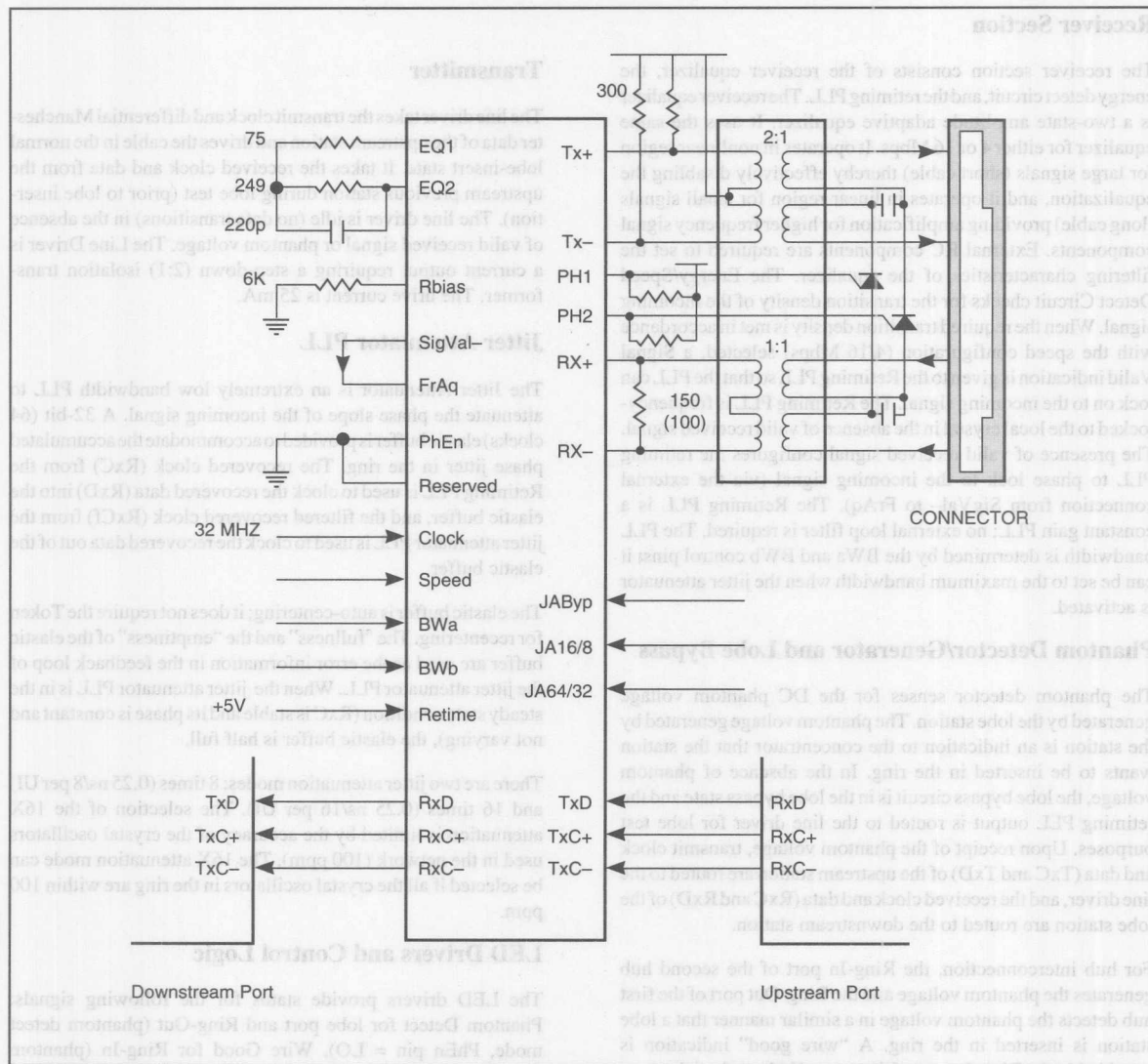
The Jitter Attenuator is an extremely low bandwidth PLL to attenuate the phase slope of the incoming signal. A 32-bit (64 clocks) elastic buffer is provided to accommodate the accumulated phase jitter in the ring. The recovered clock (RxC) from the Retiming PLL is used to clock the recovered data (RxD) into the elastic buffer, and the filtered recovered clock (RxCf) from the jitter attenuator PLL is used to clock the recovered data out of the elastic buffer.

The elastic buffer is auto-centering; it does not require the Token for recentering. The "fullness" and the "emptiness" of the elastic buffer are used as the error information in the feedback loop of the jitter attenuator PLL. When the jitter attenuator PLL is in the steady state condition (RxC is stable and its phase is constant and not varying), the elastic buffer is half full.

There are two jitter attenuation modes: 8 times (0.25 ns/8 per UI) and 16 times (0.25 ns/16 per UI). The selection of the 16X attenuation is limited by the accuracy of the crystal oscillators used in the network (100 ppm). The 16X attenuation mode can be selected if all the crystal oscillators in the ring are within 100 ppm.

LED Drivers and Control Logic

The LED drivers provide status for the following signals: Phantom Detect for lobe port and Ring-Out (phantom detect mode, PhEn pin = LO), Wire Good for Ring-In (phantom generate mode, PhEn pin = HI), valid received signal, lobe speed, and speed mismatch. The Control Logic sets the following: hub speed selection, PLL bandwidth selection, and jitter attenuator selection.



APPLICATION NOTES

GENERAL INFORMATION

STANDARD AND 25Ω OUTPUT RESISTOR SERIES 5V FCT LOGIC PRODUCTS

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12.3	STANDARD 3.3V LOGIC PRODUCTS WITH 5V TOLERANT I/O	3
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BUS SWITCH PRODUCTS

CLOCK DISTRIBUTION PRODUCTS

CLOCK GENERATOR PRODUCTS

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APPLICATION NOTES

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GROUND BOUNCE IN HIGH SPEED LOGIC

Today's demand for higher speed systems is for increased performance, but with strong consideration for power usage. Traditionally, high-drive bus interface logic have been implemented in Bipolar technology, but recent years have witnessed strong demand for a CMOS counterpart series called FCT. In fact, FCT has evolved to deliver far greater performance (shorter propagation delays) than is available in Bipolar technology, thus becoming the only available avenue for very high-speed system designers. Maintaining the same high output drive capabilities as the Bipolar products (64 mA sink), FCT circuits from Pericom Semiconductor are now available with propagation delay down to 3.6 ns (maximum) for some functions. However, speed improvements and power reduction has not come without some penalties in the form of a noise phenomena called "Ground Bounce."

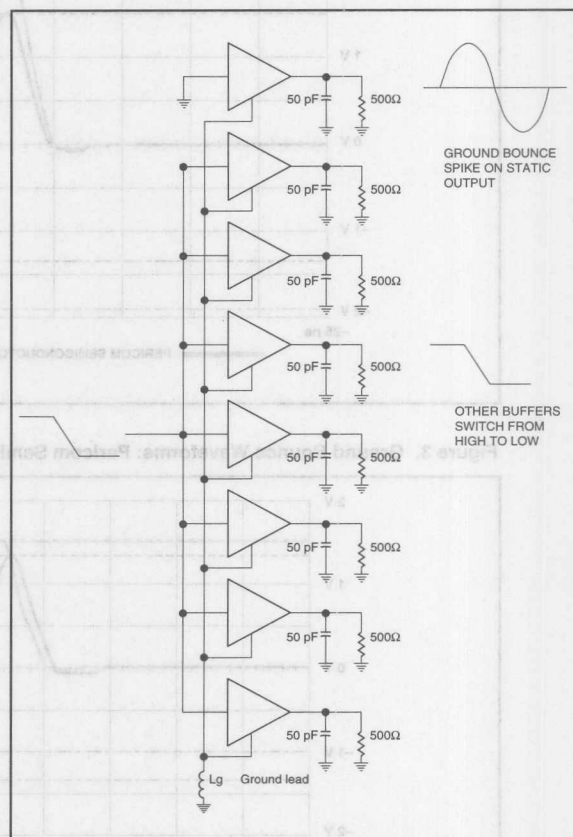
Ground Bounce is the simultaneous switching noise of outputs during the logic HIGH to LOW transition and the resultant potential difference between the chip ground and the external ground plane. When several outputs switch simultaneously, the total build up of current in the common ground or Vcc lead inductance can be substantial. The noise becomes more pronounced as the output edge rate and the drive capability increase or as more current is switched through the ground lead.

Pericom Semiconductor's FCT products are designed to have low ground bounce. The FCT family is TTL compatible and the output swing is limited to 3.4 volt TTL output swings instead of 5 volts. This reduces the discharge current through the ground lead and reduces maximum noise by 30 to 40%. Specially optimized control circuits are designed to gradually turn on the output driver to reduce ground bounce while achieving high speed. Optimized layout of the power and ground lines in the chip further reduces ground bounce.

Ground bounce and speed characterization were done on a special bench setup as shown in Figure 1. Ground bounce measurement was done with seven bits simultaneously driven

from logic HIGH to logic LOW and the remaining bit tied to ground. The noise voltage waveform generated at the undriven bit (quiet bit) is measured and represents the worst case ground bounce noise. This is the standard setup and measurement in characterizing ground bounce. On system boards, the noise characteristics are usually much lower with proper board design.

Figure 1. Typical Ground Bounce Evaluation Setup



An FCT244 device in a plastic DIP package from Pericom Semiconductor and two other suppliers were characterized with the setup as shown in Fig. 1. Figures 2 and 3 compare the waveforms of the output voltage transitions and the corresponding ground bounce as observed at the undriven LOW output. Table 1 summarizes the results. The results show that Pericom Semiconductor's FCT device has significantly lower ground bounce compared to the other suppliers.

Table 1. Ground Bounce Comparison at room temperature Pericom Semiconductor vs Competitors 1 and 2.

Unit	Speed (ns)		Ground Bounce (V)	
	T _{PHL}	T _{PLH}	Pos.	Neg.
PSC, D Speed	2.84	2.88	1.52	1.28
Comp. 1, D Speed	2.92	3.08	2.04	1.88
PSC, C Speed	3.2	3.4	1.32	1.00
Comp. 2, C Speed	3.24	3.84	1.52	1.34

Figure 2. Ground Bounce Waveforms: Pericom Semiconductor vs Competitor 1.

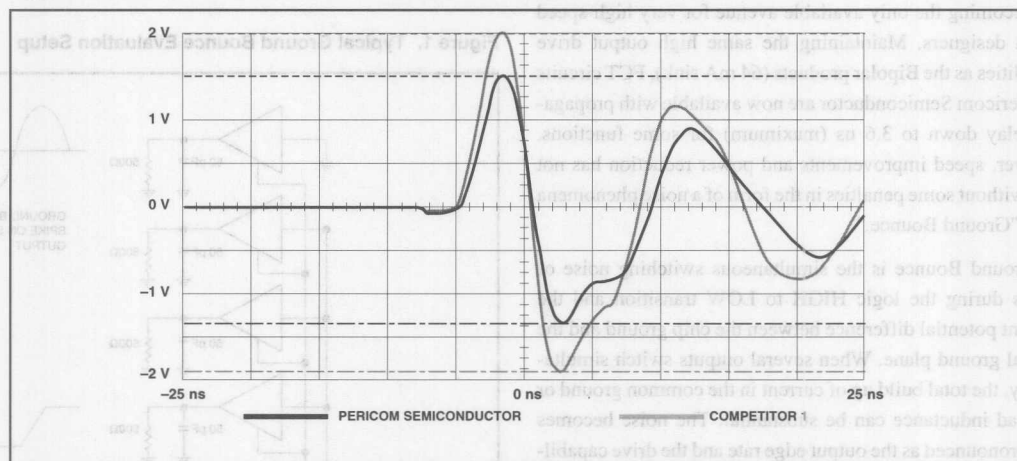
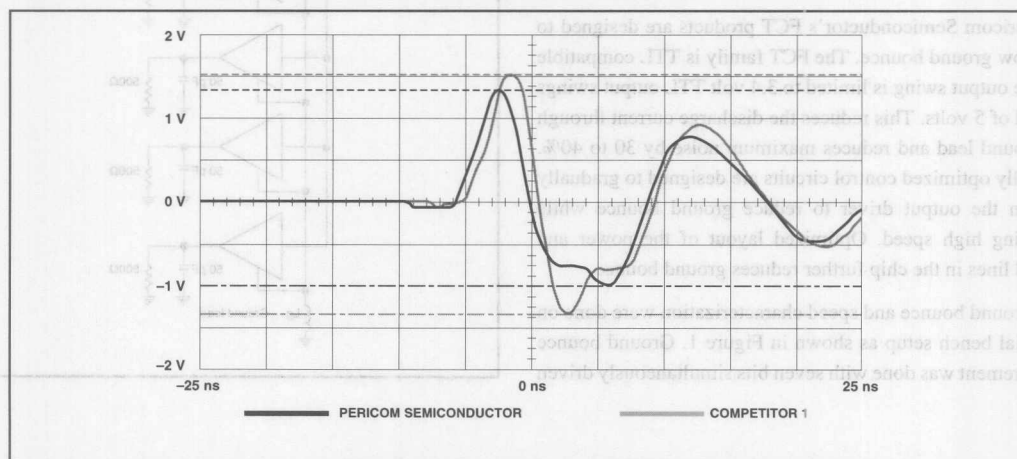


Figure 3. Ground Bounce Waveforms: Pericom Semiconductor vs Competitor 2.



Key to High Speed Low Noise Design

Ground bounce can only be minimized or circumvented, but rarely eliminated since the parasitic inductance cannot be totally removed from the package. Figure 4 shows a simplified circuit model to help explore several key factors which are critical for good ground bounce control design.

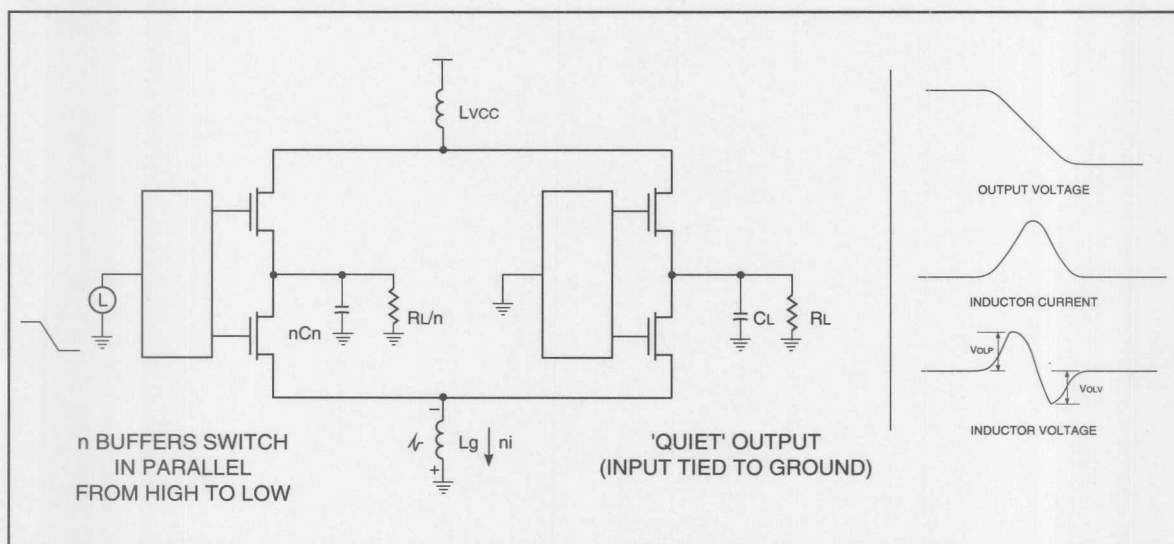
During the output HIGH to LOW transition, the sum of output load current and all switching current through the device flows through the ground lead and generates noise voltage. Several factors affect the amplitude of this voltage:

- Number of outputs switching simultaneously. The more outputs switching simultaneously, the more ground bounce.
- Magnitude of lead inductance. Higher lead inductance results in greater ground bounce. Thus, a package with less parasitic ground lead inductance would result in better noise performance.

- **Output voltage swing.** Higher output voltage swing would result in higher ground bounce. Thus, a CMOS compatible output with 5 volts V_{OH} would inherently result in higher noise than a TTL compatible output with lower V_{OH} voltage.
- **Output edge rate.** The output edge rate determines how fast the current discharges through the ground lead inductor. Since the transient voltage across an inductor increases with the rate of change of the current, the faster the rate, the higher the noise. Thus it is very critical to control this output edge rate to get low noise performance.

Pericom Semiconductor addresses these issues directly at the outset of the design. First, we design our FCT products to be TTL compatible. This limits the output swing to 3.4 volts instead of 5 volts. This reduces the maximum noise as the

Figure 4. Simplified Circuit Model



maximum output swing is lowered. To control the output edge rate without compromising speed, a proprietary control circuit is designed to gradually turn on the output driver to optimize the speed performance and ground bounce characteristics. Also, alternative package choices complement the high-speed low-noise design. Plastic DIP packages have the highest lead inductance and hence, the worst ground bounce characteristics. Packages like SOIC and QSOP have much lower lead inductance and hence, much lower ground bounce. Table 2 shows a comparison of package inductance and estimated ground bounce. It is evident that the surface mount packages (SOIC, QSOP) offer system designers the advantages of reduced board space, higher speed performance and lower ground bounce.

Table 2. Ground Bounce Package Comparison.

Package	Ground Lead Inductance	Relative Ground Bounce
PDIP	13.7 nH	100%
SOIC	8.5 nH	80%
QSOP	3.6 nH	50%

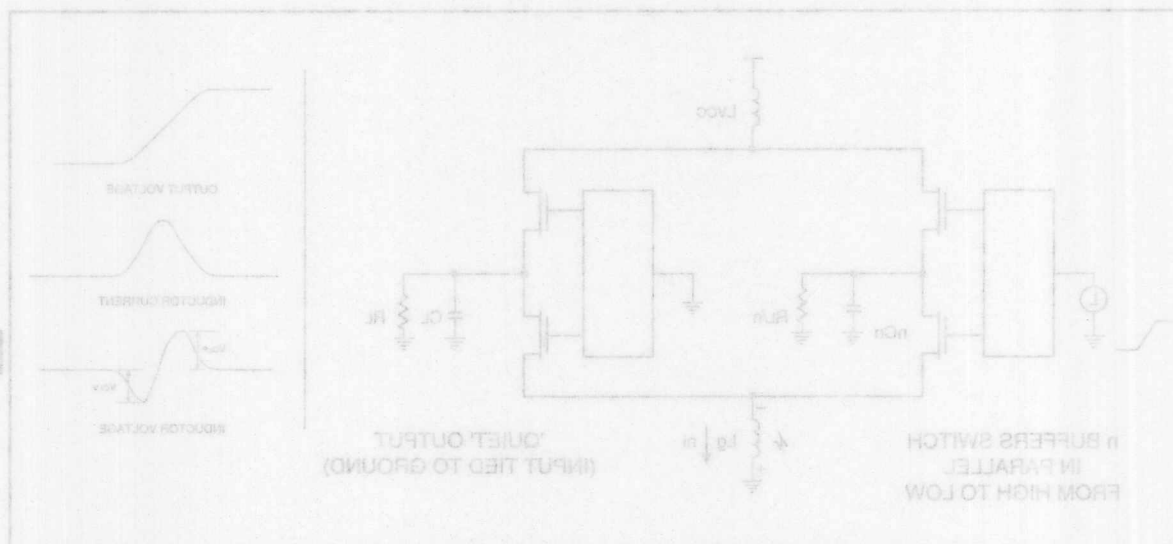


Figure 4. Simplified Circuit Model

FCT CHARACTERIZATION AND QUALIFICATION DATA

FEATURES OF PERICOM SEMICONDUCTOR'S 0.8 MICRON HIGH-SPEED CMOS PROCESS

Pericom Semiconductor's bus interface logic products are fabricated in Pericom Semiconductor's advanced CMOS technology to achieve industry leading speed grades and high reliability.

Process Features:

- 0.8 micron CMOS process
- NMOS and PMOS LDD devices for reliability and low leakage
- High speed, high drive transistors which can work down to 0.55 μm effective channel length
- Low capacitance and low resistance interconnect for high performance
- Fully planarized metal technology
- Barrier metal technology

Process Outline:

- N well
- N channel punchthrough suppression
- Contact
- Metal 2
- Field/Island
- Poly gate
- N+ Source/Drain
- Metal 1
- Passivation
- Field Implant
- LDD mask
- P+ Source/Drain
- Metal via

Parameters	Conditions	Data		
		125°C	50°C	25°C
t_{in}	50 pF, 3000	3.44	3.68	3.80
t_{out}	50 pF, 3000	3.28	3.52	3.73
t_{out}	OE to AB	3.40	3.80	3.86
t_{out}	OE to AB	3.88	4.16	4.33
t_{out}	OE to AB	3.86	4.08	4.13
t_{out}	OE to AB	3.34	3.74	3.90
t_{out}	OE to AB	—	—	—
t_{out}	OE to AB	—	—	—
t_{out}	OE to AB	—	—	—
t_{out}	OE to AB	—	—	—

Product Features:

- Very high speed (up to D speed)
- Output Delay has low sensitivity to temperature and power supply voltage
- Lower ground bounce compared to other FCT's at the same speed

CHARACTERISTICS SUMMARY

DC Electrical Characteristics

Parameters	Conditions	D Speed Spec.	Data	Units
			25°C	
VOH	IOH = -8 mA IOH = -15 mA	2.4	3.4	V
		2.0	3.1	V
VOL	IOL = 48 mA IOL = 64 mA	—	0.22	V
		0.55	0.28	V
VIH		2.0	1.55	V
VIL		0.8	1.15	V
IiH	VIN = 2.7 V	1	0	µA
IiL	VIN = 0.5 V	-1	0	µA
VIK	IIN = 18 mA	-1.2	-0.7	V
Ios	VOUT = GND	-60	-220	mA

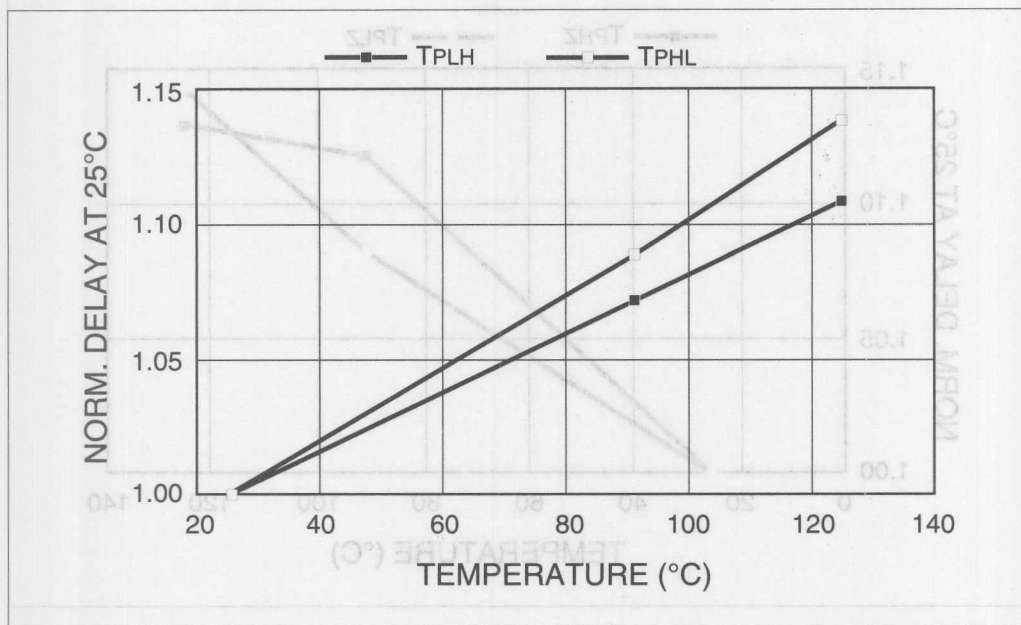
Power Supply Characteristics

Parameters	Conditions	D Speed Spec.	Data	Units
			25°C	
ICC	VIN = GND/VCC	1.5	0	µA
ΔICC	VIN = 3.4 V	2.5	0.948	mA
ICCD	One bit toggle	0.25	0.197	mA/MHz

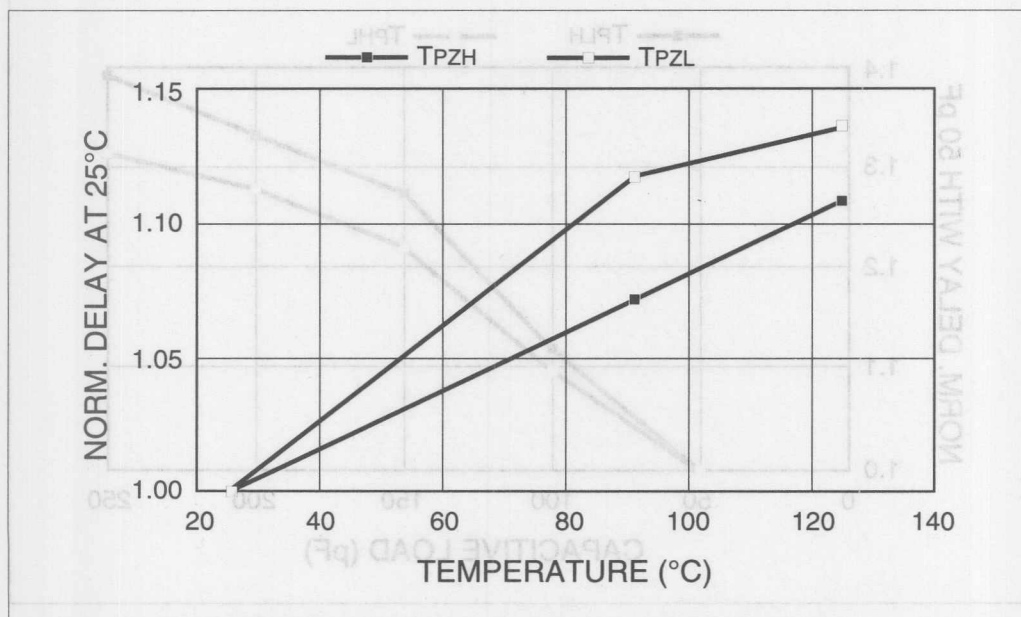
Switching Characteristics

Parameters	Conditions	D Speed Spec.	Data			Units
			25°C	90°C	125°C	
TPLH	50 pF, 500Ω	3.8	3.44	3.68	3.80	ns
TPHL	50 pF, 500Ω	3.8	3.28	3.56	3.72	ns
TPZH	OE to A/B	5.5	3.40	3.80	3.86	ns
TPZL	OE to A/B	5.5	3.88	4.16	4.32	ns
TPHZ	OE to A/B	4.6	3.66	4.08	4.12	ns
TPLZ	OE to A/B	4.6	2.54	2.74	2.90	ns
TPZH	OE to A/B	5.5	—	—	—	ns
TPZL	OE to A/B	5.5	—	—	—	ns
TPHZ	OE to A/B	4.6	—	—	—	ns
TPLZ	OE to A/B	4.6	—	—	—	ns

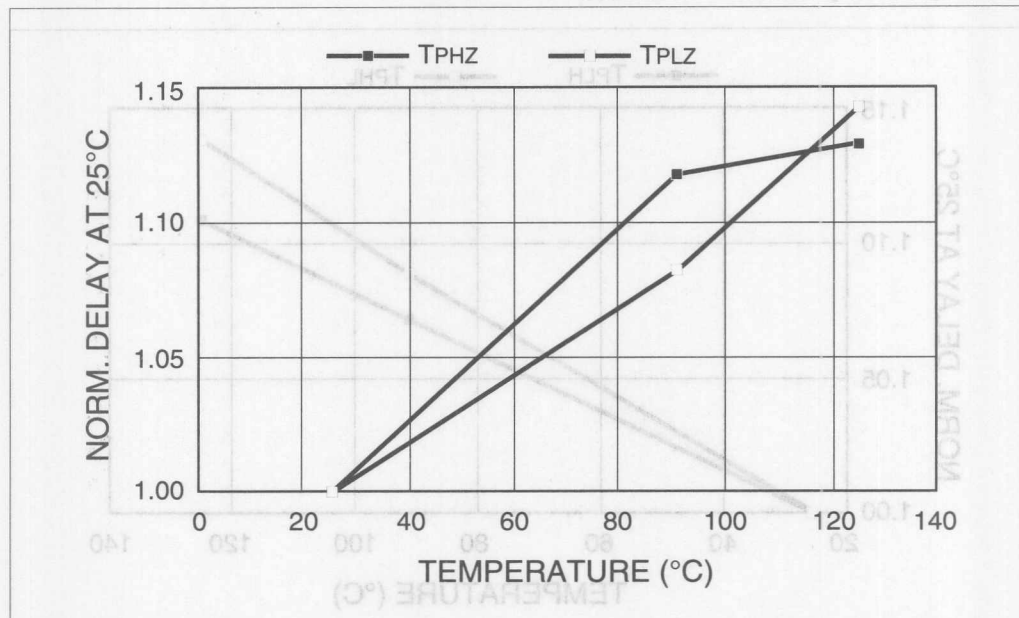
Output Delay vs Temperature — T_{PLH}/T_{PHL}



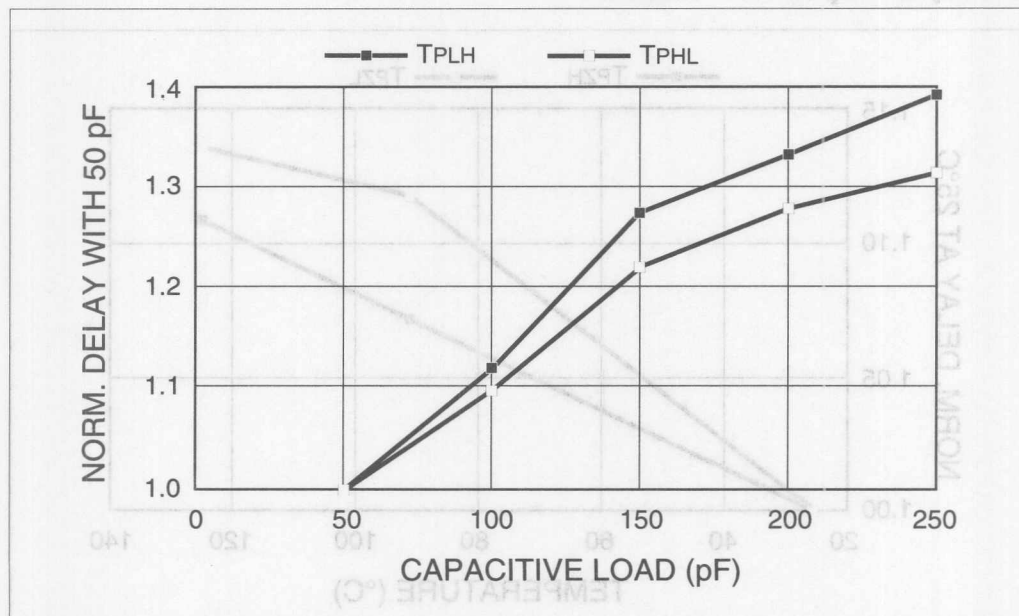
Output Delay vs Temperature — T_{PZH}/T_{PZL}



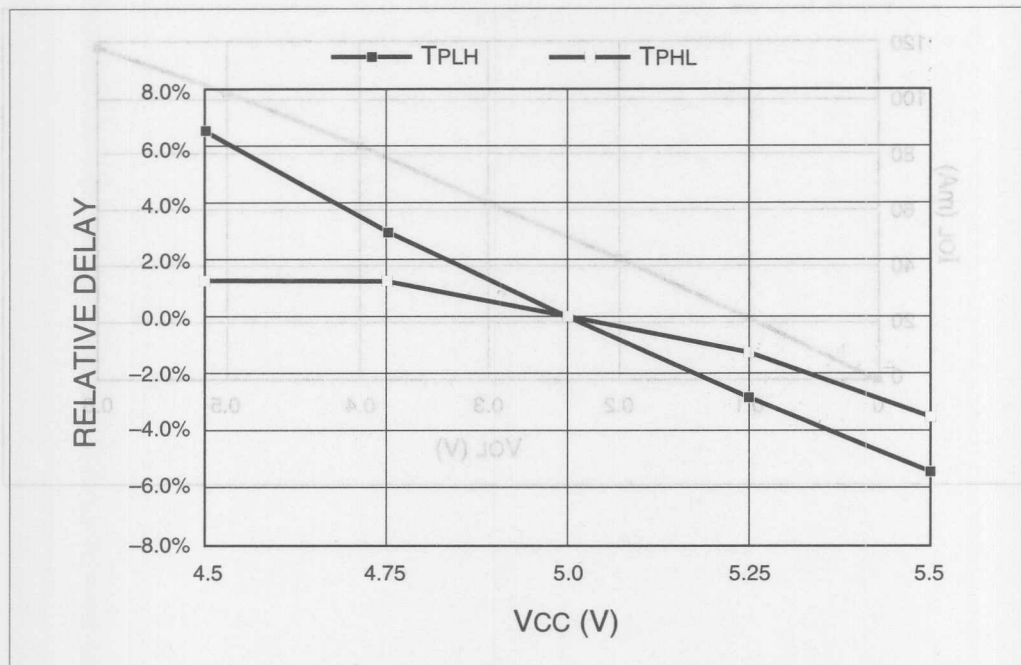
Tristate Delay vs Temperature — T_{PHZ}/T_{PLZ}



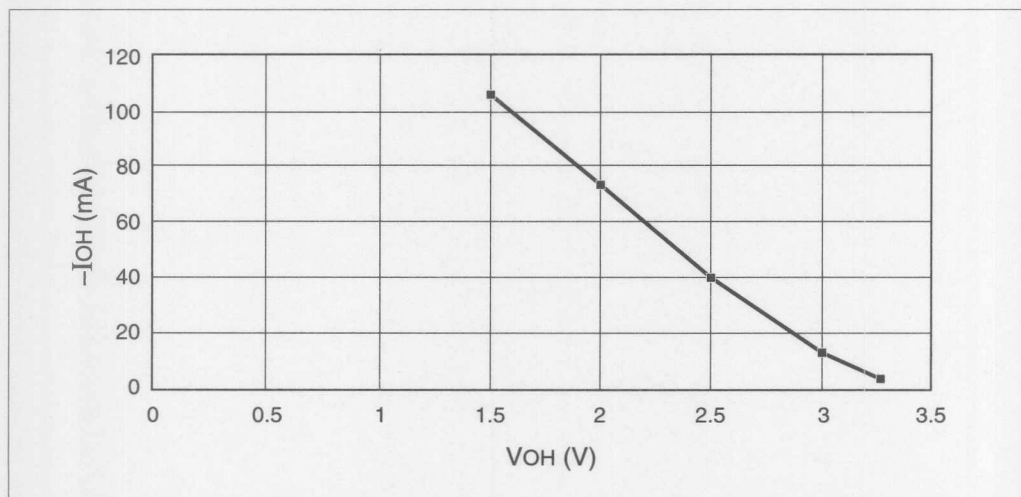
Output Delay vs Output Capacitance — T_{PLH}/T_{PHL}



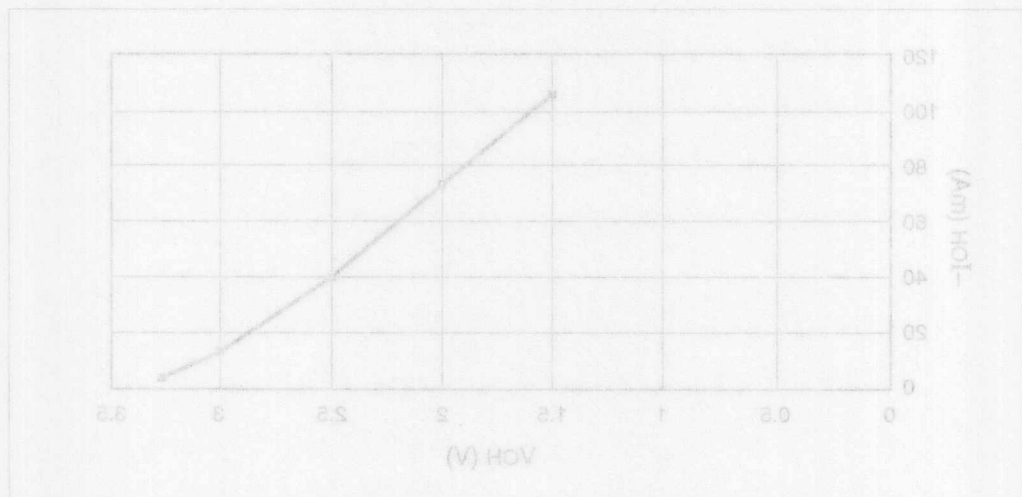
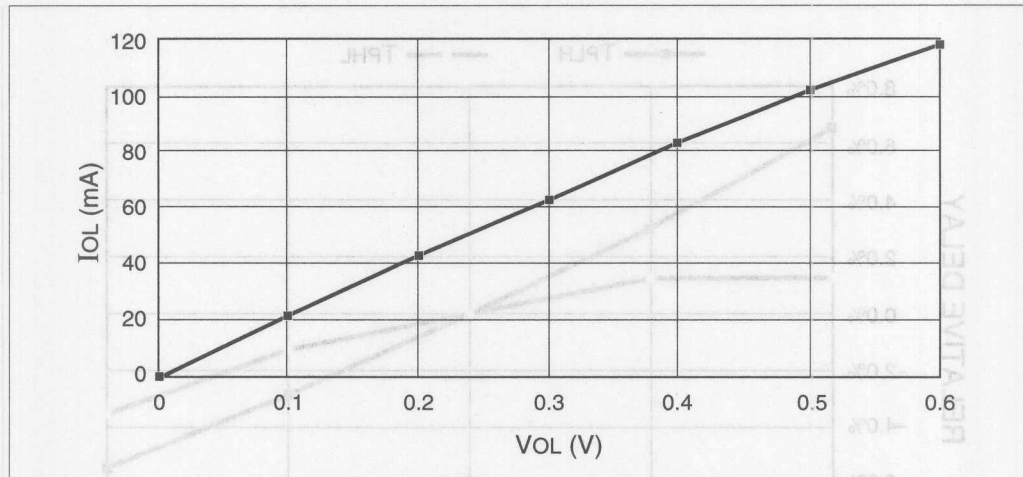
Output Delay vs Power Supply Voltage — TPLH/TPHL



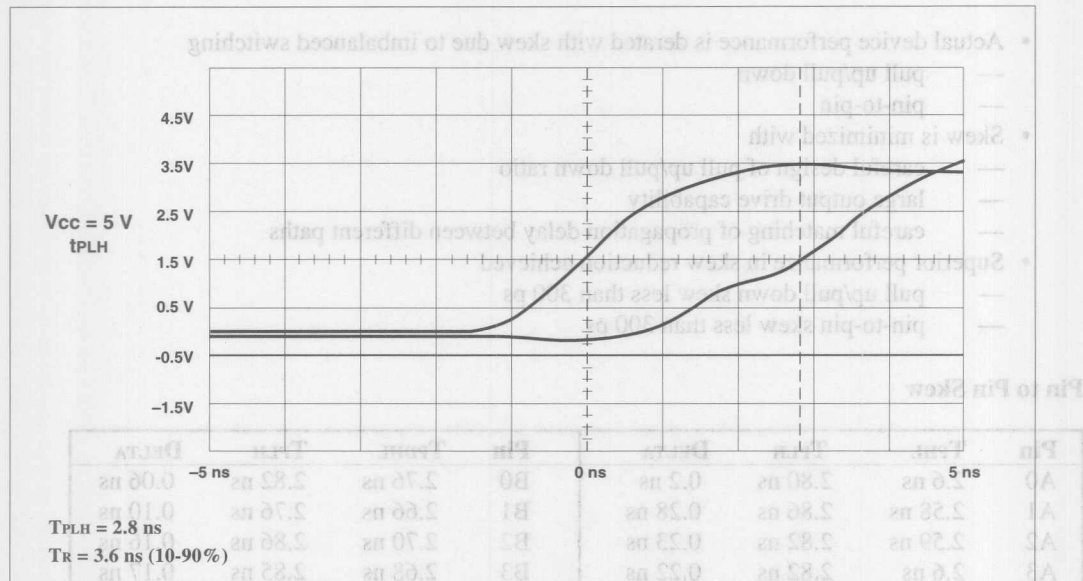
I_{OH} vs V_{OH}



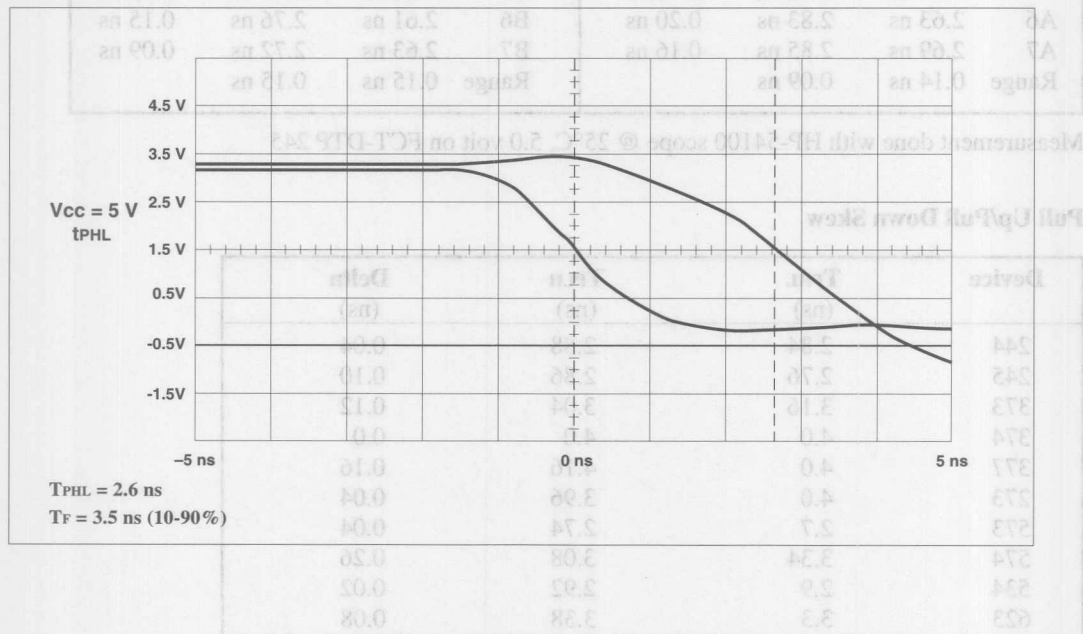
IOL vs VOL



Output Rise Time Characteristics (25°C)



Output Fall Time Characteristics (25°C)



HIGH PERFORMANCE BUS INTERFACE LOGIC

LOW SKEW

- Actual device performance is derated with skew due to imbalanced switching
 - pull up/pull down
 - pin-to-pin
- Skew is minimized with
 - careful design of pull up/pull down ratio
 - large output drive capability
 - careful matching of propagation delay between different paths
- Superior performance in skew reduction achieved
 - pull up/pull down skew less than 300 ps
 - pin-to-pin skew less than 300 ps

Pin to Pin Skew

Pin	T _{PHL}	T _{PLH}	DELTA	Pin	T _{PDHL}	T _{PLH}	DELTA
A0	2.6 ns	2.80 ns	0.2 ns	B0	2.76 ns	2.82 ns	0.06 ns
A1	2.58 ns	2.86 ns	0.28 ns	B1	2.66 ns	2.76 ns	0.10 ns
A2	2.59 ns	2.82 ns	0.23 ns	B2	2.70 ns	2.86 ns	0.16 ns
A3	2.6 ns	2.82 ns	0.22 ns	B3	2.68 ns	2.85 ns	0.17 ns
A4	2.55 ns	2.77 ns	0.22 ns	B4	2.65 ns	2.82 ns	0.17 ns
A5	2.63 ns	2.82 ns	0.19 ns	B5	2.61 ns	2.71 ns	0.10 ns
A6	2.63 ns	2.83 ns	0.20 ns	B6	2.61 ns	2.76 ns	0.15 ns
A7	2.69 ns	2.85 ns	0.16 ns	B7	2.63 ns	2.72 ns	0.09 ns
Range	0.14 ns	0.09 ns		Range	0.15 ns	0.15 ns	

Measurement done with HP-54100 scope @ 25°C, 5.0 volt on FCT-DTP 245

Pull Up/Pull Down Skew

Device	T _{PHL} (ns)	T _{PLH} (ns)	Delta (ns)
244	2.84	2.88	0.04
245	2.76	2.86	0.10
373	3.16	3.04	0.12
374	4.0	4.0	0.0
377	4.0	4.16	0.16
273	4.0	3.96	0.04
573	2.7	2.74	0.04
574	3.34	3.08	0.26
534	2.9	2.92	0.02
623	3.3	3.38	0.08

Measurement done with 1 GHz HP Sampling Scope, @ 25°C, V_{cc} = 5.0 volts.

ZERO DELAY BUS SWITCHES

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Figure 2. Bus Switch Equivalent Circuit When Disabled.



ZERO DELAY BUS SWITCHES

1. Features of Bus Switches

Pericom Semiconductor's bus switch product family has many ideal features very useful in logic circuit design, not provided by TTL logic IC's. These devices are a bus connect device utilizing an enable/disable control, with no propagation delay. Using bus switches, a logic designer can accomplish certain design goals with a very simple and effective circuit.

The Pericom bus switches are high-speed TTL bus connect devices. When they are enabled, the bus switches directly connecting two buses with a connection resistance of less than 5 ohms. Since these devices directly connect the bus signals between two buses, they introduce no propagation delay, timing skew or noise. They are inherently bidirectional and dissipate very little power.

Figure 1 shows the equivalent circuit of a bus switch when enabled. The switch provides a low resistance connection between inputs and outputs for input or output voltage below 3V. Pericom Semiconductor's bus switches have lower resistance, as compared with competitor devices. This low resistance feature of Pericom Semiconductor's devices make them very ideal for bus switching applications.

When the bus switch is disabled, the N-channel transistor gate is at logic 0 level, and the transistor is off. Figure 2 shows that the input pin A and the output pin B are fully isolated when the transistor is off.

Figure 1. Bus Switch Equivalent Circuit When Enabled.

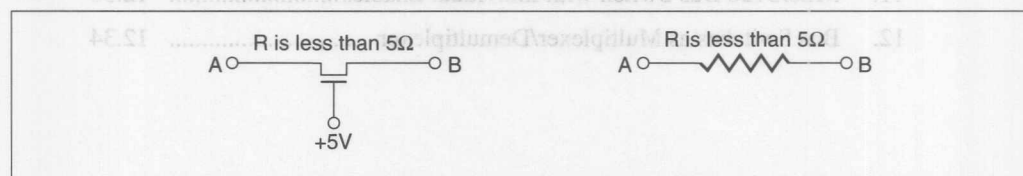
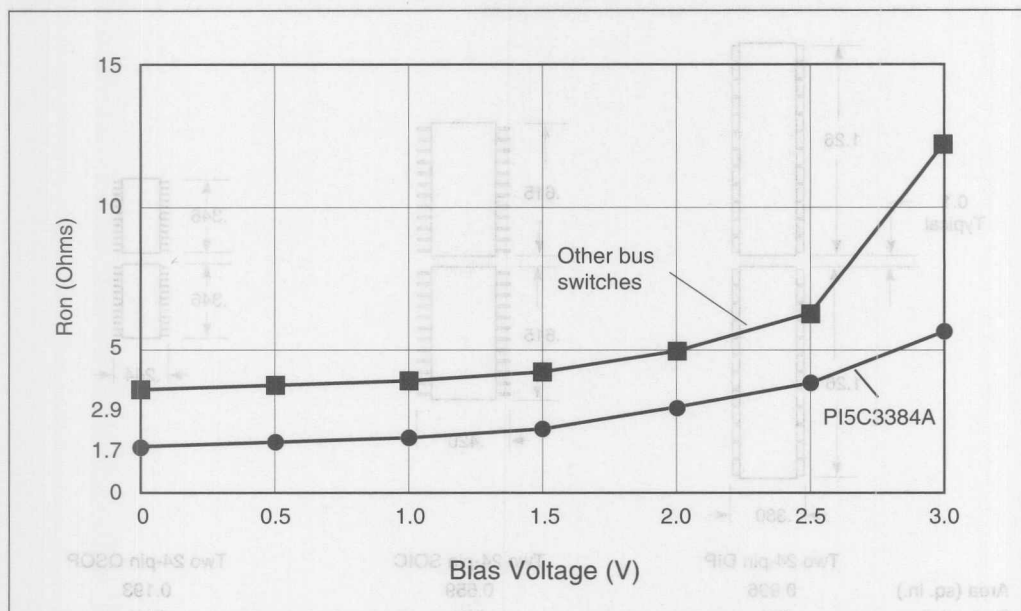


Figure 2. Bus Switch Equivalent Circuit When Disabled.



Figure 3. ON-Resistance of Pericom Semiconductor's Bus Switch, at $V_{CC} = 4.75V$.



The resistance characteristic is shown in Figure 3. If the voltage at point A or point B of Figure 1 is 1V, then most of Pericom Semiconductor's bus switches have only 2 to 3.5 ohm resistance. As the I/O voltage rises above 3V, at both points A and B of Figure 1, the switch resistance increases until the switch turns off, at approximately 4V.

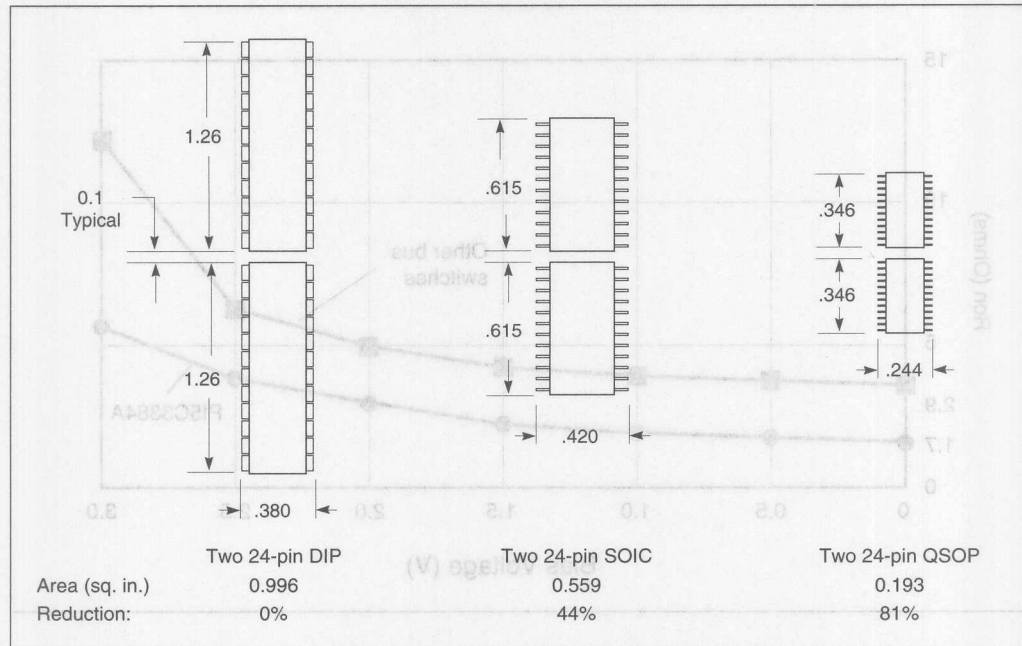
When the I/O voltages are below 3V, the voltages at A and B are identical, since they are connected by an equivalent resistor of less than 5 ohms. Note that the value of resistance is determined by the lower of the voltages on the two I/O pins (points A and B). When the input voltage at point A rises above 4V, the output voltage at point B does not follow the input voltage, but rises and maintains at $V_{CC} - V_T$, where V_{CC} is the supply voltage at pin 24 or pin 20, and V_T is the threshold voltage of the N-channel transistor, typically 1V.

Pericom's bus switches are low power devices with quiescent power supply current $I_{CC} = 3.0 \mu A$. Excellent for Green PC and notebook PC applications.

Pericom Semiconductor's bus switch products are available in three package types: 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and industry's new 150 mil wide plastic QSOP package. The pin-to-pin pitch of the SOIC package is 50 mil. The pin-to-pin pitch of the QSOP package is only 25 mil. As shown in Figure 4, SOIC saves 44% of board space as compared with plastic DIP. Amazingly, QSOP saves 81% of board space as compared with the plastic DIP.

The bus switch has many unique applications which cannot be easily implemented by other devices.

Figure 4. Package Comparison Board Space Requirements.



The resistance characteristic is shown in Figure 3. The voltage at point A or point B of Figure 1 is 1V, then most of Pericom Semiconductor's bus switches have only 2 to 3 ohm resistance. As the I/O voltage rises above 3V, at both points A and B of Figure 1, the switch resistance increases until the switch turns off at approximately 4V.

When the I/O voltages are below 3V, the voltages at A and B are identical, since they are connected by an equivalent resistor of less than 2 ohms. Note that the value of resistance is determined by the lower of the voltages on the two I/O pins (points A and B). When the input voltage at point A rises above 4V, the output voltage at point B does not follow the input voltage, but rises and maintains at $V_{CC} - V_T$, where V_{CC} is the supply voltage at pin 24 or pin 20, and V_T is the threshold voltage of the N-channel transistor, typically 1V.

Pericom's bus switches are low power devices with quiescent power supply current $I_{CC} = 3.0 \mu A$. Excellent for Green PC and notebook PC applications.

Pericom Semiconductor's bus switch products are available in three package types: 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and industry's new 120 mil wide plastic QSOP package. The pin-to-pin pitch of the SOIC package is 50 mil. The pin-to-pin pitch of the QSOP package is only 25 mil. As shown in Figure 4, SOIC saves 44% of board space as compared with plastic DIP. Amazingly, QSOP saves 81% of board space as compared with the plastic DIP.

The bus switch has many unique applications which cannot be easily implemented by other devices.

2. Bus Isolation and Multiplexing

The PI5C3245 and PI5C3861 CMOS bus switches are ideal for bus isolation application. A logic block diagram of the PI5C3245 is shown in Figure 5, which is pin compatible with 74 x 245 TTL transceiver. This device, when enabled, allows eight signals at bus A to be connected to eight signals at bus B. Since the corresponding bus signals are directly connected, the bus switch does not introduce propagation delay, timing skew, or noise, as compared with the traditional TTL 74F245 transceiver or 74F244 driver. The purpose of bus isolation may be zero delay bus multiplexing or bus loading reduction for isolating the loads which are not currently in use.

Figure 6 shows the application of bus load reduction. The microprocessor's output driver can drive only one bank of SRAMs. It cannot drive two banks simultaneously due to capacitive loading of memory arrays. By address decoding, only one bank is enabled at a time. Each data driver of each SRAM does not tie with other bank's SRAM. The driver loading is reduced and the bus switch transceiver does not have any propagation delay. As a result, the access time of SRAM array is reduced. This is an ideal application for a high-performance system.

Figure 5. PI5C3245, 8-Bit, 2-Port Bus Switch, or PI5C3384A, 10-bit, 2-Port Bus Switch for zero delay multiplexing.

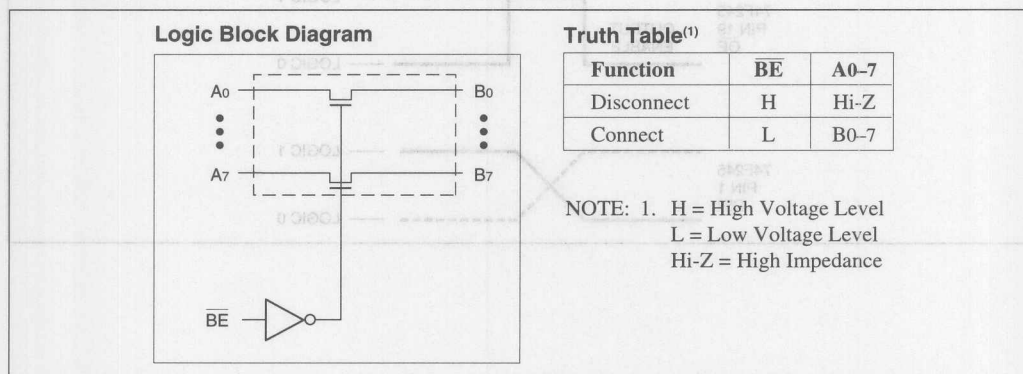
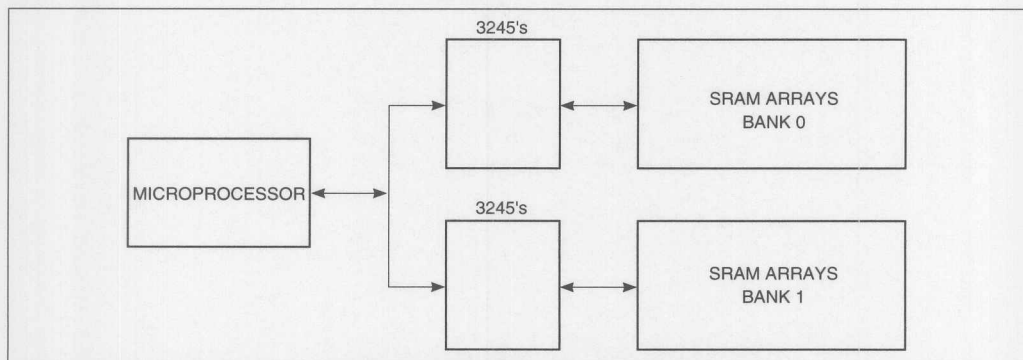


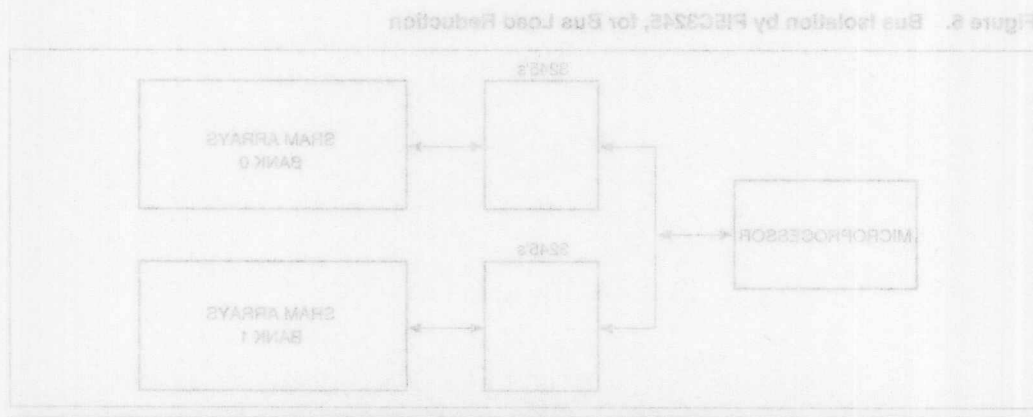
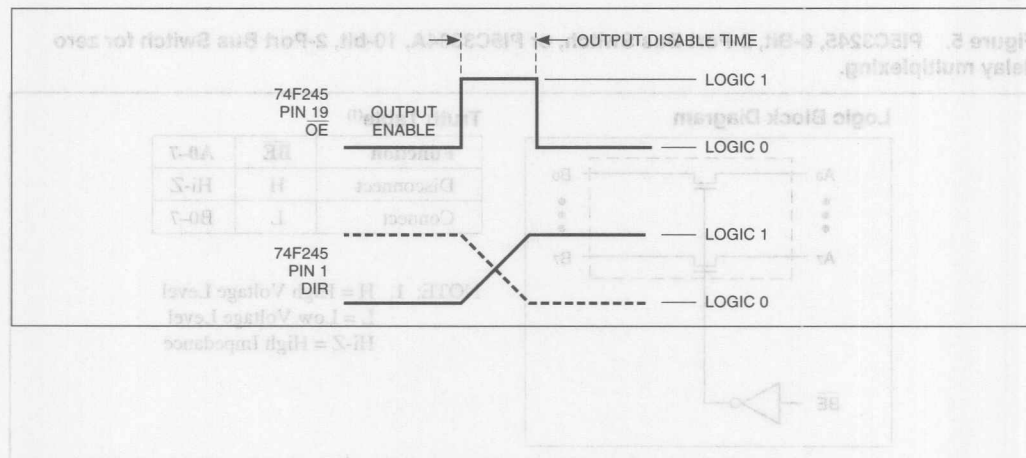
Figure 6. Bus Isolation by PI5C3245, for Bus Load Reduction



3. Zero Delay Bus Transceiver

Bus switches PI5C3245 and PI5C3861 can replace TTL transceivers 74F245/F861 in systems to eliminate the propagation delay of the transceiver. In this application, the driver driving the input pin of the bus switch can drive the output load at the output pin. Since the bus switch directly connects two buses, it provides no drive of its own but relies on the driver that is driving the input pin. The bus switch has an advantage over a TTL transceiver, in addition to zero delay benefit. The TTL transceivers require a complex timing of the direction signal to direct the data flow either from A bus to B bus or from B bus to A bus. In order to avoid a current glitch at the power/ground plane, the TTL transceiver's direction signal must remain unchanged while the transceiver is enabled, as shown in Figure 7. The direction signal may switch only during the window of time when a TTL transceiver is disabled. The bus switch does not require a direction signal. Therefore, bus switch does not need the logic circuit generating the appropriate direction signal and does not have the problem of ground glitch due to improper switching time of the direction signal.

Figure 7. Time Relationship Between OE and DIR of 74F245 Transceiver.



4. Conversion Between 5V Logic and 3V Logic

The existing popular Pentium chipsets are the Intel 82430 Mercury chipset and the Opti 82C596/82C597 chipset. These chipsets work well and the motherboards have been in volume production.

Recently, Intel announced a new 3V Pentium microprocessor. The P54C is clearly a winner due to much reduced power, and 100 MHz speed.

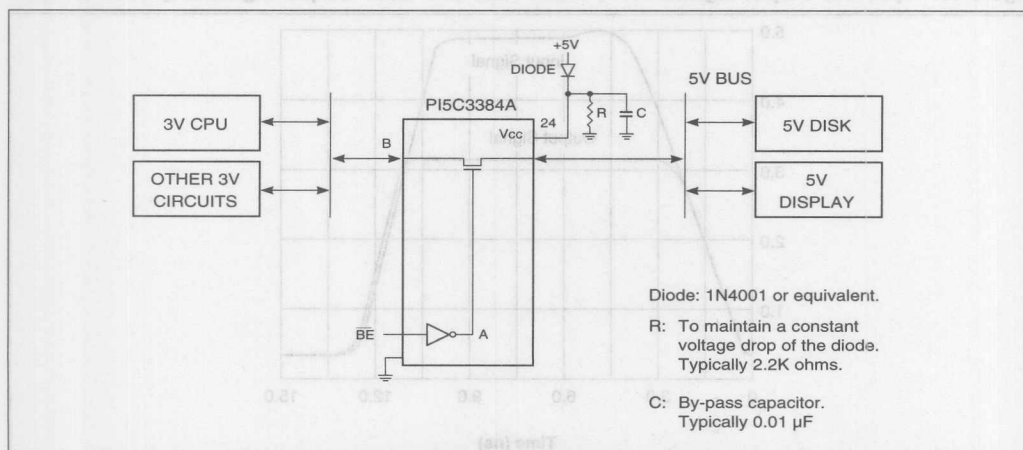
The key issue to the motherboard vendors is how to ship a clean 5V motherboard with the 3V P54C in large volume as soon as possible. The answer is clear:

Use Pericom 3384A bus switches to interface the P54C to the existing clean 5V motherboards.

Since the P54C is a 3V part and is not 5V tolerant, it cannot directly interface with any 5V parts on the motherboard such as the existing 5V support chipset, 5V DRAM/SRAM, 5V video/disk-drive/bus-interface, etc. Pericom's 3384A bus switch has been widely used to provide the 3V to 5V level shift function needed between P54C and any 5V parts on motherboards and other applications.

Battery operated computers, such as notebook computers, uses 3V TTL logic families for both high-speed and low power. Most systems have a mixture of 5V TTL and 3V TTL logic, for the reason that peripheral/peripheral controllers still need 5V TTL logic. The conversion between the two types is required to prevent damage to the 3V TTL even though their logic levels are compatible, since the 3V TTL often cannot tolerate any input voltage swing above 3.3V. To assure a proper interface between the two types, a bus switch can be used as shown in Figure 8. If the diode has 0.8V drop, the V_{cc} voltage is at 4.2V. The internal enabling signal at point A is 4.2V max. When signals B are connected to 3V TTL circuit from the 3384 bus switches, voltage will be 3.2V max, which will not cause any problem to 3V TTL circuit.

Figure 8. 5V TTL to 3V TTL Conversion.



In order to assume a reliable voltage drop across the diode, the circuit must consist of:

- (1) A diode which is capable of maintaining a constant voltage drop, such as 1N4001.
- (2) A resistor R to provide a constant forward current required by the diode. Missing this resistor can cause the diode voltage drop to become unpredictable, and cause intermittent failure problems. Some Pentium board design takes this unwise design risk. Any well designed Pentium motherboards always include the resistor. The typical value is 2.2K ohms.
- (3) A by-pass capacitor C to avoid any glitch at the Vcc pin, typically 0.01 μ F.

One of this diode circuit may provide the 4.2V Vcc to be shared by several bus switches, for cost savings.

Figure 9. On-Resistance RON of PI5C3384A Increases Only Slightly When Vcc Voltage Drops Below 5.0V, for TTL Signal Between 0V and 2.5V.

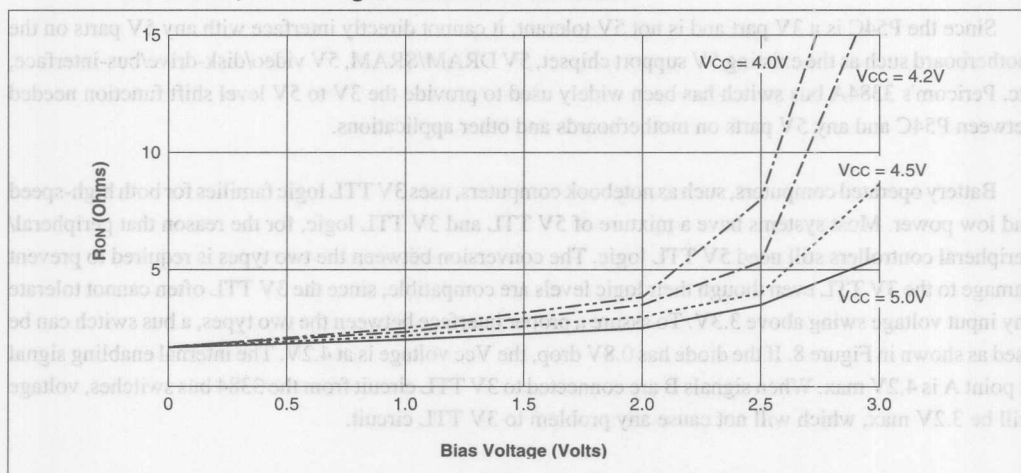
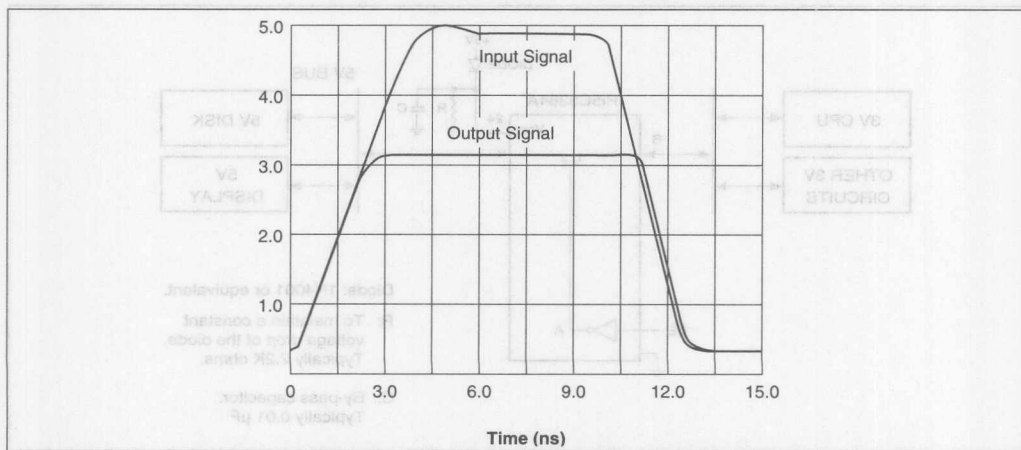


Figure 10. Input and Output Signals of PI5C3384A at Vcc = 4.2V. Output Signal Stays Below 3.3V.

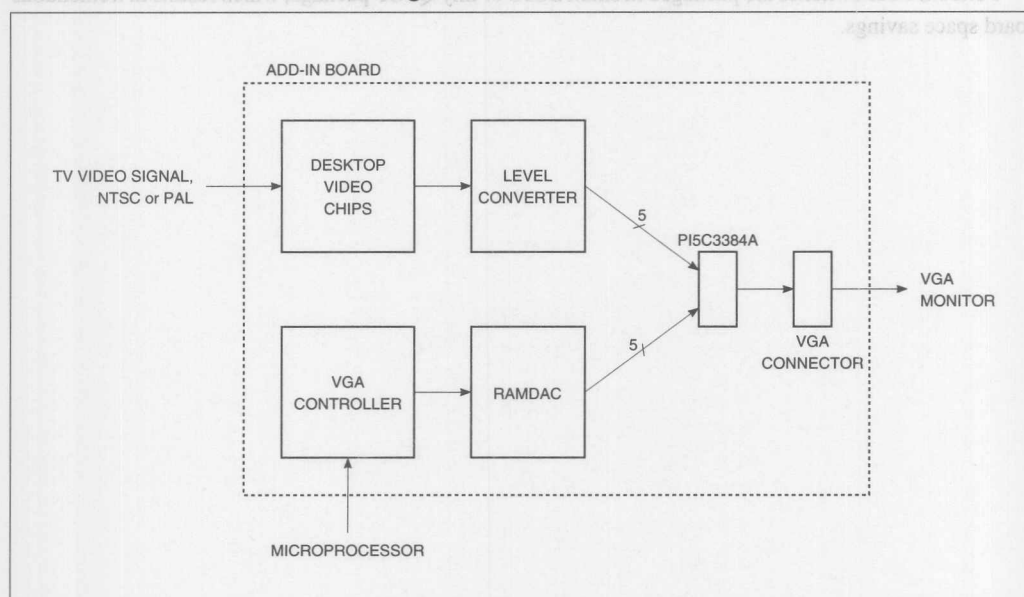


5. Multiplexing Analog Signals with Bus Switch

Bus switches is an ideal device to multiplex small analog signals. It offers many advantages over traditional analog switching devices. Bus switch has only 5 ohm resistance. Traditional analog switching devices have over 80 ohm to several hundred ohm resistance. The bus enable/disable time of bus switch is 10 to 100 time faster, as compared with the traditional analog switching devices.

In multimedia applications, for example, it is desired to multiplex video signals without any signal loss at multiplexing circuit. The VGA signals are 0V to 0.7V peak-to-peak. Bus switch is the best device for this application at low cost.

Figure 11. A Single Pericom's Bus Switch PI5C3384A Multiplexes the VGA Signals from VGA Controller and TV Video Signal.



12

Propagation Delay:

Pericom's Bus switches offer zero delay, since it adds less than 5 ohm resistance to the VGA signal propagation path. In contrast, a traditional analog switching device has 20 ns to over 50 ns propagation delay.

Enable/Disable Time:

Pericom's Bus Switches enable/disable a bus at 6.5 ns max. Since it is less than one VGA clock time period, it is very easy to be used as a VGA multiplex circuit. For comparison, a traditional analog switching device needs enable/disable time in the order of 50 ns to over 100 ns.

Crosstalk and Off-isolation:

Crosstalk measures the noise that couples from a switching signal to another signal at adjacent channels. Off-isolation measures the noise that couples from a switching signal to the output of an unused channel.

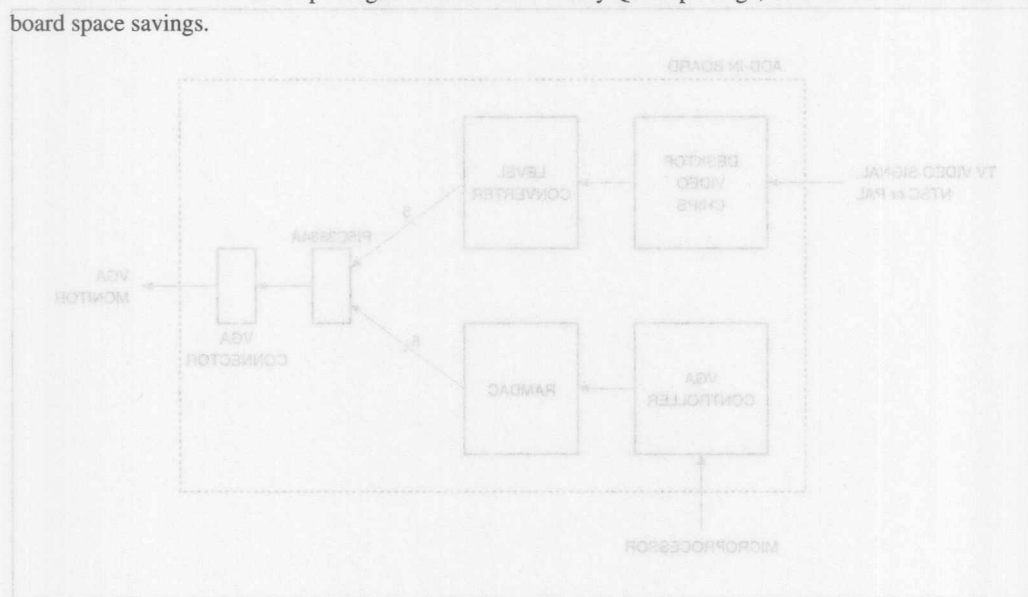
The noise level of crosstalk and off-isolation depends on circuit layout and circuit loading. For VGA applications, crosstalk and off-isolation of Pericom's bus switches are equivalent to traditional analog switching device.

Insertion Loss:

Insertion loss is the attenuation of an analog signal propagating from an input to an output of a bus switch. Since Pericom's bus switch resistance is very small, its insertion loss is very small for VGA applications.

Package:

Pericom's bus switches are packaged in small SOIC or tiny QSOP package, which results in tremendous board space savings.



Pericom's Bus switches offer zero delay, since it adds less than 5 ohm resistance to the VGA signal propagation path. In contrast, a traditional analog switching device has 20 ns to over 30 ns propagation delay.

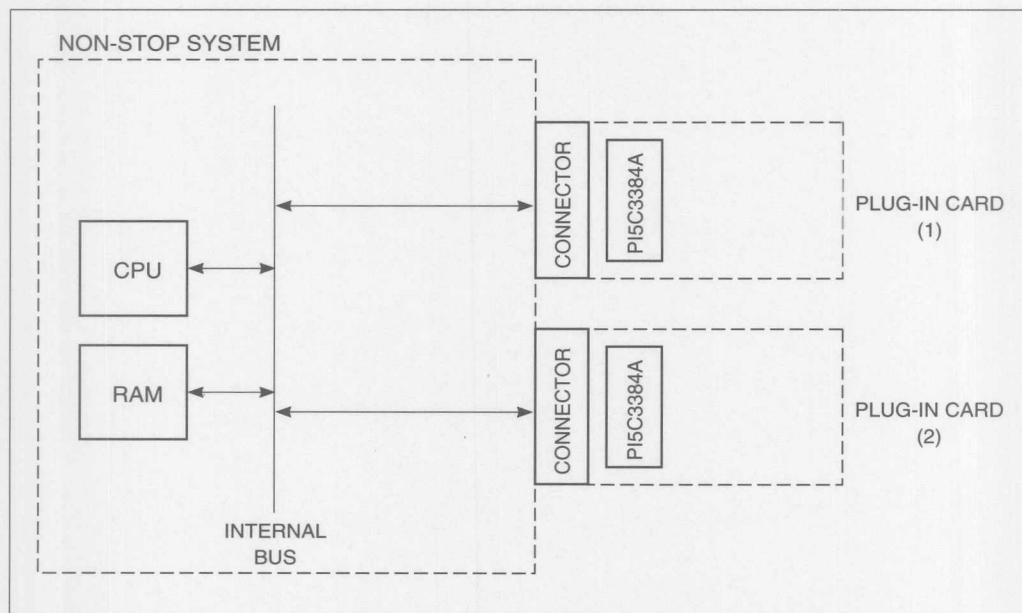
Pericom's Bus Switches enable/disable a bus at 6.5 ns max. Since it is less than one VGA clock time period, it is very easy to be used as a VGA multiplex circuit. For comparison, a traditional analog switching device needs enable/disable time in the order of 30 ns to over 100 ns.

6. Hot-Plug

Certain computer systems, such as airline reservations, manufacturing control, and telecommunication, cannot be regularly shut down for maintenance services or adding new hardware enhancement. These systems must allow installation/removal of hardware without turning off power. Hot-plug means the ability to replace a plug-in board in a system while the system power is fully active. When a board is plugged in, it must not disturb the operation of the system, even though it initially has no power. Bus switch is useful to entirely isolate the connector of the plug-in board from the bus until the bus switch is enabled by the system.

Figure 12 shows the application. The CPU must run all the time, even for the purpose of adding new hardware or repair service. The PI5C3384's isolate the bus completely when disabled. Adding a plug-in board or removing a plug-in board will not disturb the CPU operation while the bus switches are disabled.

Figure 12. Hot-Plug System.

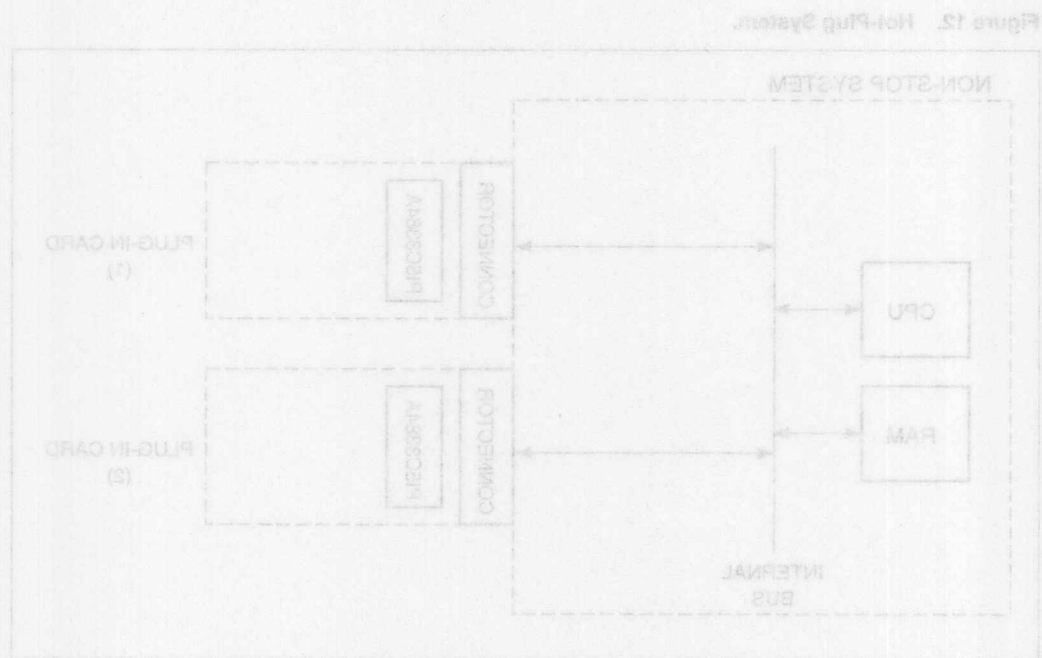


Staggered Pin Arrangement for an edge connector:

A staggered edge connector arrangement can be adopted that will provide control of an output enable pin (\overline{OE}) to ensure high impedance on the backplane. It will satisfy both insert and removal requirements. By offsetting the \overline{OE} pin, \overline{OE} , driven by the backplane, will reach a high level before VCC is applied or \overline{OE} remains at a high level during VCC ramp.

Pericom's bus switch devices offer the features required by hot plug application. During the process of plugging in the card, all signal pins at bus interface remain floating, when VCC is not connected. See Figure 2, "Staggered" Finger Arrangement for Hot Plug Applications in Application Note 5.

Figure 12 shows a staggered edge connector arrangement for hot plug applications. The P15C3381 isolates the bus completely when disabled. Adding a plug-in board or removing a plug-in board will not disturb the CPU operation while the bus switches are disabled.



7. Bus Exchange for Shared Memory

Figure 14 shows the logic diagram of the PI5C3383 CMOS 5-Bit, 4-Port Bus Switch designed with a low ON-resistance. When the exchange control BX is low and \overline{BE} is active, A-bus is directly connected with C-bus while B-bus is directly connected with D-bus. When the exchange control BX is high, A-bus is connected with D-bus while B-bus is connected with C-bus. This exchange configuration allows bit swapping of buses in systems. Figure 15 shows Host CPU and DSP CPU exchange Memory A and Memory B. Note that in this configuration, Host CPU and DSP CPU are allowed to access Memory A and Memory B simultaneously, for high-performance system application. A typical DMA configuration does not allow such a simultaneous memory access operation. A bus switch has many benefits over TTL transceivers: a bus switch does not incur a propagation delay, and does not require generation of a direction signal.

Figure 14. PI5C3383, 5-Bit, 4-Port Bus Switch.

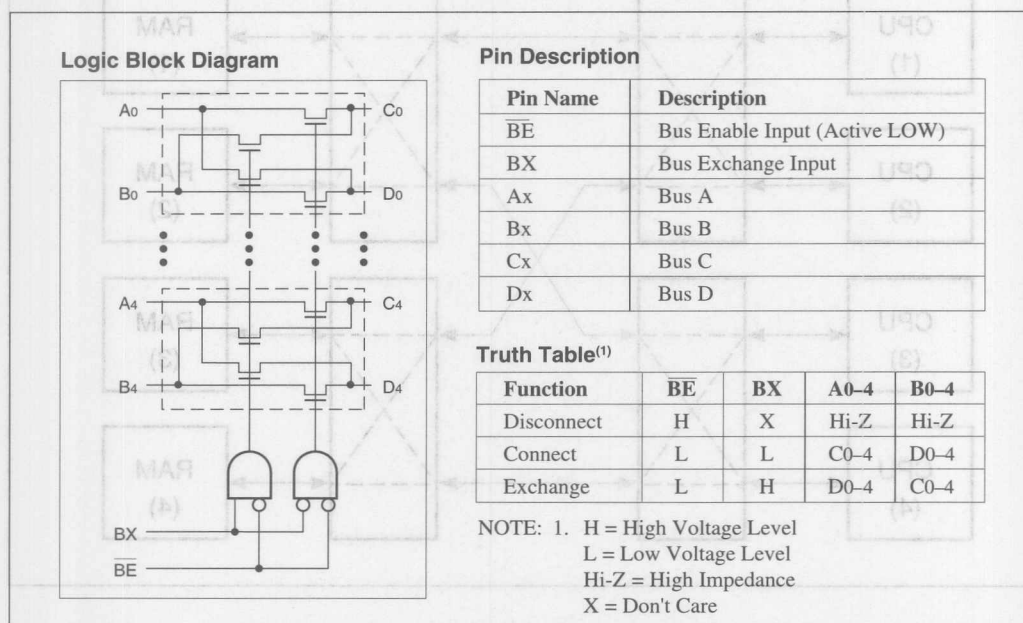
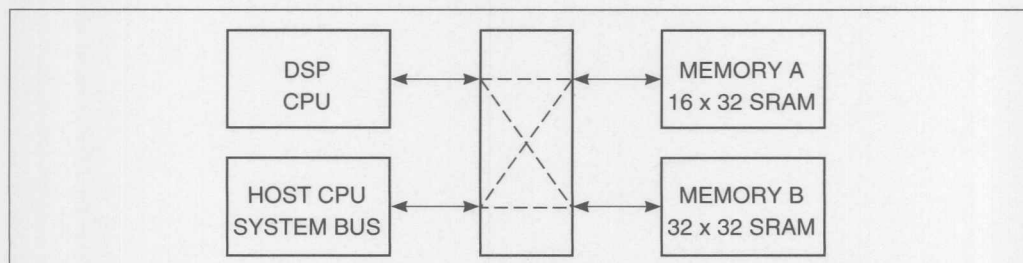


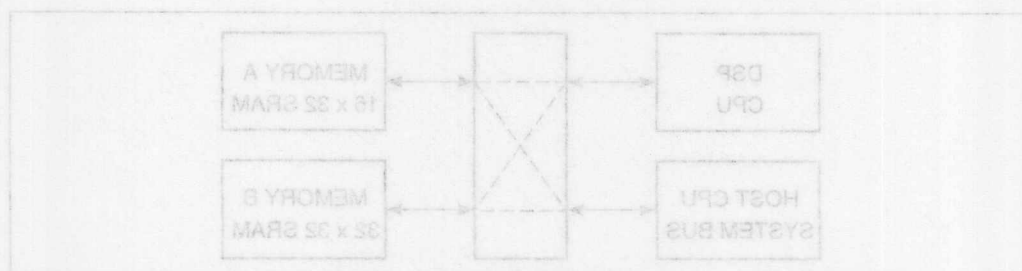
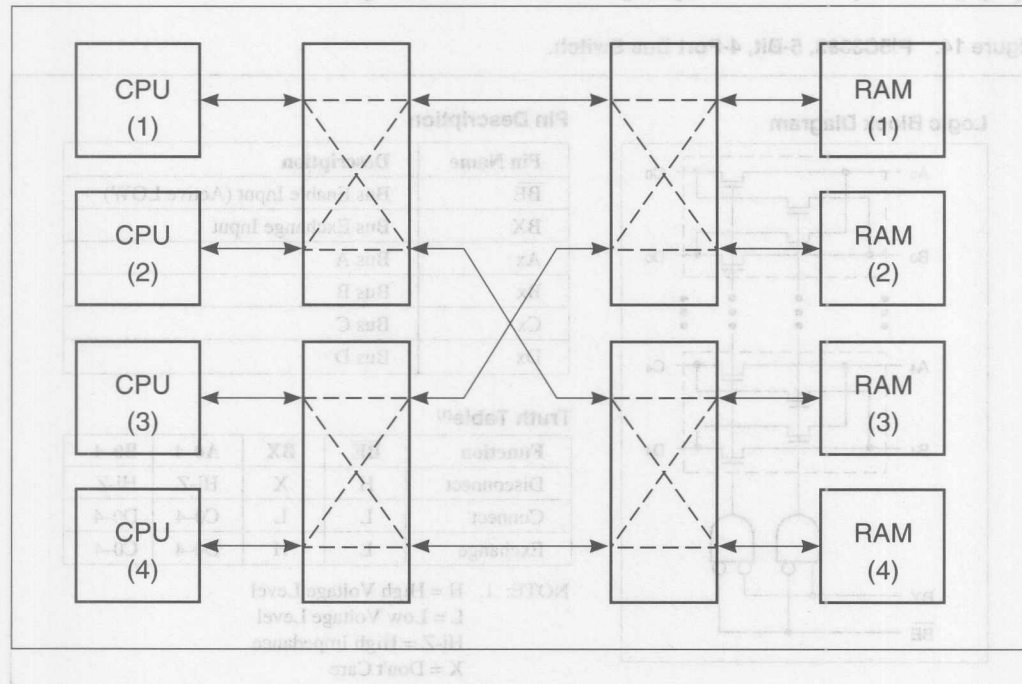
Figure 15. Bus Exchange for Share and Memory.



8. Bus Exchange for Crossbar Systems

Figure 16 shows the 3383 bus exchange switch used to connect four CPUs and four memories in a crossbar configuration, where any CPU can be connected to any memory. The 3383 bus exchange switch is ideal for crossbar work because it introduces no delay of its own. The CPU sees a simple RAM interface. If traditional bus transceivers are used, the multiple stages of bus switching require long propagation delays which will result in a complicated timing skew problem. Using bus switches eliminates the need of a complex logic circuit to generate the direction signals at a proper time.

Figure 16. Crossbar Switch Between Four CPUs and Four RAMs.



9. Data Byte Swap in Hardware

The bus switch PI5C3245, PI5C3384A or PI5C3400 can also be used to provide byte swapping capability between a CPU and memory. Bus swap in hardware is extremely useful in systems where Big Endian and Little Endian byte orders are mixed within the same system. Figure 17 shows the Big and Little Endian memory formats and Figure 18 illustrates a conversion between the two memory formats.

Figure 17. Big vs Little Endian Memory Format.

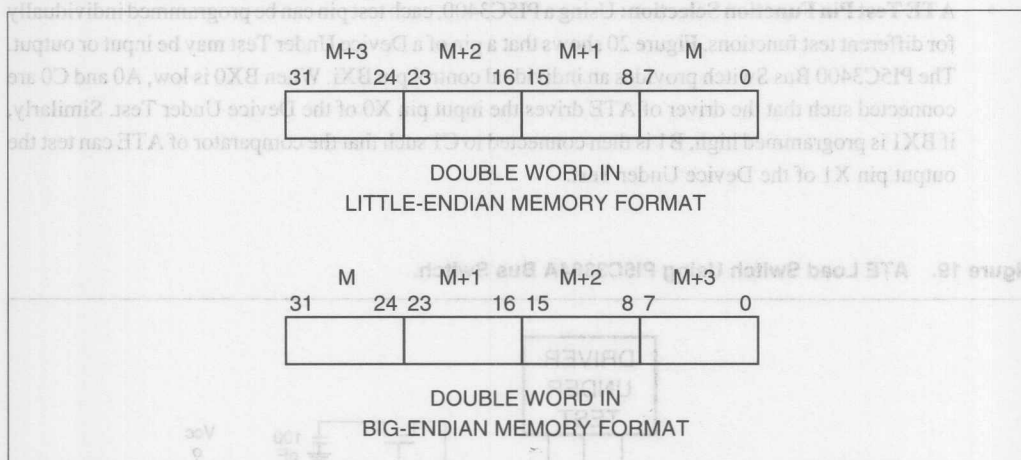
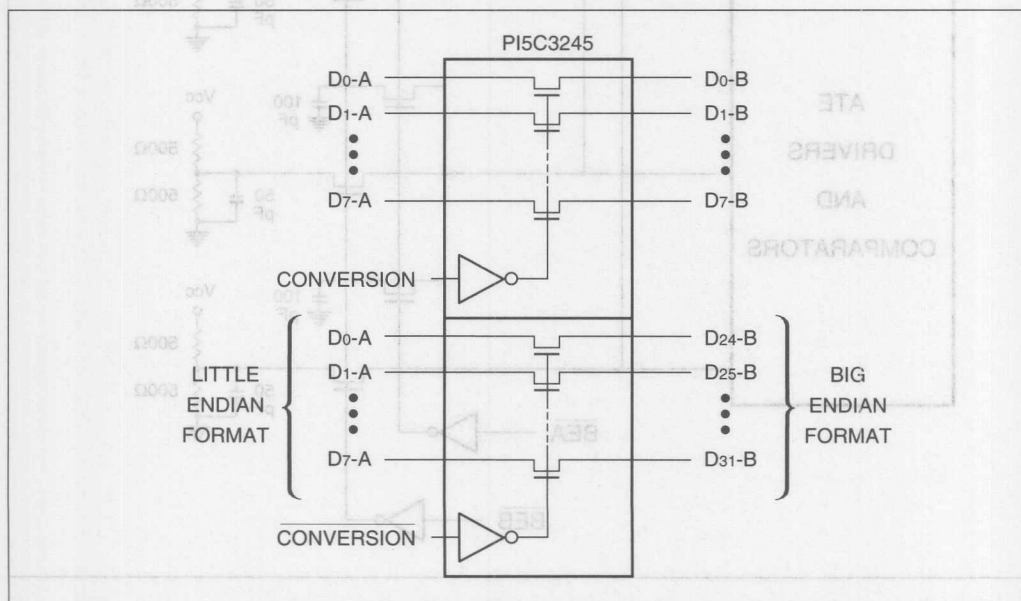


Figure 18. Conversion Between Little Endian and Big Endian Format.



10. Test Load/Driver or Test Channel Selection

Bus Switch is an ideal selection circuit for automatic test equipment, since it contributes no added load.

- **ATE Load/Driver Switch:** Automated test equipment needs to test an output driver of a Device Under Test for different test loads. Bus switch allows the tester to switch to a new test load and isolate the old test load for an output pin (see Figure 19). Bus switch also allows a tester to select a different driver to drive an input pin.

- **ATE Test Pin Function Selection:** Using a PI5C3400, each test pin can be programmed individually for different test functions. Figure 20 shows that a pin of a Device Under Test may be input or output. The PI5C3400 Bus Switch provides an individual control pin BXi. When BX0 is low, A0 and C0 are connected such that the driver of ATE drives the input pin X0 of the Device Under Test. Similarly, if BX1 is programmed high, B1 is then connected to C1 such that the comparator of ATE can test the output pin X1 of the Device Under Test.

Figure 19. ATE Load Switch Using PI5C3384A Bus Switch.

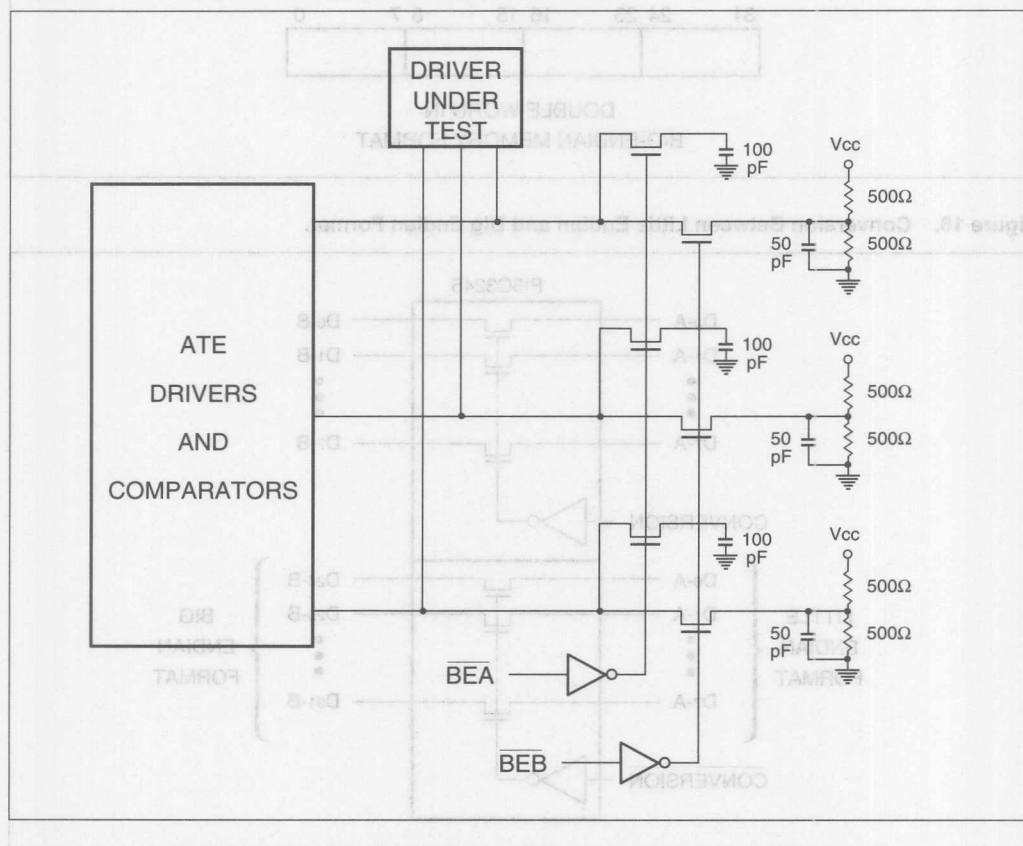
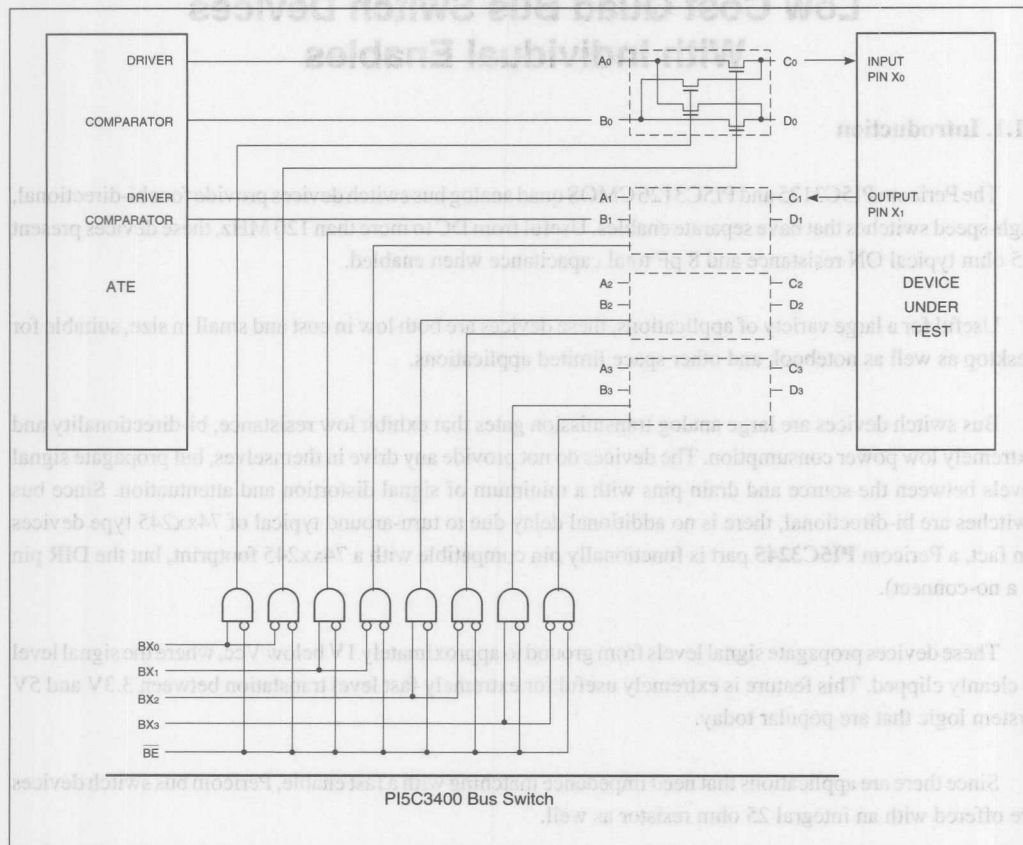


Figure 20. Test Pin Selection Under Individual Control.



Low Cost Quad Bus Switch Devices With Individual Enables

11.1. Introduction

The Pericom PI5C3125 and PI5C3126 CMOS quad analog bus switch devices provide four bi-directional, high-speed switches that have separate enables. Useful from DC to more than 120 MHz, these devices present a 5 ohm typical ON resistance and 8 pF total capacitance when enabled.

Useful for a large variety of applications, these devices are both low in cost and small in size, suitable for desktop as well as notebook and other space limited applications.

Bus switch devices are large analog transmission gates that exhibit low resistance, bi-directionality and extremely low power consumption. The devices do not provide any drive in themselves, but propagate signal levels between the source and drain pins with a minimum of signal distortion and attenuation. Since bus switches are bi-directional, there is no additional delay due to turn-around typical of 74xx245 type devices (in fact, a Pericom **PI5C3245** part is functionally pin compatible with a 74xx245 footprint, but the DIR pin is a no-connect).

These devices propagate signal levels from ground to approximately 1V below Vcc, where the signal level is cleanly clipped. This feature is extremely useful for extremely fast level translation between 3.3V and 5V system logic that are popular today.

Since there are applications that need impedance matching with a fast enable, Pericom bus switch devices are offered with an integral 25 ohm resistor as well.

11.2. Applications

Following is a list of applications that bus switch devices are useful. Additional information about bus switch devices and typical applications are available in the application section of the Pericom Data Book.

1. Fast in-line signal enable/disable without introducing additional propagation delay.
2. Fast signal multiplexing with a minimum of waveform distortion.
3. Pull up and pull down (up to 100 mA), can be used in pairs for cable driving
4. Replace manual jumpers on motherboards (pull-up, pull-down, and signal enable/disable) and use one dip switch or hex switch to select user configurations.

5. **Load isolation:** several parallel banks of load can be isolated by bus switches so that the controller sees only one bank at a time, and the bank sees only the controller. This is particularly useful for DRAM memory applications, where the capacitance of several banks of DRAM can force additional wait-states.
6. **Fast Local Bus Ready control:** Peripheral controller cards that reside on a local processor bus (almost any architecture) need to pass or control handshake lines. In situations where the particular controller card is not being addressed, these critical control signals need to be passed on as quickly and as cleanly as possible, or the system will start introducing additional undesirable wait states. The Pericom PI5C3125 (or PI5C3126 for active high enables) can be placed near the connector and used to bypass the control signal (like the LRDY# of the VESA bus) around the normal control logic if the card is not actually being addressed.
7. **Signal blanking applications:** In situations where a signal needs to be suppressed during a critical interval, or where unnecessary clock data need to be removed from a data stream, the PI5C3125/PI5C3126 can be used as a fast signal flow controller. One typical application is the data from CCD arrays, where clock and data are gated together. Once the clock is recovered from the data stream, the clock can then be used to blank the clock information in the data stream.
8. Applications that already use the 74xx125/126 parts that can benefit from a faster enable/disable time.
9. Small multiplex/demultiplex applications that need to be local to a particular part of the design. The 3125/3126 has four separate bi-directional gates with individual enables. Joining inputs and/or outputs together, custom mux/demux designs can be built efficiently. Requirements that need decoded enable/control signals can use the Pericom 3251/3253/3257 for mux/demux applications and the Pericom 3383/3400/3401 devices for switch matrix applications. Since the bus switch is inherently bi-directional, there is no direction control necessary.

Another multiplexer application that is particularly useful is on the VESA Video feature connector that allows a second device (video capture/playback for example) to gain access to the VGA connector. The bus switch provides an ideal solution for this application since the bus switch will not introduce any additional waveform distortion or signal-to-signal skew.

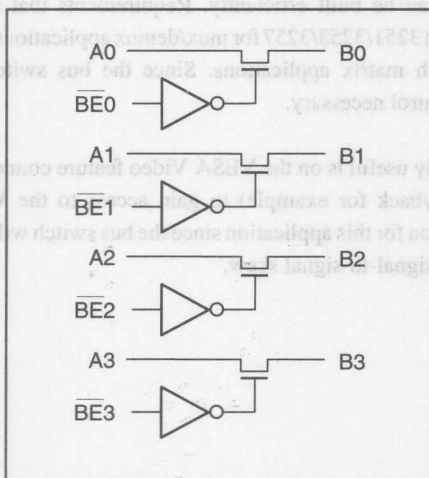


10. **Hot Plug and Hot Swap isolation:** Pericom bus switch devices exhibit extremely low leakage (less than 0.2 μA typical when disabled and/or when power is off). Since these gates are designed without "P" channel devices (which can cause latch-up) and do not have a diode clamp to Vcc, there is no leakage path when power is off and the signal level is above ground. Internal clamp diodes from signal to ground prevent false enable effects due to signal undershoot, up to better than 1V below ground level. As a result, the impact of a hot plug-in on a live circuit is minimized to the stray capacitance of the device and the layout. Good hot-plug module designs can minimize accidental pre-enables by carefully managing the connect pin strategy (ground then control then Vcc) as well as using pull-ups on active low enables (and pull-downs on active high enables).

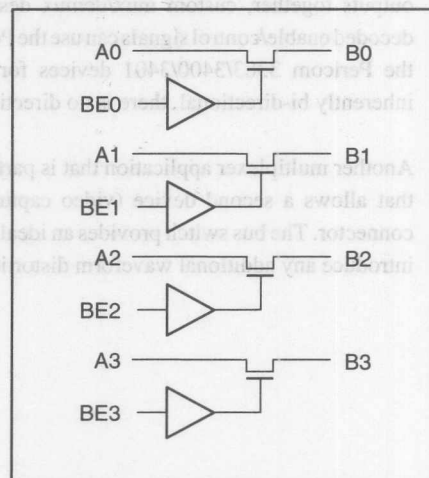
11.3 Product Features:

- Near zero propagation delay (250 ps typically)
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- Fast Individual Enable (6 ns typical)
- Ultra Low Quiescent Power (0.2 μA Typical)
- Familiar 74xx125/126 footprint
- Packaged in 14-pin 150 mil SOIC, 14-pin 300 mil PDIP or "1/4 size" 16-pin surface mount QSOP
- Quiescent power, package size and features are ideally suited for notebook applications

PI5C3125 Block Diagram



PI5C3126 Block Diagram



11.4 Product Description:

Pericom Semiconductor's PI5C series of logic circuits are produced using the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI5C3125 and PI5C3126 devices have four individual 5 ohm bus switches with fast individual enables in an industry standard 74xx125/126 pinout. When enabled via the associated bus enable (\overline{BE}) pin, the "A" pin is directly connected to the "B" pin for that particular gate. The bus switch introduces virtually no additional propagation delay or additional ground bounce noise.

The PI5C3125 part has active low enables, and the PI5C3126 has active high enables.

Quad Analog Switch with Individual Enables

Product Pin Description

Pin Name	Description
\overline{BE}	Switch Enable (PI5C3125)
BE	Switch Enable (PI5C3126)
A3-A0	Bus A
B3-B0	Bus B
Vcc	Power
GND	Ground

Truth Table⁽¹⁾

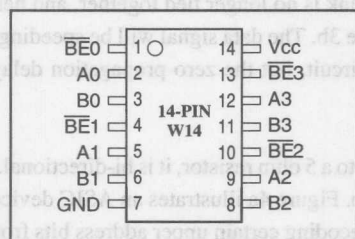
PI5C3125 \overline{BE}	PI5C3126 BE	A _n	B _n	Vcc	Function
X*	X	Hi-Z	Hi-Z	GND	Disconnect
H	L	Hi-Z	Hi-Z	Vcc	Disconnect
L	H	B _n	A _n	Vcc	Connect

Notes:

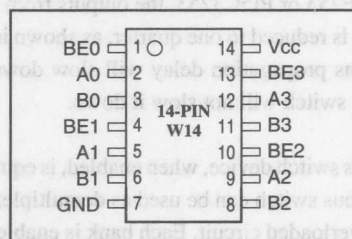
1. H = High Voltage Level, L = Low Voltage Level
Hi-Z = High Impedance, X = Don't Care

* A pull-up resistor should be provided for power-up protection.

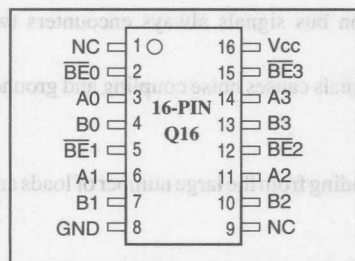
PI5C3125 14-Pin Product Configuration



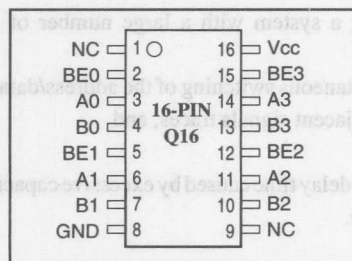
PI5C3126 14-Pin Product Configuration



PI5C3125 16-Pin Product Configuration



PI5C3126 16-Pin Product Configuration



Section 12: Bus Switches as MULTIPLEXER/DEMULPLEXER

Pericom offers three bus switch multiplexer/demultiplexers:

PI5C3251	8:1 multiplexer/demultiplexer
PI5C3253	Dual 4:1 multiplexer/demultiplexer
PI5C3257	Qual 2:1 multiplexer/demultiplexer,

which are functionally pin-compatible with F-series multiplexers F251, F253, and F257, respectively.

Recall that a bus switch device in Figure 1, when enabled, is equivalent to a 5 ohm resistor. The advantage of bus switch device over F-series multiplexer is that a bus switch device has nearly zero propagation delay. This is an ideal circuit for a system design, assuming that the output "A" providing the input signal to the bus switch device input "IN" can also drive the output load "L" of the bus switch device.

Figure 2 shows a 4:1 multiplexer PI5C3253. The selection signals S0 and S1 determine which one of the four input signals is connected to the output. This is exactly identical to the function of F253 multiplexer. Their pinouts are also identical.

Figure 3a shows a 4-bank circuit, whose outputs are tied together to produce one data bit signal. Only one bank is enabled at one time. The output load is excessive and causes a slow down in throughput speed. Using a multiplexer F253 or PI5C3253, the outputs from each bank is no longer tied together, and hence the load of each output is reduced to one quarter, as shown in Figure 3b. The data signal will be speeding up. If F253 is used, its 8 ns propagation delay will slow down the circuit, but the zero propagation delay feature of PI5C3253 bus switch will not slow it down.

Since a bus switch device, when enabled, is equivalent to a 5 ohm resistor, it is bi-directional. As a result, a multiplexer bus switch can be used as demultiplexer also. Figure 4a illustrates an ASIC device driving an excessively overloaded circuit. Each bank is enabled by decoding certain upper address bits from the ASIC and only one bank is enabled at one time. Figure 4b shows that the output A is now driving only two banks at one time, reducing the output loading to one half.

Designing a system with a large number of common bus signals always encounters two common problems:

1. Simultaneous switching of the address/data bus signals causes noise coupling and ground bounce on the adjacent signals traces, and
2. Large delay time caused by excessive capacitive loading from the large number of loads and long trace length.

The Pericom PI6C3xxx bus switch devices are ideal for solving this type of system problems. This is due to its excellent features of zero propagation delay, zero ground bounce, and low connection resistance, 5 ohms, between an input pin and its output pin.

Figure 5a illustrates a large memory of eight banks, in which each address signal and each data signal are excessively loaded. Figure 5b shows the memory circuit can be improved by using bus switch as both demultiplexer and multiplexer. PI6C3257 bus switch is used as a 2:1 demultiplexer to reduce the output load of the memory address bit MA0 to one half. PI6C3251 bus switch is used as a 8:1 multiplexer for a data bit D0 to reduce the output load of each D0-x to one-eighth. A significant performance increase and noise reduction can be achieved, by the bus switch as demultiplexer and multiplexer, plus the zero propagation delay feature of the bus switch.

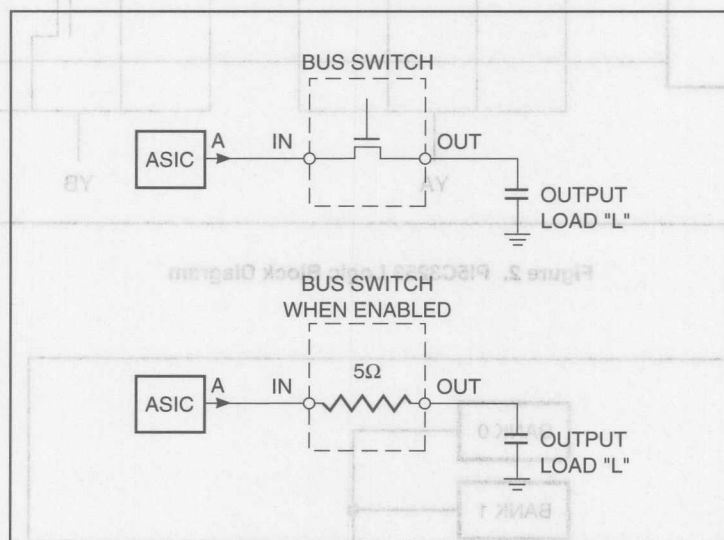


Figure 1. Equivalent Circuit of a Bus Switch

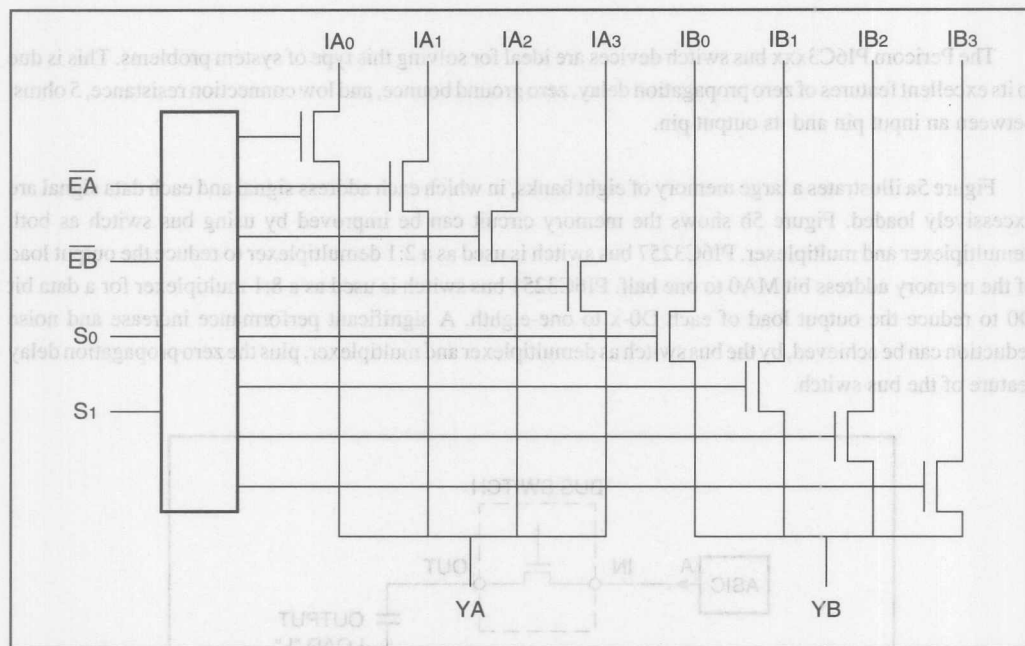


Figure 2. PI5C3253 Logic Block Diagram

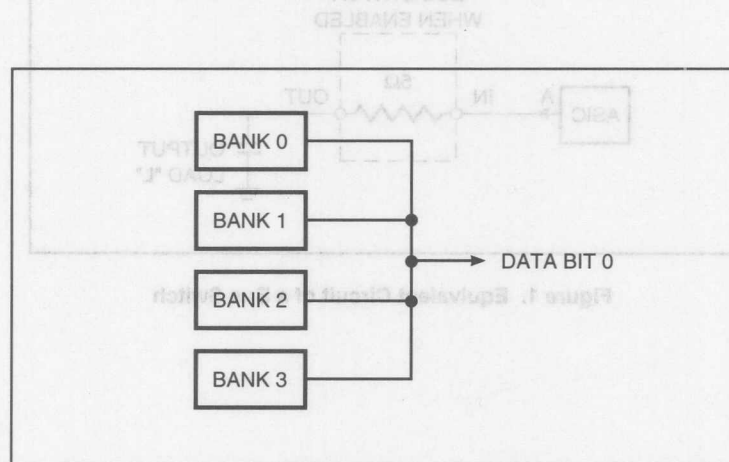


Figure 3a. Overloaded Data Bit

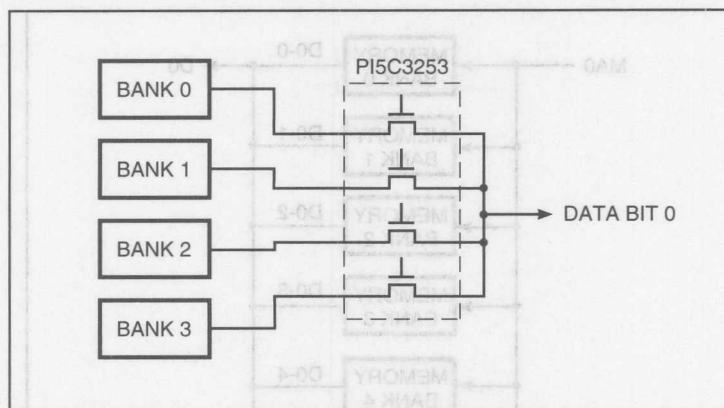


Figure 3b. Use PI5C3253 as a Multiplexer to Reduce Output Load and Increase Performance

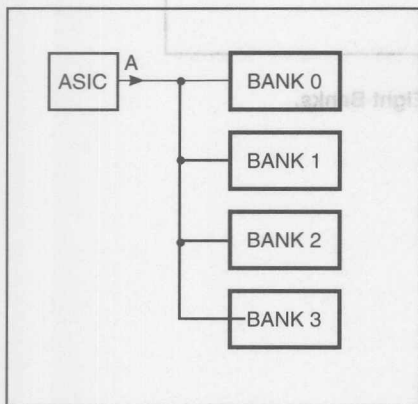


Figure 4a. The ASIC Output A is Heavily Loaded by Four Banks of Circuits.

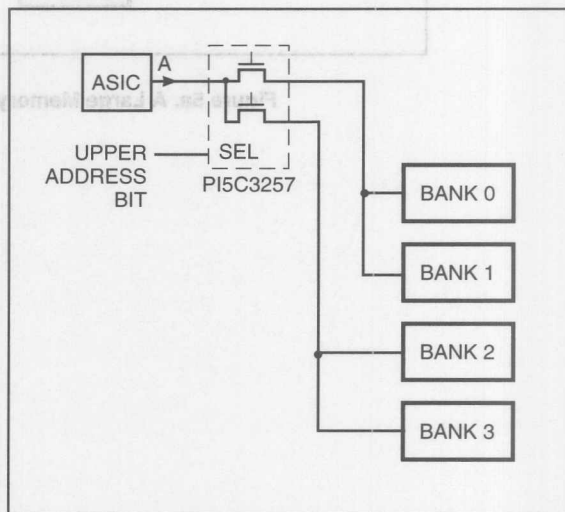


Figure 4b. Use PI5C3257 as a Demultiplexer to Reduce Output Load and Increase Performance.

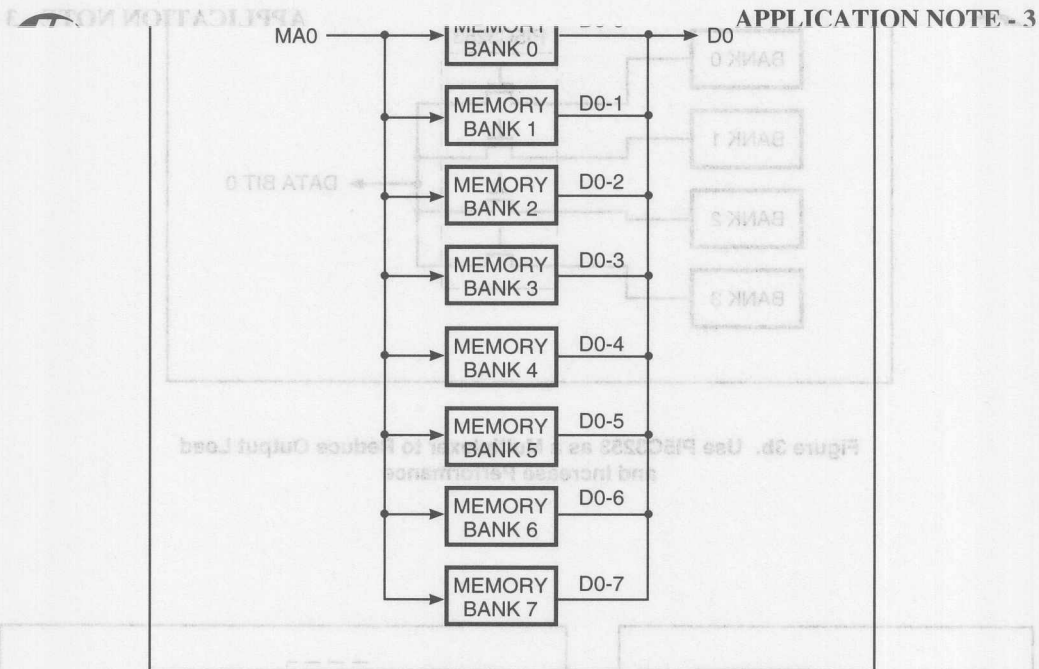


Figure 5a. A Large Memory of Eight Banks.

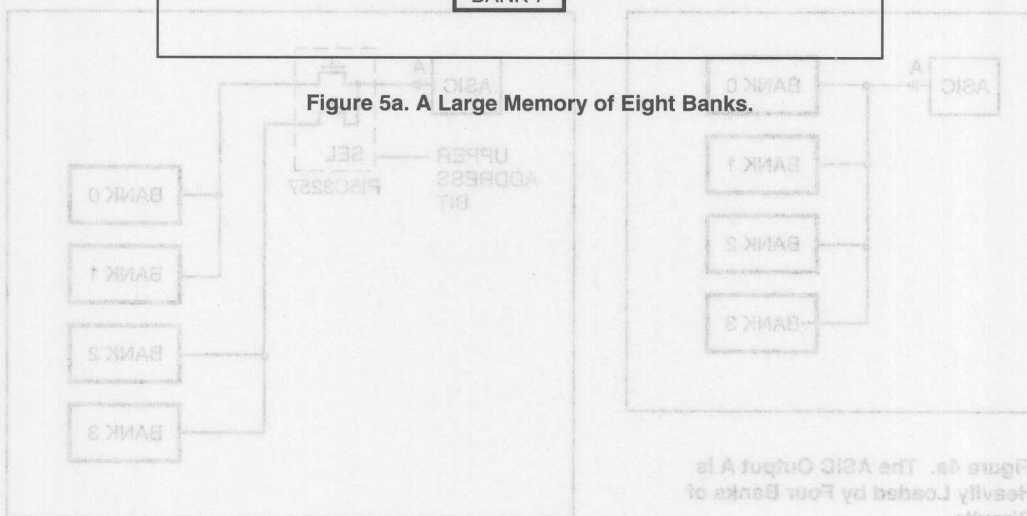


Figure 4b. Use PISC3257 as a Demultiplexer to Reduce Output Load and Increase Performance.

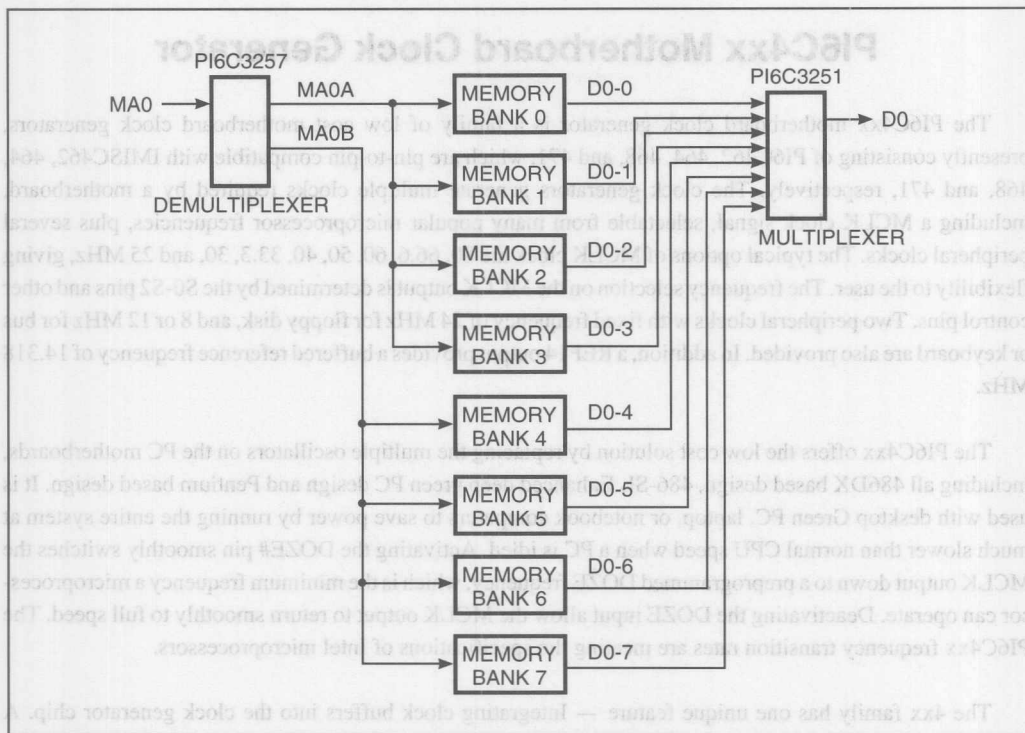


Figure 5b. A Large Memory of Eight Banks, Improved by Bus Switch Demultiplexer and Multiplexer.

PI6C4xx Motherboard Clock Generator

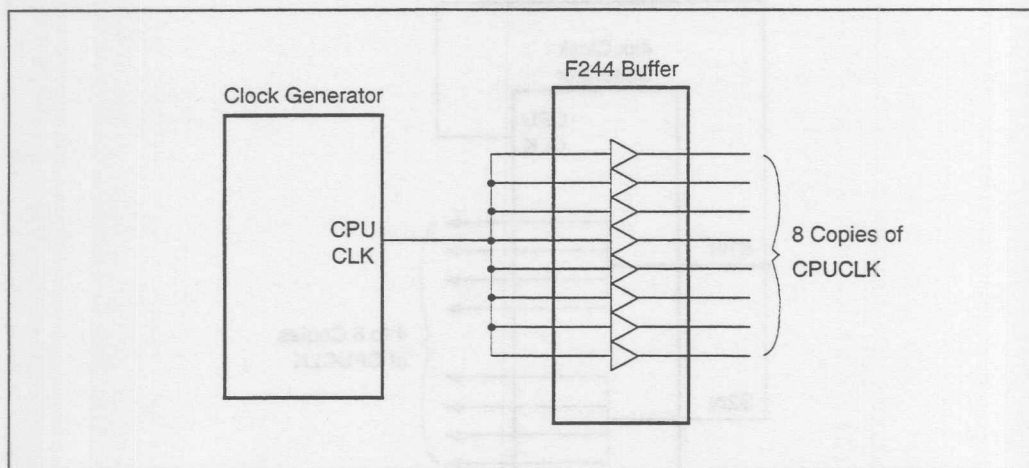
The PI6C4xx motherboard clock generator is a family of low cost motherboard clock generators, presently consisting of PI6C462, 464, 468, and 471, which are pin-to-pin compatible with IMISC462, 464, 468, and 471, respectively. The clock generators generate multiple clocks required by a motherboard, including a MCLK clock signal, selectable from many popular microprocessor frequencies, plus several peripheral clocks. The typical options of MCLK clock are 80, 66.6, 60, 50, 40, 33.3, 30, and 25 MHz, giving flexibility to the user. The frequency selection on the MCLK output is determined by the S0-S2 pins and other control pins. Two peripheral clocks with fixed frequency of 24 MHz for floppy disk, and 8 or 12 MHz for bus or keyboard are also provided. In addition, a REF14 output provides a buffered reference frequency of 14.318 MHz.

The PI6C4xx offers the low cost solution by replacing the multiple oscillators on the PC motherboards, including all 486DX based design, 486-SL Enhanced deep green PC design and Pentium based design. It is used with desktop Green PC, laptop, or notebook computers to save power by running the entire system at much slower than normal CPU speed when a PC is idled. Activating the DOZE# pin smoothly switches the MCLK output down to a preprogrammed DOZE frequency, which is the minimum frequency a microprocessor can operate. Deactivating the DOZE input allow the MCLK output to return smoothly to full speed. The PI6C4xx frequency transition rates are meeting the specifications of Intel microprocessors.

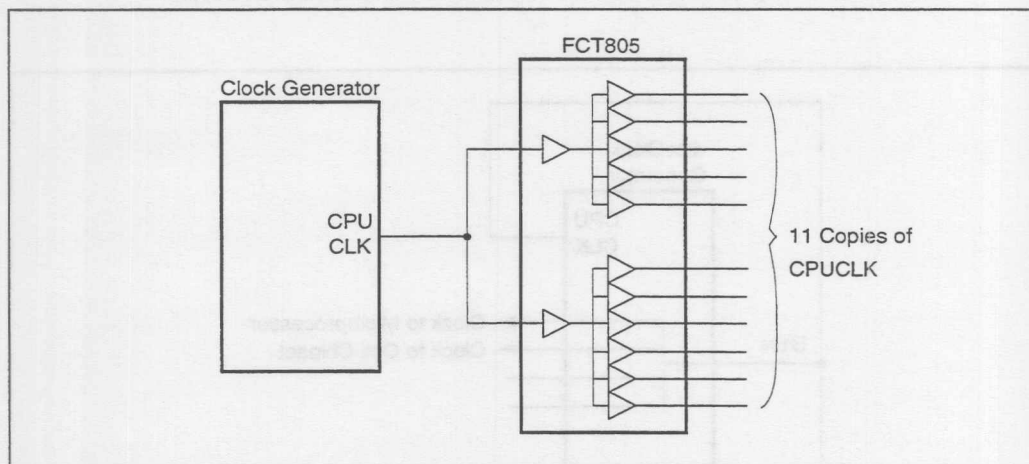
The 4xx family has one unique feature — Integrating clock buffers into the clock generator chip. A motherboard requires several copies of the CPU clock signals — one CPU clock to drive each microprocessor, one or more CPU clocks to drive the chipset. A PCI bus-based motherboard needs a clock buffer driver to provide an individual CPU clock, or 1/2 CPU clock, for each bus connector. In other words, a CPU clock signal from a clock driver output cannot drive more than one PCI bus connector. Figure 1 shows a clock circuit, using low cost F244, to generate the clock signals. This circuit has two obvious problems. First, the skew among the eight clock outputs are too large. Secondly, the input clock signal drives eight input pins — a heavy load to slow down the rise and fall times of the clock input, resulting in undesirable clock duty cycle.

The skew time among all the CPU clock signals must be much tighter than 0.9 ns for most cases. Figure 2 shows a clock circuit, using a low skew clock buffer FCT805 for high end product. The skew among the clock outputs can be 0.5 ns max.

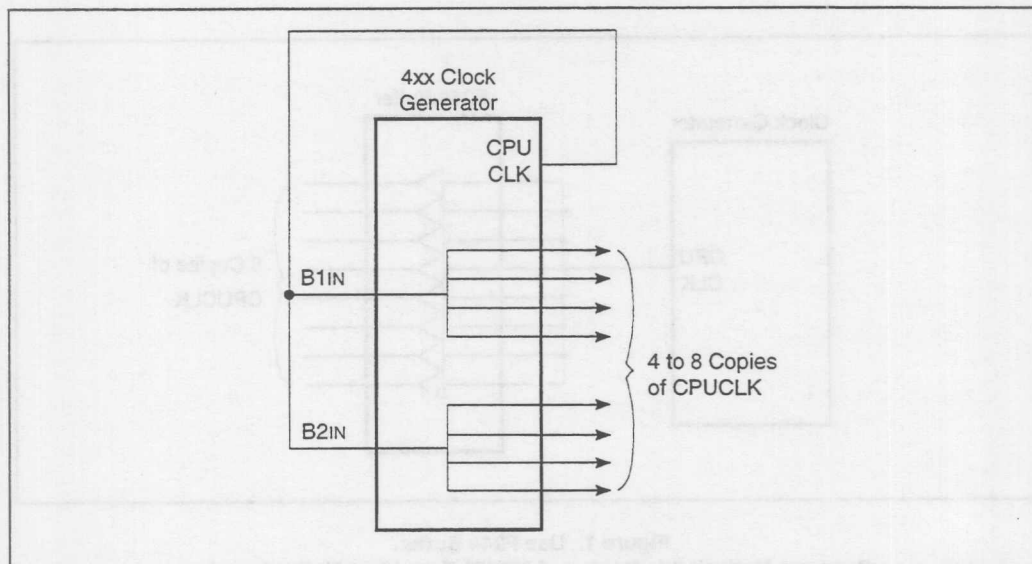
The 4xx family offers a low cost solution to attain a desired tight skew among the clock outputs. Figure 3 describes the block diagram connection. Figures 4 and 5 show the typical connection for Opti and SIS chipset based design. Figure 6 describes the Xtal and digital/analog power ground connections. Use short traces to connect the crystal to the Xtal pins. Connect the analog ground AGND to the digital ground DGND at one single point. It is a good practice to use 15 - 33 ohm series resistor for each clock output, to reduce clock signal reflection.



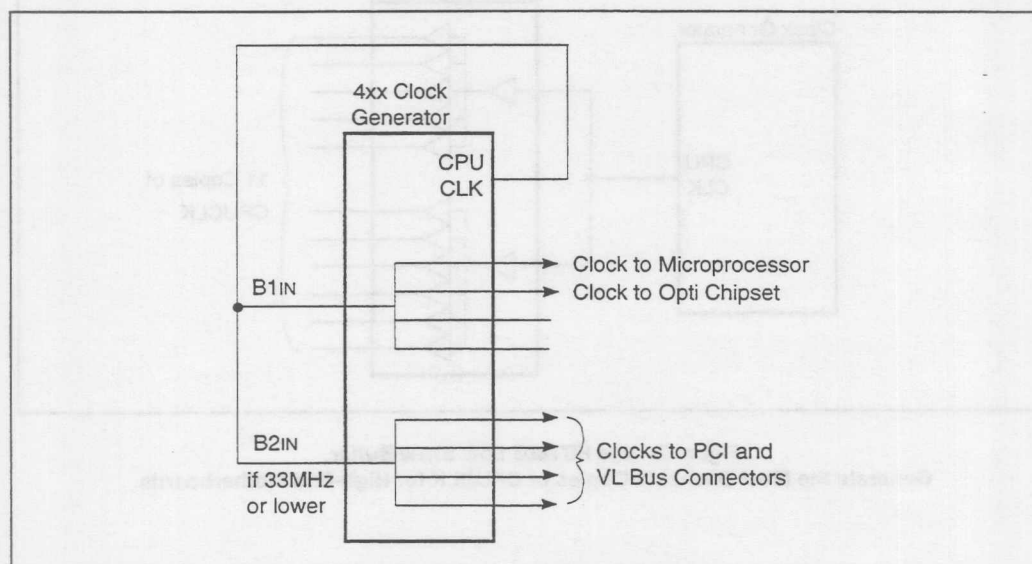
**Figure 1. Use F244 Buffer.
Generate Undesirable Copies of CPUCLK for Most Motherboards.**



**Figure 2. Use FCT805 Low Skew Buffer.
Generate the Most Desirable Copies of CPUCLK for High-End Motherboards.**



**Figure 3. Use 4XX Clock Generator.
Generate Copies of CPUCLK Without an External Clock Buffer Device.**



**Figure 4. Use 4XX Clock Generator
on Opti Chipset Based Motherboards**

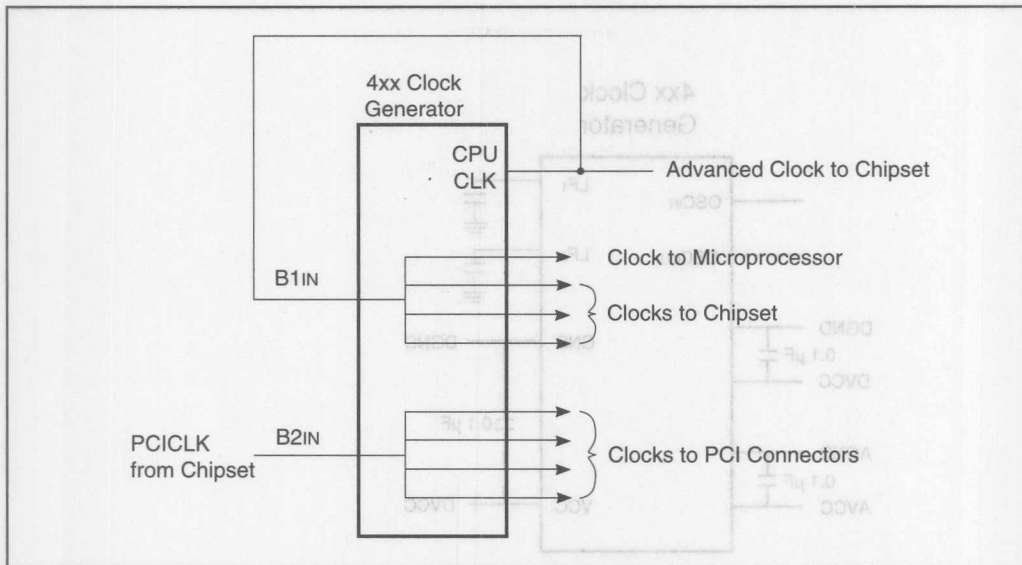


Figure 5. Use 4XX Clock Generator on SIS Motherboards.

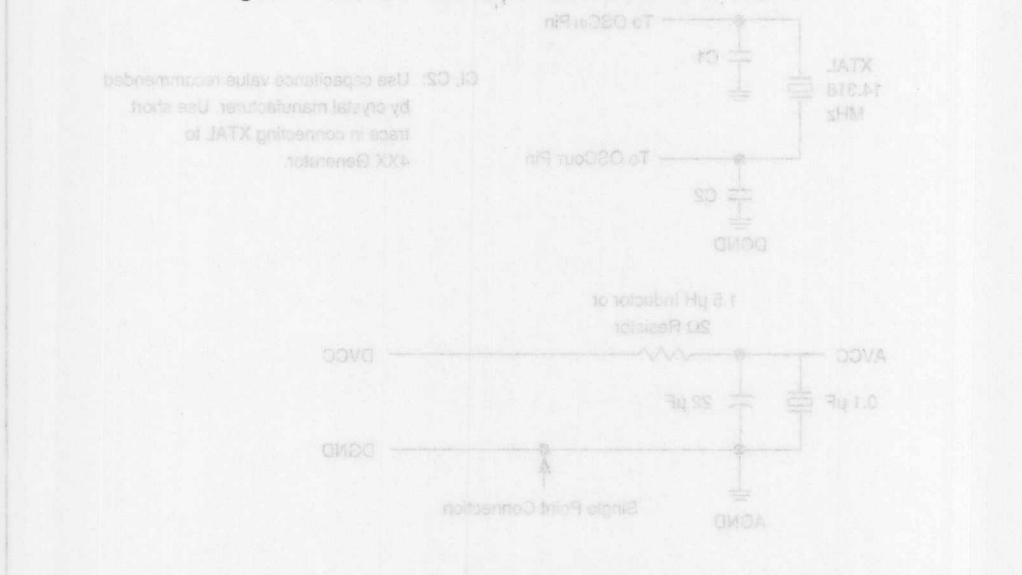


Figure 6. XTAL and Power/Ground Connections

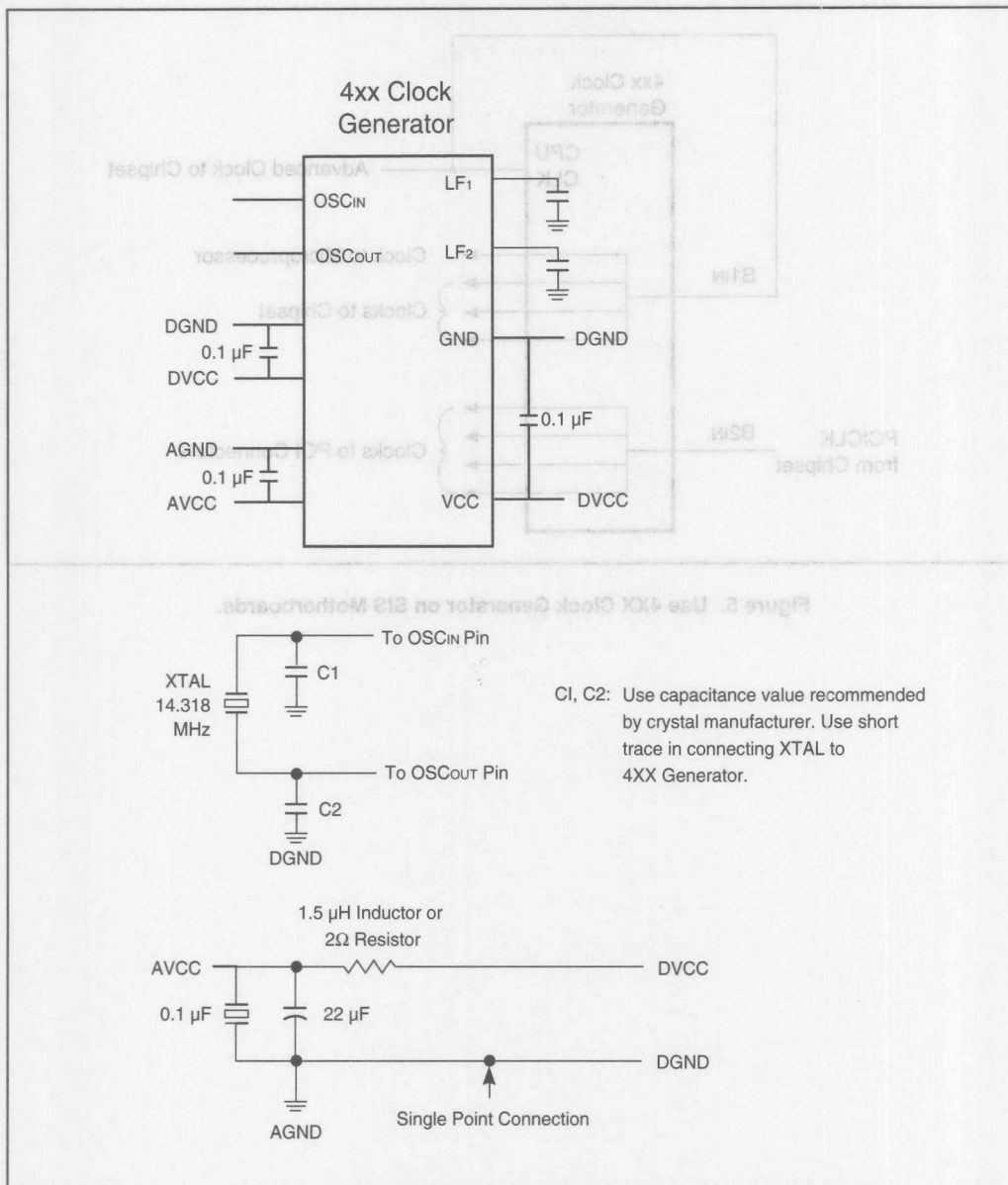


Figure 6. XTAL and Power/Ground Connections

Pericom FCT Logic for Hot Plug Applications

Introduction

"Hot-Plug" and "Live Insertion" are both terms that apply to the technique of adding or removing modular components from a system while power is applied and the system is fully or partially operational.

These systems might typically be a complex computer system used for airline ticket reservations or for a large department store, where even short periods of down-time can result in thousands or even millions of dollars of lost business and good will. Another typical "Hot Plug" system might easily be found in a hospital where, although not used directly for life-support, a badly timed (or lengthy) computer failure can seriously delay the movement of critical information necessary for both health maintenance as well as for billing and insurance management.

One growing application that needs hot plug capability is portable computers, where deck insertion and removal from a docking station and the insertion and removal of PCMCIA cards often occur while power is applied.

Pericom Semiconductor's family of FCT, fast TTL compatible CMOS logic, when used in conjunction with good design practices can allow dynamic removal and insertion of subsystem modules while the power is on and the system is operating.

The Working Environment

Typically, hot plug modules or cards are connected to a system through a live backplane. In some instances, a disabled or powered-down section of an existing board may be activated and subsequently enabled onto an internal system bus. Both of these instances require similar design considerations.

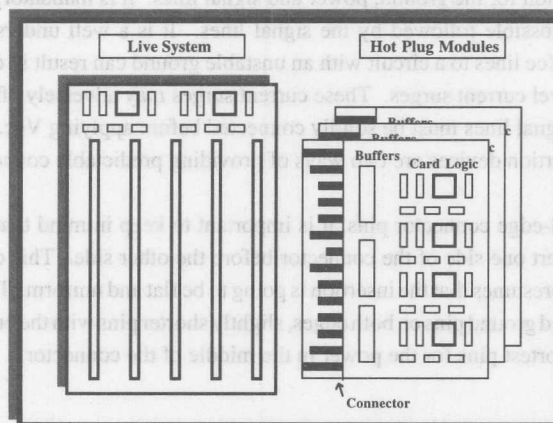


Figure 1. A Bus-Based System with Hot Plug Modules

When designing a system with hot-plug capabilities two main issues come to light:

- Uninterrupted system operation,
- Protection of all devices during the insertion or removal operation.

The management of system operation begins with the impact of the module that is being added or removed. Adding new functionality to an existing system (expanding communications, adding additional processors or memory, etc.) usually depends on the ability of the system to integrate the new devices on-the-fly, assuming that the process of adding the new module is clean. In this application, (as well as during re-insertion of a repaired or replaced module) the key issue is how to ensure that the addition of the module does not create any undesirable electrical conditions that may upset the operation of the operating bus. Transient isolation and suppression during the insertion process, as well as during the power-up of the new module is critical.

The second issue concerns protection of both the new circuit components as they power up as well as existing live components. In this situation, the design of the plug-in module, the target host and the connectors plays a very important role. Although power sequencing has traditionally been the main concern, power-on reset, power-on preset to known conditions, controlled output enables, controlled PCB trace length, device input and output structure design, per-pin and total capacitive load, host power supply characteristics, module power consumption and bypass design, low power detection and valid power detection as well as ESD protection (and more) all play a vital role in the overall design.

The following paragraphs will discuss how Pericom FCT devices can be successfully used as an interface between a host system and a hot-plug module as well as some important related design considerations.

Basic Design Considerations in Hot-Plug Systems

The Connector

When adding a module into a running system, the connecting mechanism must be designed to provide quick and solid electrical connection for the ground, power and signal lines. It is mandatory that the ground lines be connected as early as possible followed by the signal lines. It is a well understood phenomena that connecting signal lines or Vcc lines to a circuit with an unstable ground can result in device damage as well as unpredictable system level current surges. These current surges may adversely affect system operation. The ground and then the signal lines must be solidly connected before applying Vcc. Staggered connector pins and spring loaded insertion devices are two ways of providing predictable connections.

When using staggered card-edge connector pins, it is important to keep in mind that even with good card guides, it is possible to insert one side of the connector before the other side. This can defeat a card edge connector sequencing that presumes that the insertion is going to be flat and uniform. To minimize the effects of this situation, use extended ground pins on both edges, slightly shorter pins with the output enables and other control signals, and the shortest pins for the power in the middle of the connector.

Figure 1. A Bus-Based System with Hot Plug Modules

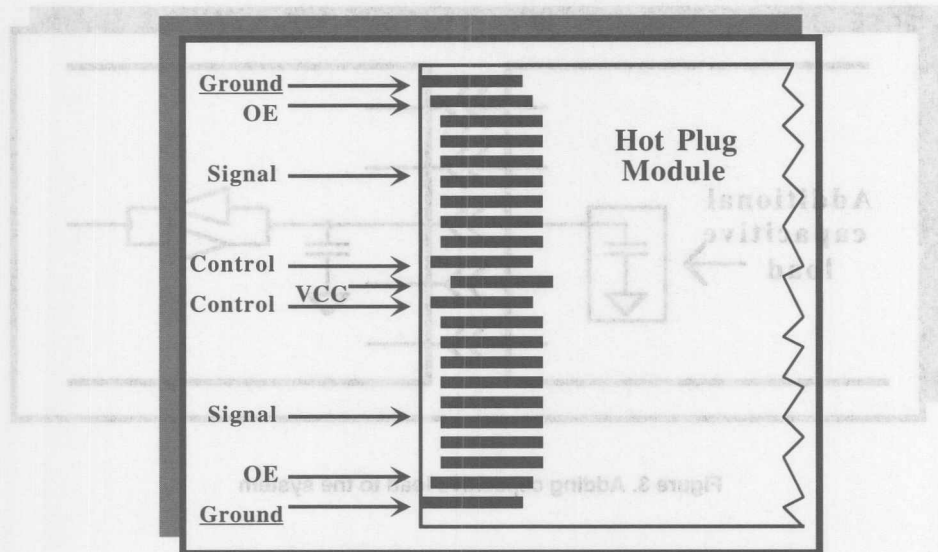


Figure 2. Staggered Finger Arrangement for Hot Plug Applications

The Capacitance

When a hot plug card is connected to a bus structure, an additional load is applied to the system signal lines. One major effect of this additional load on the target bus is caused by the instantaneous charge redistribution between the system's bus capacitance and the capacitance of the added load. In general, a card used for a hot-plug application should have a minimum number of loads connected to the bus signal lines, preferably only one device pin per signal. In addition, the device placement and trace layout of such a board must be designed to minimize trace length between the card edge or the card's connector to the board's components. This will help to minimize the capacitive load connected to the bus. Additional capacitive loads of 5 pF up to 20 pF will typically have no discernible effect on active signal levels of a bus driven by FCT devices. In the case of an internal bus with weak drivers, close attention will need to be paid to the drive characteristics of the devices used and their susceptibility to the addition of capacitive loads while operational. In some cases, experimentation may be required.

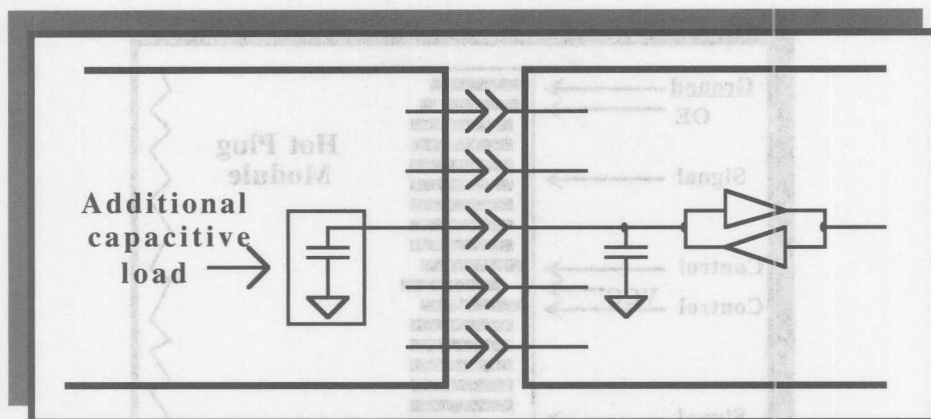


Figure 3. Adding capacitive load to the system

The Enables

The logic on the hot plug card must be designed to disable all output signals going off board while power up is taking place. Once the card has stable power, the card logic or the host system may then enable the I/Os onto the system bus. Often, pull-up (or pull-down) resistors are added to these lines to force them to known states during uncontrolled conditions. This solution has some problems associated with it which are addressed later in this paper.

Pericom FCT Input and Output Structures

Signal pins connected to the host bus at the card-edge may be inputs, outputs, tri-state I/Os. The Input structure of a typical FCT device will be reviewed first.

The Input Structures

All FCT logic input (and output) structures have industry standard (2000 volt) ESD protection circuits. All devices have input clamp diodes to ground, and most have hysteresis circuitry. Unlike many TTL devices, Pericom FCT does not have a clamp diode to Vcc.

This lack of a Vcc clamp diode is very important for hot plug applications. A Vcc clamp diode will limit the input voltage to the Vcc level existing on the device's Vcc pin. If the Vcc pin is at ground, then the Vcc clamp diode shunts the input pin to ground. This is a real problem for an active system! With Pericom's FCT logic, the inputs (and outputs and control lines as well) can tolerate levels up to 7V regardless of the Vcc level.

The Output Structures

Traditional CMOS Logic

Some CMOS logic families have an output structure consisting of an N channel between the output ground and a P Channel transistor from Vcc to the output pin. The P-channel transistor creates an inherent diode from the output pin to Vcc. As a result, when the output is not driven by the device (disabled) or when the Vcc pin at any level below the level seen on the pin, the signal is effectively "clamped" to Vcc. Again, this means that in hot plug operation such devices will temporarily short some system signals to ground.

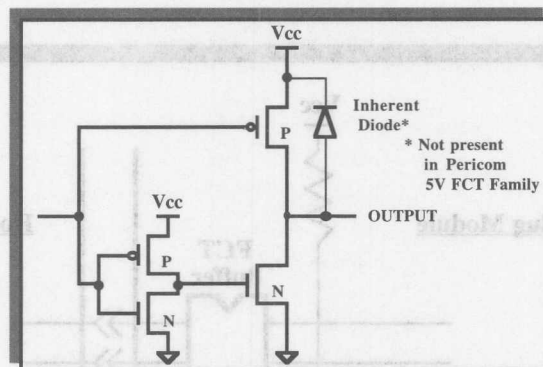


Figure 3. Output Stage with N-P Structure

Pericom 5V FCT TTL Compatible CMOS Logic

Pericom's FCT output stage is made up of only N-channel transistors between the output and Vcc and ground (Figure 4). This structure isolates the output pin when disabled so that the host system can drive normal logic swings regardless of the Vcc supply to the output stage. This allows designers to connect the I/Os of an unpowered FCT device to an active bus without worrying about the integrity of the FCT devices or impacting the active logic state of the bus. Pericom FCT Logic typically has about 5 pF or 6 pF of capacitance per pin, so the insertion is accomplished with a minimum of trauma.

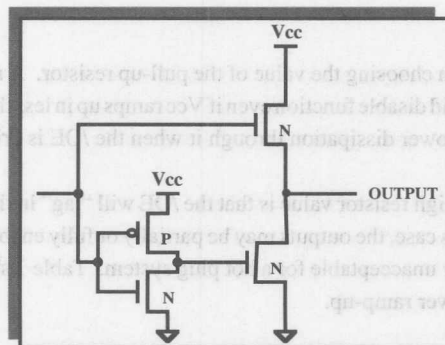


Figure 4. N-N Output Stage Structure

Hot Plug Implementation Scenarios

Figure 5 depicts a simple circuit that can be used to disable the hot-plug card I/Os during power-up as well as allow the hot-plug card's logic to enable/disable the buffers during normal operation. The use of a pull-up resistor guarantees that the /OE line will follow Vcc, thus keeping the FCT I/Os disabled. Once the system has power, a logic low on the /OE signal will enable the I/Os onto the bus. The enable signal can also be sourced from the host system, allowing the module to be enabled when the system desires.

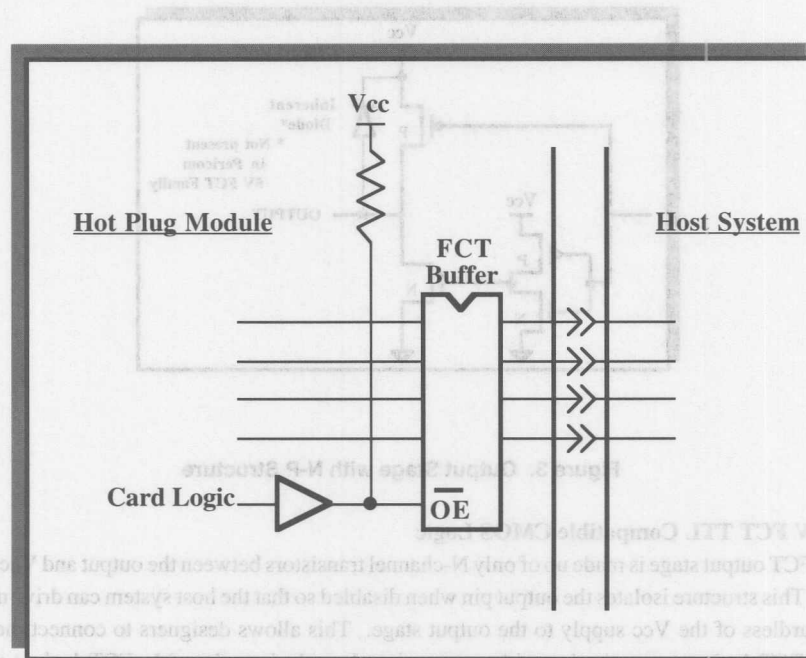


Figure 5. Simple Example of Output Enable Control for Hot-Plug Applications

Special care must be exercised in choosing the value of the pull-up resistor. A resistor with a value of a few hundreds ohms will provide a solid disable function even if Vcc ramps up in less than 100 ns. The disadvantage of a small resistor value is the power dissipation through it when the /OE is driven low.

The main item of concern with high resistor value is that the /OE will "lag" in time behind Vcc, especially if the Vcc ramps up quickly. In this case, the outputs may be partially or fully enabled accidentally when power is ramping up. This is obviously unacceptable for a hot plug system. Table 1 shows some examples of Vcc and the minimum allowable power ramp-up.

Table 1. Minimum Vcc ramp-up allowed for Different pull-up resistor values.

Minimum Ramp-up Time	Pull-Up (Ohms)
80 ns	500
200 ns	20K
800 ns	100K
4 ms	200K

The rate at which power ramps up on a board which is dynamically plugged into an active system depends mainly on the capacitance seen by the host power lines that connect the board to the system power and the ability of these lines to source current. A typical logic board has multiple decoupling capacitors, and one or more are going to be seen by the power line as the effective impedance of the board. While limiting the ability of the power line to drive may seem to be counterproductive, a very high current upon insertion of a board into the system may adversely affect the rest of the system. In a typical system, the ramp-up rate of the power on a hot plug board is on the order of 50 microseconds, thus allowing a relatively large resistor value to be used for /OE pull-up. Of course this depends heavily on what logic and bypass is on the hot plug board.

Summary

Pericom FCT logic has been designed with features necessary to support hot plug applications. The input stage has no restriction on input voltage while power is ramping up, and the output stage can be pulled above Vcc when disabled due to the N-N output structure. In addition, the output enable circuitry can disable the output logic during power up as long as the /OE level is close enough to the rising Vcc to avoid false enables.

Pericom Semiconductor Corporation, located in San Jose, California, offers leading edge product families consisting of: Fast FCT bus interface and decode logic, PLL clock synthesis chips, high-speed clock and data distribution chips, a full line of "zero-propagation" delay bus switch devices, 16-bit FCT logic in industry standard SSOP and TSSOP packages as well as a line of datacom products which include active retiming and jitter attenuating Token Ring hub interface chips.

Table 1. Minimum Vcc ramp-up allowed for Distortion pull-up resistor values.

Minimum Ramp-up Time	Pull-Up (Ohms)
80 ns	500
200 ns	20K
800 ns	100K
4 ms	200K

The rate at which power ramps up on a board which is dynamically plugged into an active system depends mainly on the capacitance seen by the host power lines that connect the board to the system power and the ability of these lines to source current. A typical logic board has multiple decoupling capacitors, and one or more are going to be seen by the power line as the effective impedance of the board. While limiting the ability of the power line to drive may seem to be counterproductive, a very high current upon insertion of a board into the system may adversely affect the rest of the system. In a typical system, the ramp-up rate of the power on a hot plug board is on the order of 50 microseconds, thus allowing a relatively large resistor value to be used for OE pull-up. Of course this depends heavily on what logic and bypass is on the hot plug board.

Summary

Pericom FCT logic has been designed with features necessary to support hot plug applications. The input stage has no restriction on input voltage while power is ramping up, and the output stage can be pulled above Vcc when disabled due to the N-N output structure. In addition, the output enable circuitry can disable the output logic during power up as long as the OE level is close enough to the rising Vcc to avoid false enables.

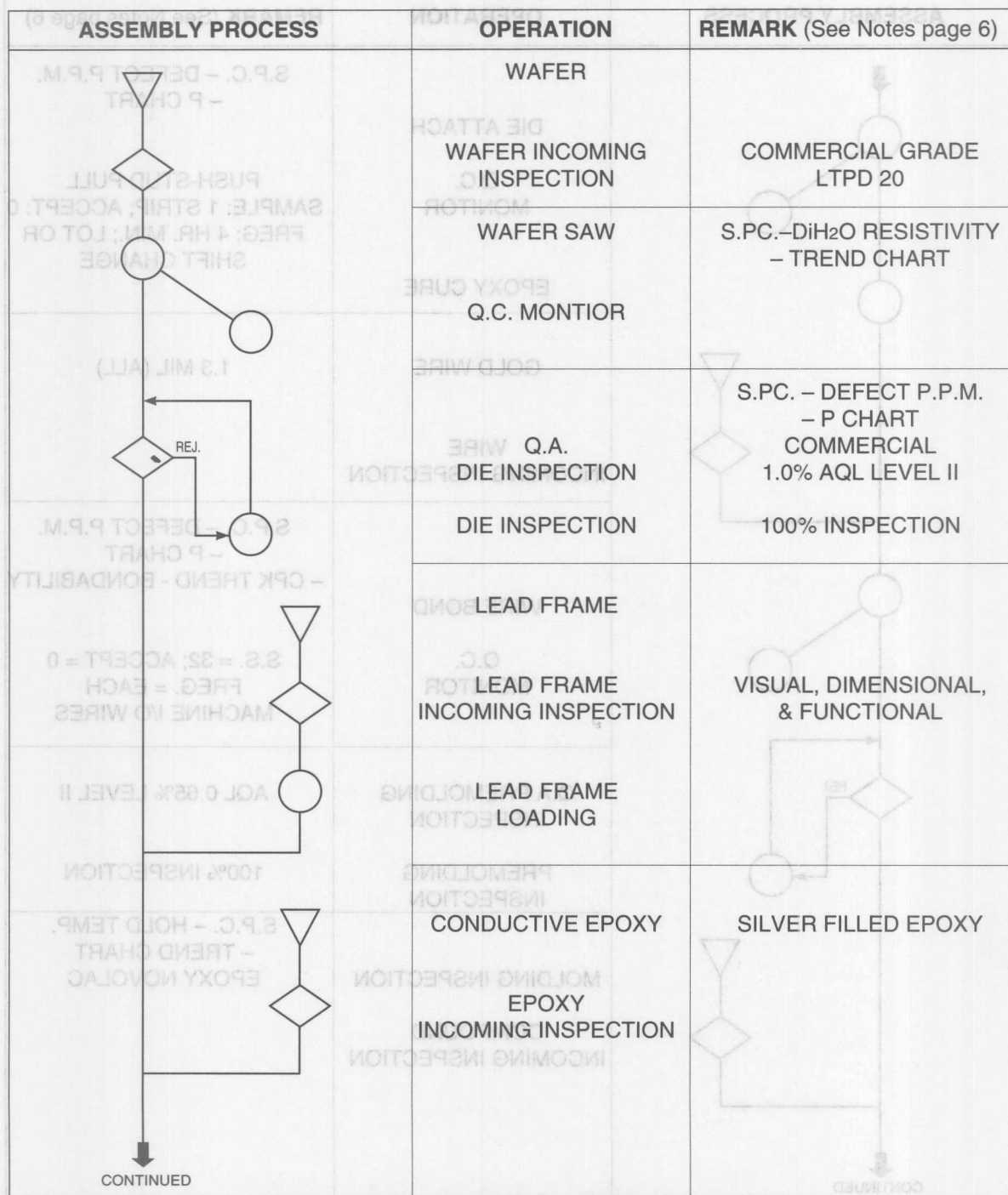
Pericom Semiconductor Corporation, located in San Jose, California, offers leading edge product families consisting of Fast FCT bus interface and decoder logic, PLL clock synthesis chips, high-speed clock and data distribution chips, a full line of "zero-propagation" delay bus switch devices, 16-bit FCT logic in industry standard SSOP and TSOP packages as well as a line of datacom products which include active retaining and jitter reducing Token Ring hub interface chips.

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5V FCT LOGIC PRODUCTS****3****DOUBLE DENSITY 3.3V FCT LOGIC PRODUCTS****4****STANDARD 3.3V LOGIC PRODUCTS
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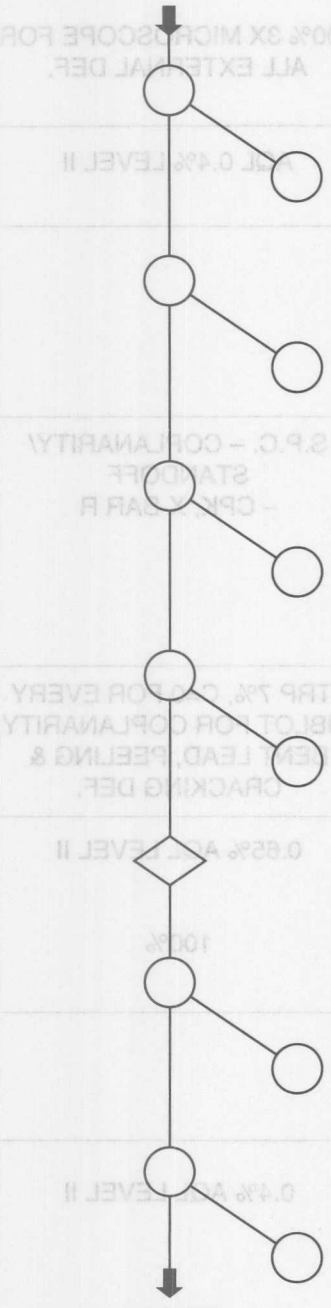
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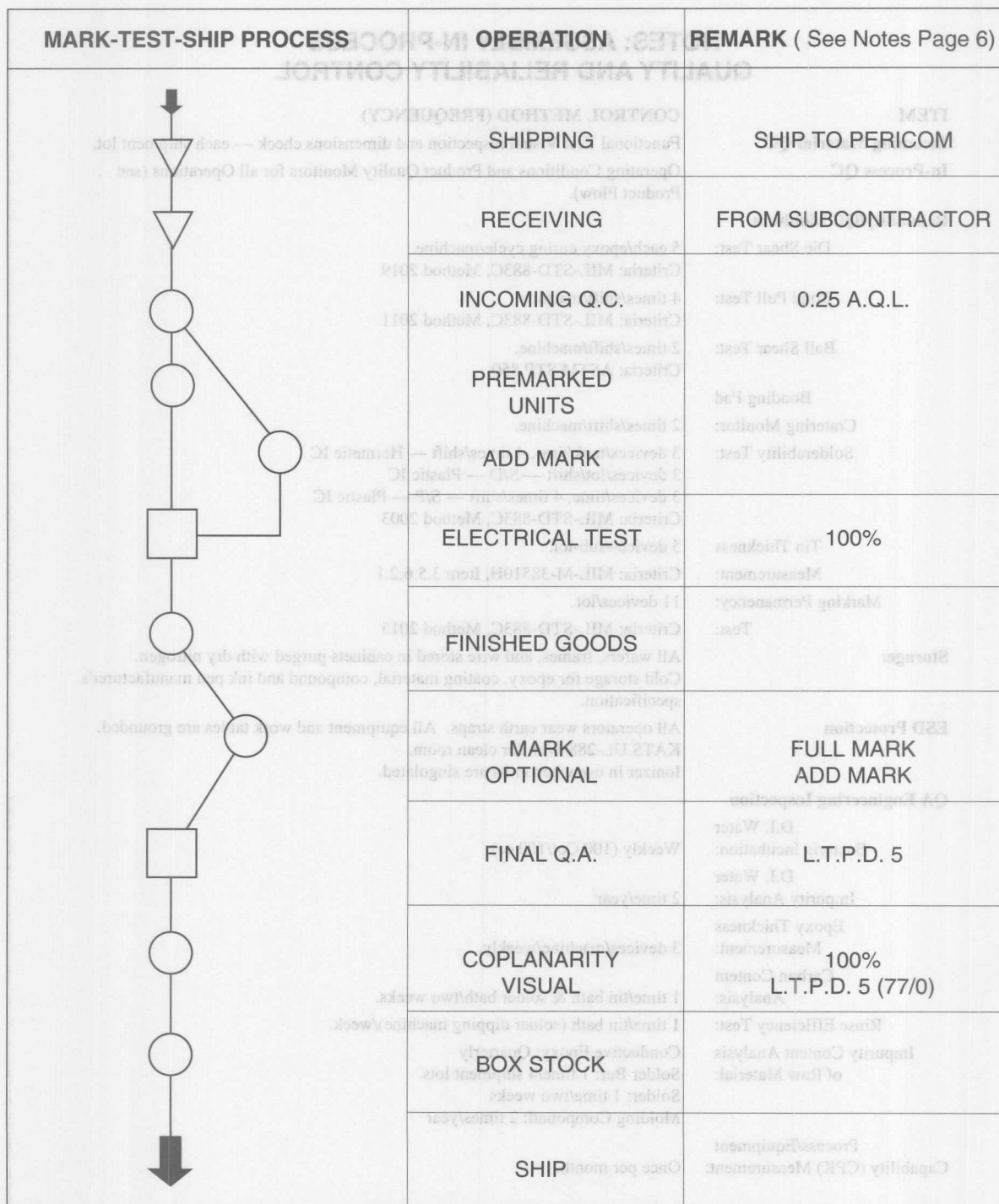
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ASSEMBLY PROCESS FLOW



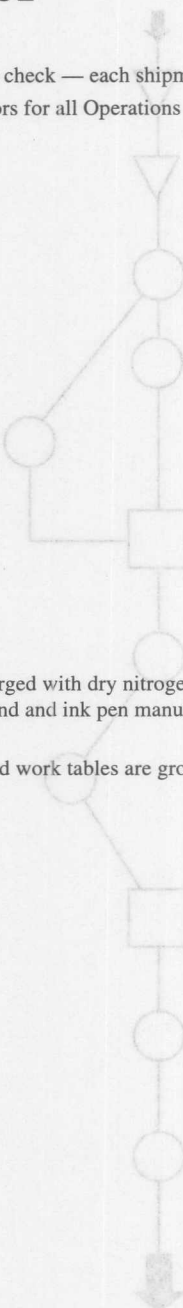
02/02/95

ASSEMBLY PROCESS	OPERATION	REMARK (See Notes Page 6)
	MOLDING	
	Q.C. MONITOR	S.S., STRIP: 1, ACCEPT: 0, FREQ.: 2X SHIFT CHANGE
	DEJUNK TRIM	
	Q.C. MONITOR	S.S., STRIP: 1, ACCEPT: 0 FREQ: 3X SHIFT REPAIR SHIFT CHANGE
	DEFLASH	
	Q.C. MONITOR	
	BOTTOM SIDE MARK	
	Q.C. MONITOR	
	Q.A. TOP SIDE MARK	A.Q.L. 0.4% LEVEL II
	POST MOLD CURE	
	Q.C. MONITOR	
	SOLDER PLATING	S.P.C. – THICKNESS – X-BAR R CHART – CARBON/CL CONTENT – TREND CHART
	Q.C. MONITOR	



NOTES: ASSEMBLY IN-PROCESS
QUALITY AND RELIABILITY CONTROL

ITEM	CONTROL METHOD (FREQUENCY)
Incoming Material QC	Functional Test Visual inspection and dimensions check — each shipment lot.
In-Process QC	Operating Conditions and Product Quality Monitors for all Operations (see Product Flow).
Reliability/QC Monitors	
Die Shear Test:	5 each/epoxy curing cycle/machine. Criteria: MIL-STD-883C, Method 2019
Bond Pull Test:	4 times/shift/machine. Criteria: MIL-STD-883C, Method 2011
Ball Shear Test:	2 times/shift/machine. Criteria: ASTM STP 850
Bonding Pad	
Cratering Monitor:	2 times/shift/machine.
Solderability Test:	3 devices/tank/time, 4 times/shift — Hermetic IC 3 devices/lot/shift — S/D — Plastic IC 3 devices/time, 4 times/shift — S/P — Plastic IC Criteria: MIL-STD-883C, Method 2003
Tin Thickness	5 devices/sub-lot.
Measurement:	Criteria: MIL-M-38510H, Item 3.5.6.2.1
Marking Permanency:	11 devices/lot.
Test:	Criteria: MIL-STD-883C, Method 2015
Storage:	All wafers, frames, and wire stored in cabinets purged with dry nitrogen. Cold storage for epoxy, coating material, compound and ink pen manufacturer's specification.
ESD Protection	All operators wear earth straps. All equipment and work tables are grounded. KATS UL-288 Wax for clean room. Ionizer in use when units are singulated.
QA Engineering Inspection	
D.I. Water	
Bacteria Incubation:	Weekly (100 Col/100 cc).
D.I. Water	
Impurity Analysis:	2 time/year.
Epoxy Thickness	
Measurement:	3 devices/machine/weekly.
Carbon Content	
Analysis:	1 time/tin bath & solder bath/two weeks.
Rinse Efficiency Test:	1 time/tin bath (solder dipping machine)/week.
Impurity Content Analysis	Conductive Epoxy: Quarterly
of Raw Material:	Solder Bar: 1 time/4 shipment lots Solder: 1 time/two weeks Molding Compound: 2 times/year
Process/Equipment	
Capability (CPK) Measurement:	Once per month.



NOTES (continued)
ASSEMBLY IN-PROCESS
QUALITY AND RELIABILITY CONTROL

ITEM	CONTROL METHOD (FREQUENCY)
Reliability Test	
Pressure Cooker Test:	Once per month by package type. (Sample Size: 32 pcs., 168 hours)
Temperature Cycle:	Once per month. (Sample Size: 32 pcs. 100/200 cycles)
Document Control System	All inspection criteria and operation procedures/conditions instructions are specified in documents.
Calibration System — Equipment and Instruments	To calibrate all tools, equipment, and instruments periodically in accordance with the requirement of MIL-STD-45662.
Environmental Monitor System	Cleaniness/atmosphere/temperature/relative humidity monitor to meet the requirement of FED-STD-209D.
Certification and Disqualified	
Qualification:	Q.A. Inspector, twice per year. Production inspector and operator, once per year.
Disqualified:	According to production inspector's monthly performance (Def PPM) to implement disqualification, retraining, and recertification system.
Traceability System	
Materials Tracking:	All production lots can be traced to supplier's lot of material used & IQC inspection results.
Assembly Conditions Tracking:	All production lots can be traced to assembly conditions.
Continuous Quality and Yield Improvement	
Attendant:	Production/Process Engineer and QA Staff.
Purpose:	To review and improve the quality and assembly yield.
Frequency:	Weekly.

(continued)

ASSEMBLY IN-PROCESS QUALITY AND RELIABILITY CONTROL

CONTROL METHOD (FREQUENCY)

ITEM

Reliability Test

Pressure Cooker Test

Once per month by package type.
(Sample Size: 32 per 168 hours)

Temperature Cycle

Once per month.
(Sample Size: 32 per 100/200 cycles)Document Control
SystemAll inspection criteria and operation procedures/conditions
instructions are specified in documents.Calibration System —
Equipment and
InstrumentsTo calibrate all tools, equipment, and instruments periodically
in accordance with the requirement of MIL-STD-45662.Environmental
Monitor SystemCleanroom/atmosphere/temperature/humidity monitor
to meet the requirement of FED-STD-209D.Certification and Disqualification
(Qualification)Q.A. Inspector, twice per year.
Production Inspector and operator, once per year.

Disqualified:

According to production inspector's monthly performance (Def PPM) to
implement disqualification, retraining, and recertification system.

Traceability System

Materials Tracking:

All production lots can be traced to supplier's lot of material used & IQC
inspection results.Assembly Conditions
Tracking:

All production lots can be traced to assembly conditions.

Continuous Quality and
Yield Improvement

Attendance:

Production/Process Engineer and QA Staff.

Purpose:

To review and improve the quality and assembly yield.

Frequency:

Weekly.

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141	50-pin Plastic TSSOP (240 Mils Wide)
142	20-pin Plastic PLCC (390 x 390)
143	20-pin Plastic TSSOP (170 Mils Wide)
143	8-pin Plastic DIP (300 Mils Wide)
144	14-pin Plastic DIP (300 Mils Wide)
144	16-pin Plastic DIP (300 Mils Wide)
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146	16-pin Plastic QSO (150 Mils Wide)
147	20-pin Plastic QSO (150 Mils Wide)
147	24-pin Plastic QSO (150 Mils Wide)
148	20-pin Plastic TSSOP (150 Mils Wide)
148	24-pin Plastic TSSOP (150 Mils Wide)
149	14-pin Plastic SOIC (300 Mils Wide)
149	16-pin Plastic SOIC (300 Mils Wide)
1410	20-pin Plastic SOIC (300 Mils Wide)
1410	24-pin Plastic SOIC (300 Mils Wide)
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1411	50-pin Plastic SSOP (300 Mils Wide)
1412	8-pin Plastic SOIC (150 Mils Wide)
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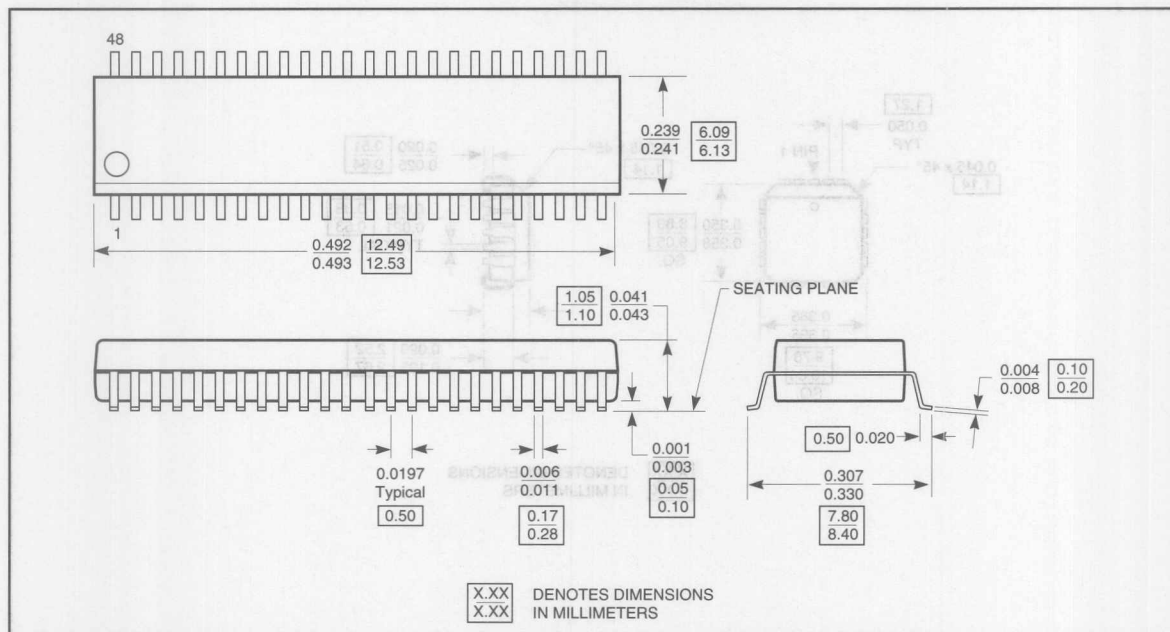
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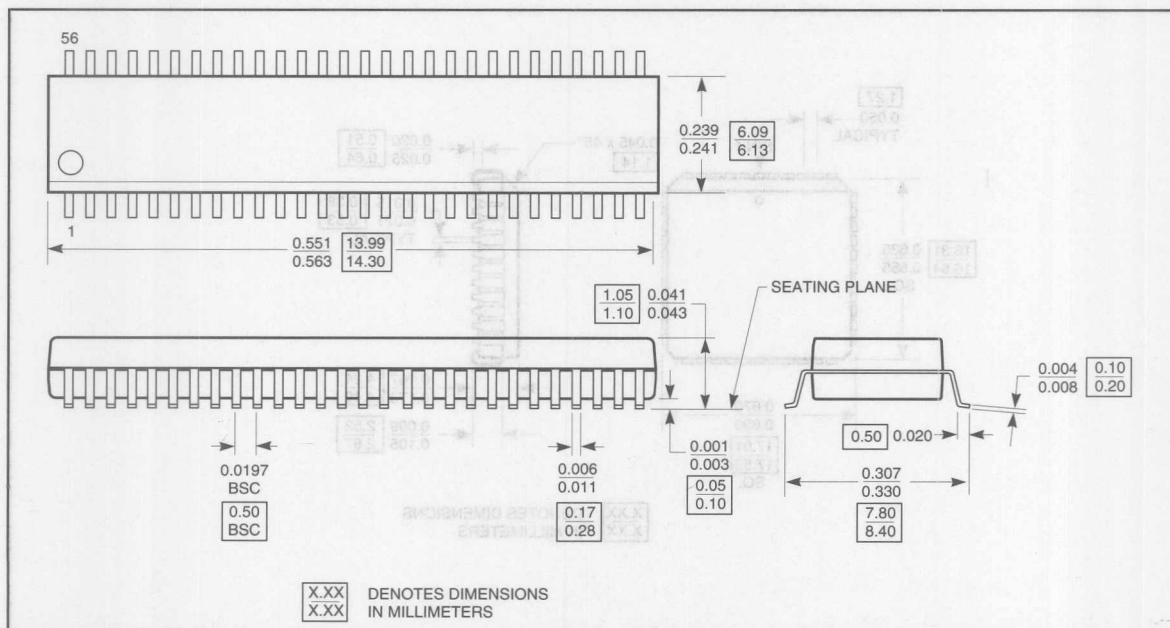
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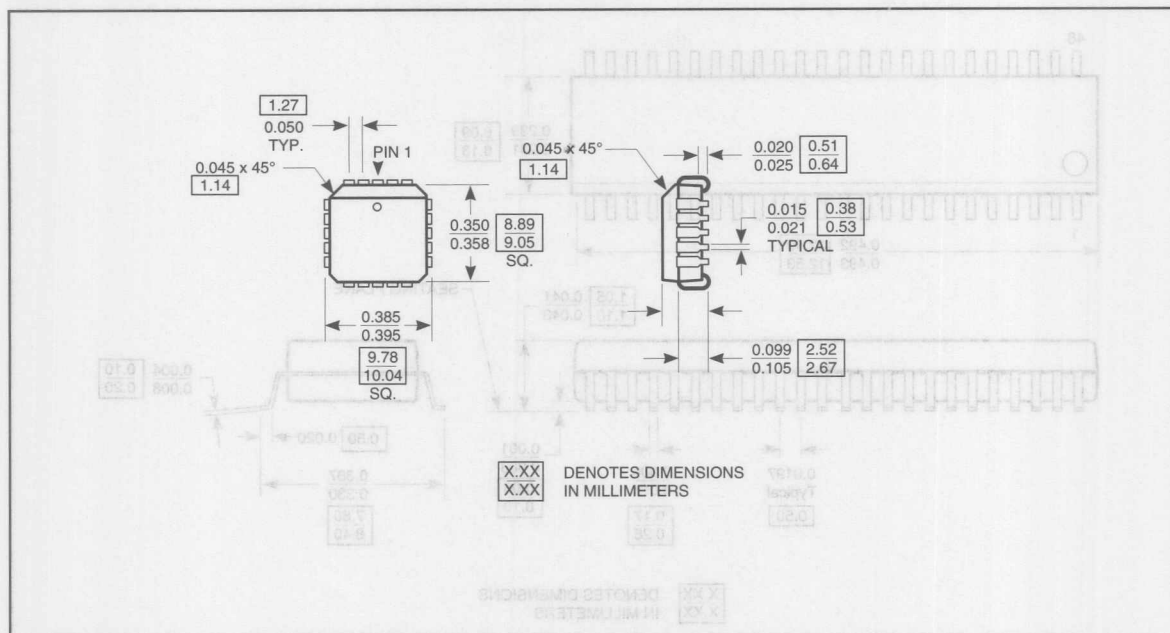
A48 — 48-Pin TSSOP (240 Mil Wide)



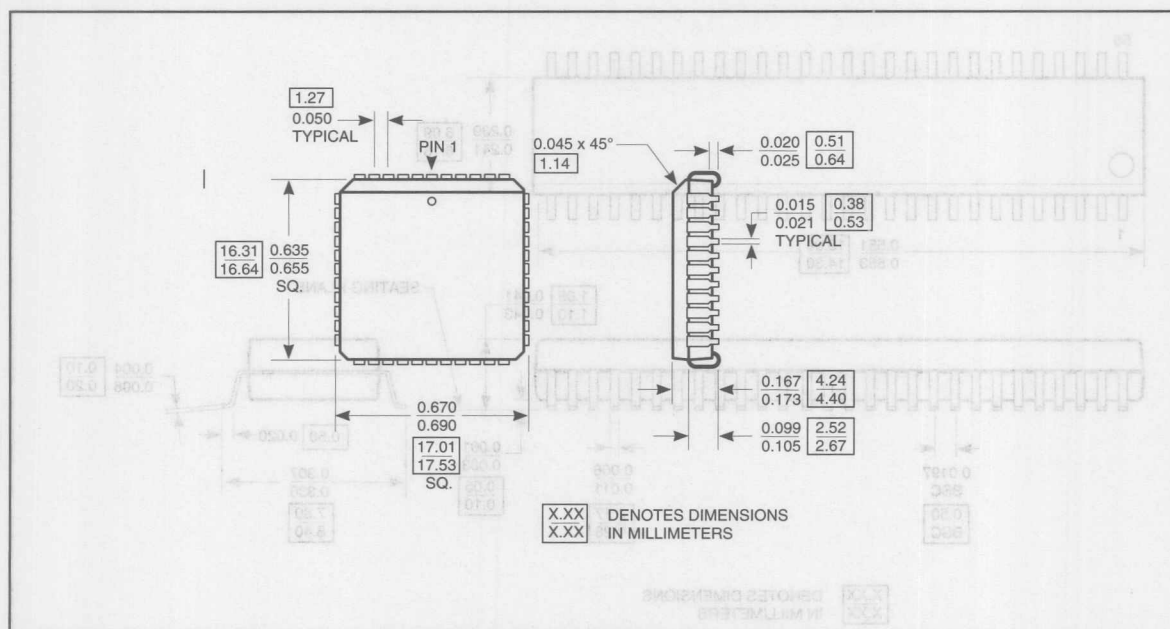
A56 — 56-Pin TSSOP (240 Mil Wide)

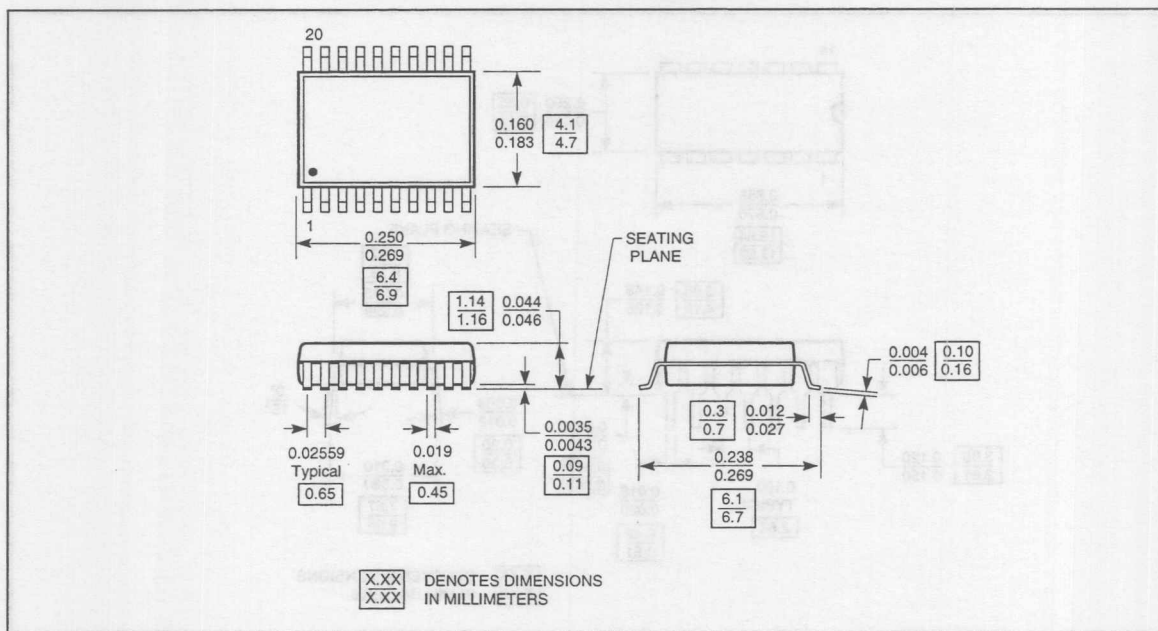
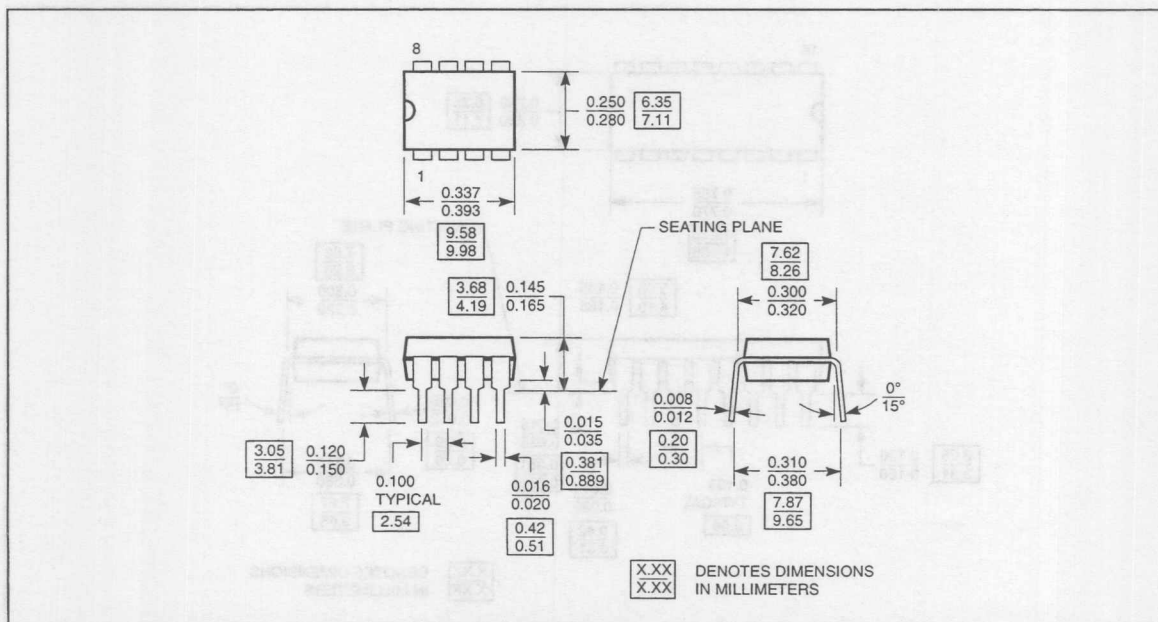


J20 — 20-Pin PLCC (390 x 390)

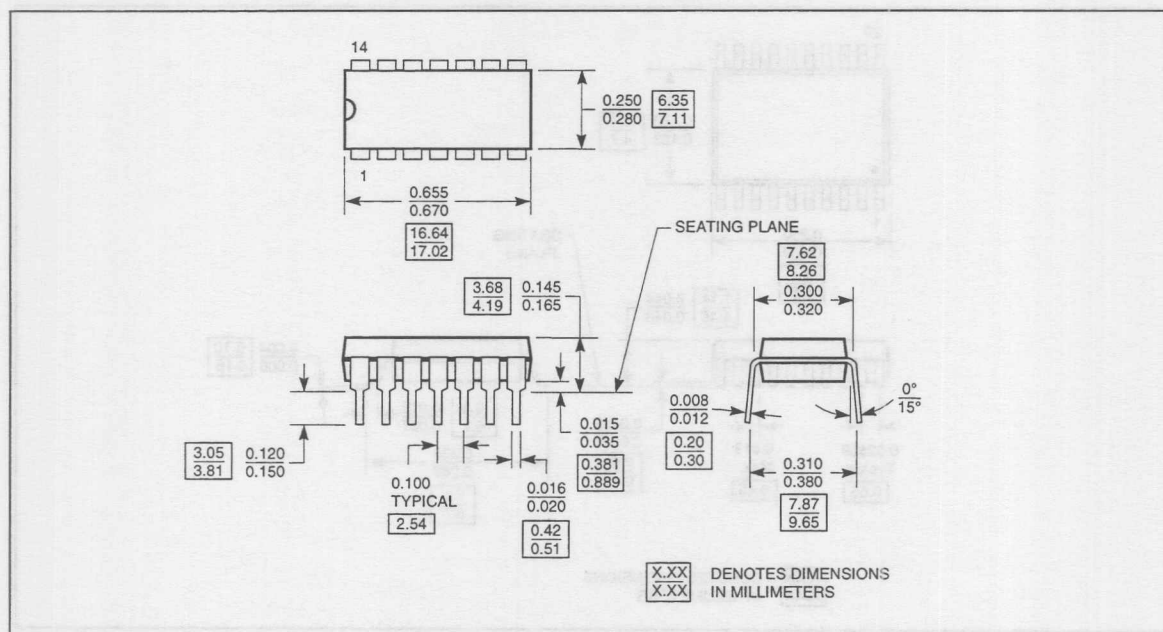


J44 — 44-Pin PLCC (680 x 680)

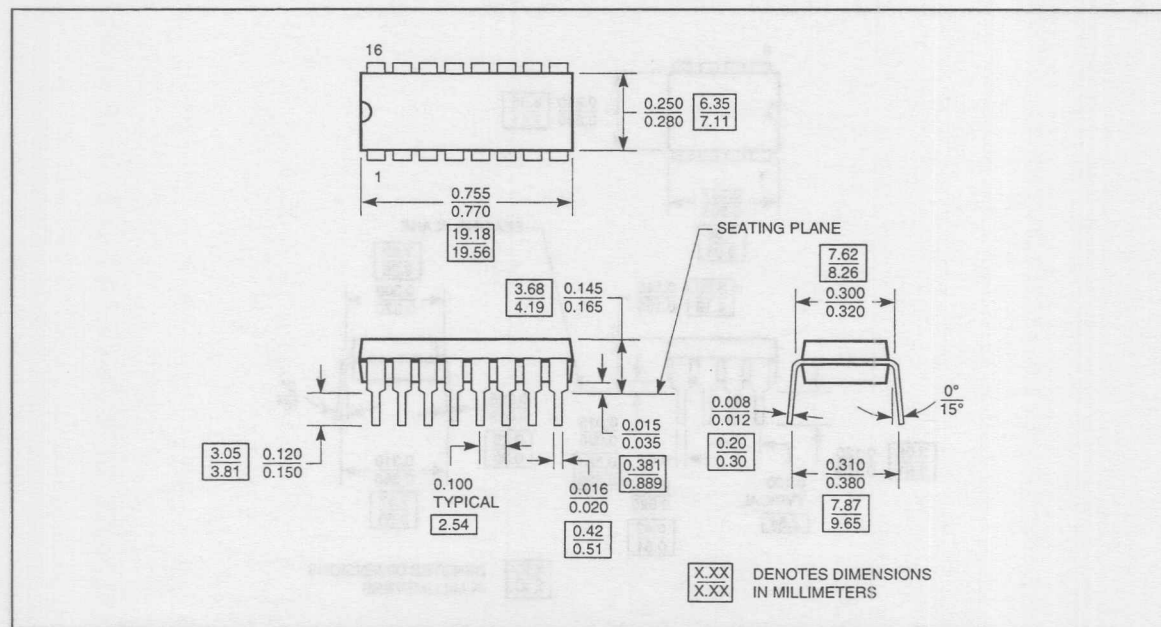


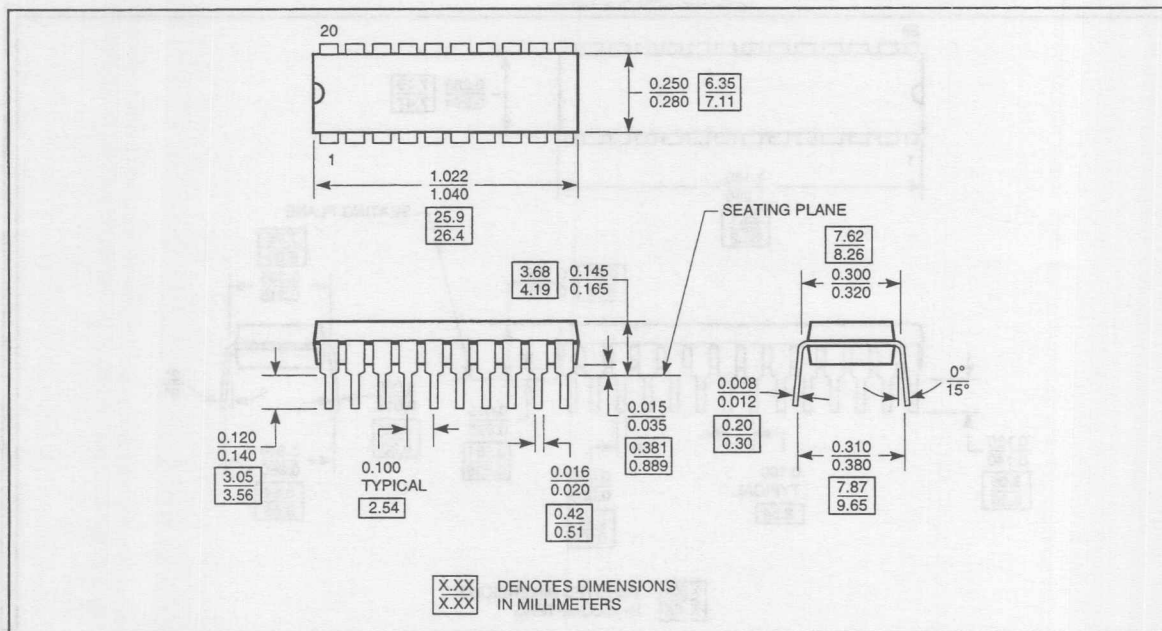
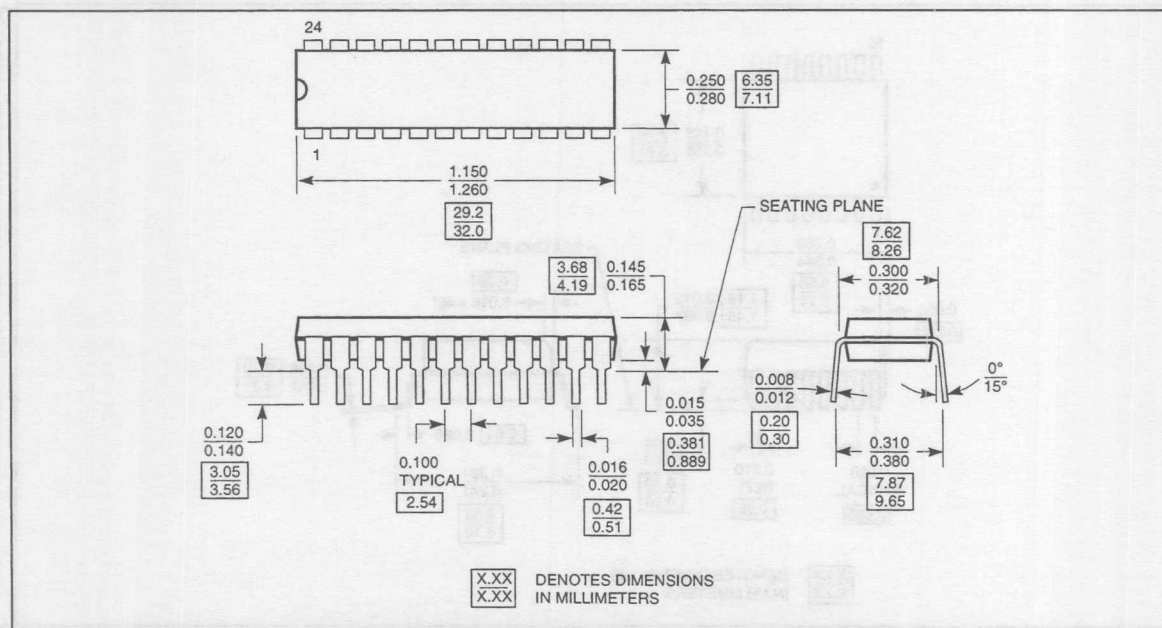
L20 — 20-Pin TSSOP (170 Mil Wide)

P8 — 8-Pin Plastic DIP (300 Mil Wide)


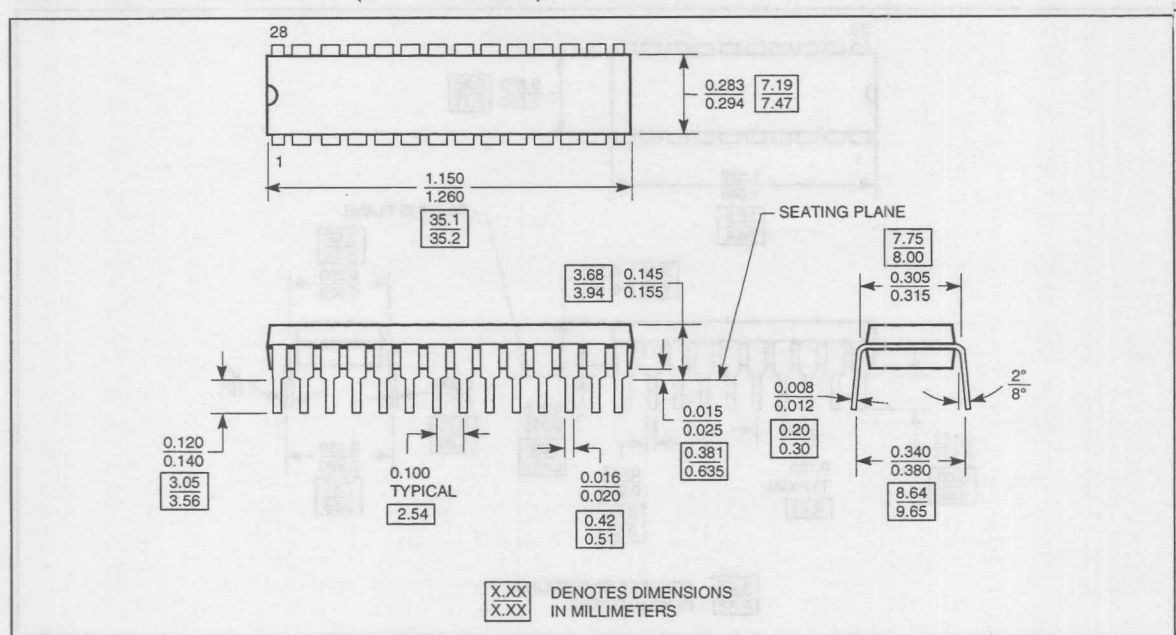
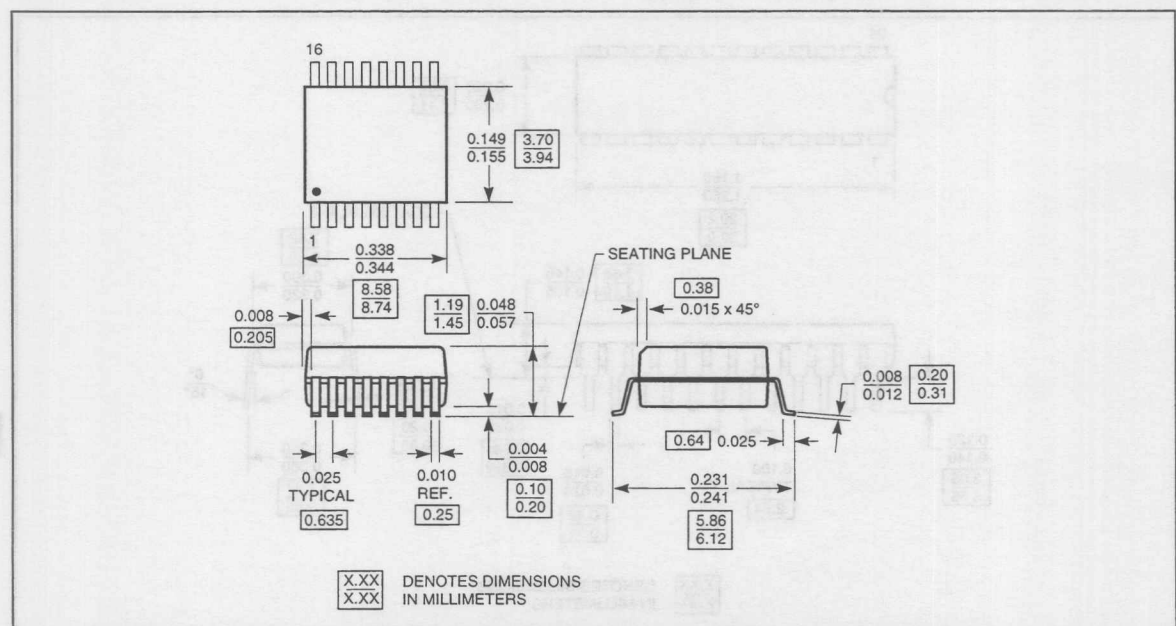
P14 — 14-Pin Plastic DIP (300 Mil Wide)



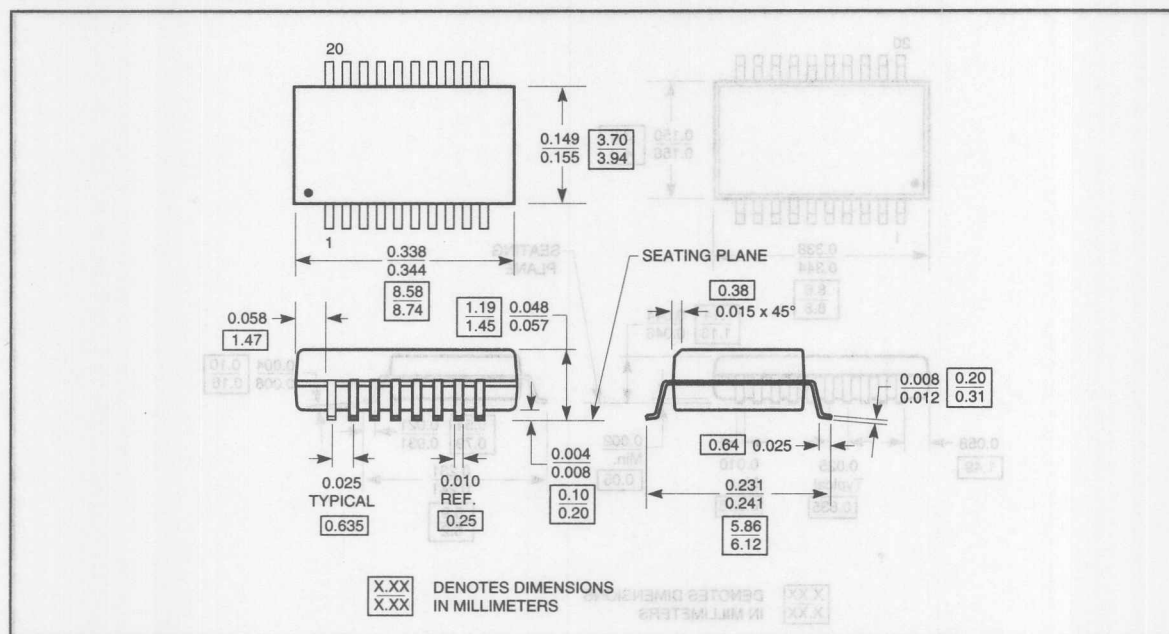
P16 — 16-Pin Plastic DIP (300 Mil Wide)



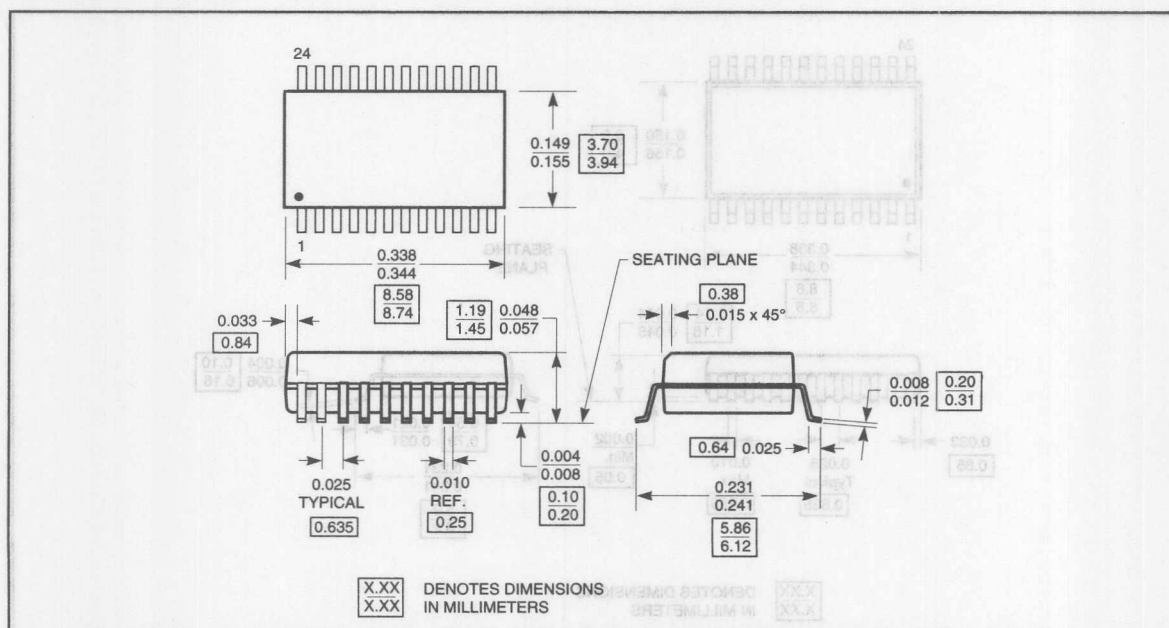
P20 — 20-Pin Plastic DIP (300 Mil Wide)

P24 — 24-Pin Plastic DIP (300 Mil Wide)


P28 — 28-Pin Plastic DIP (300 Mil Wide)

Q16 — 16-Pin QSOP (150 Mil Wide)


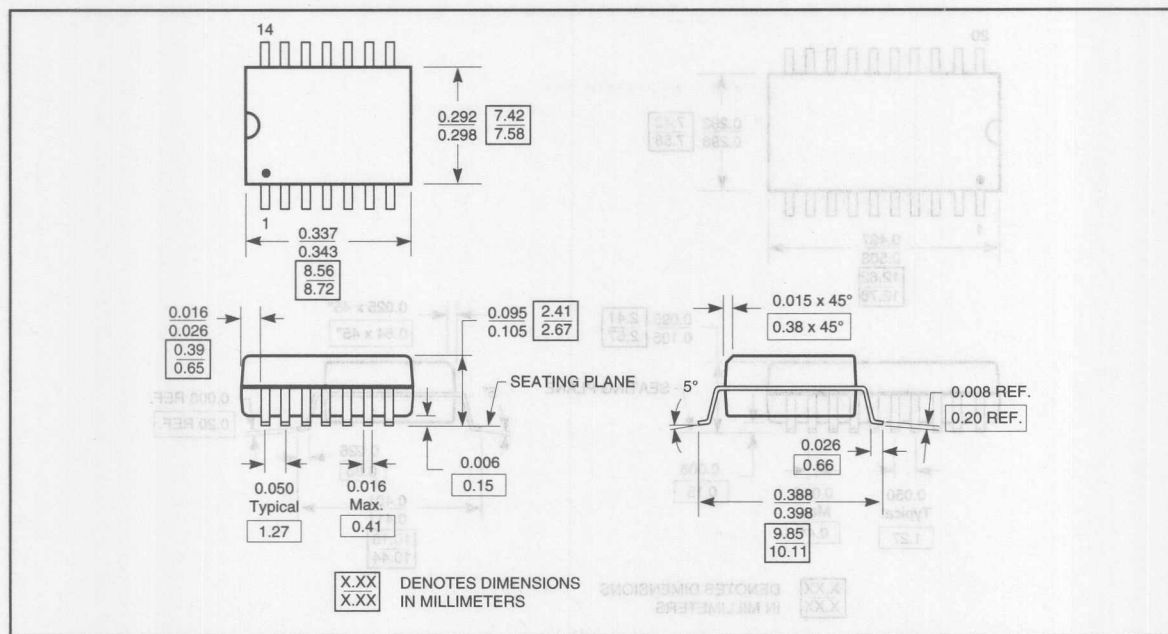
Q20 — 20-Pin QSOP (150 Mil Wide)



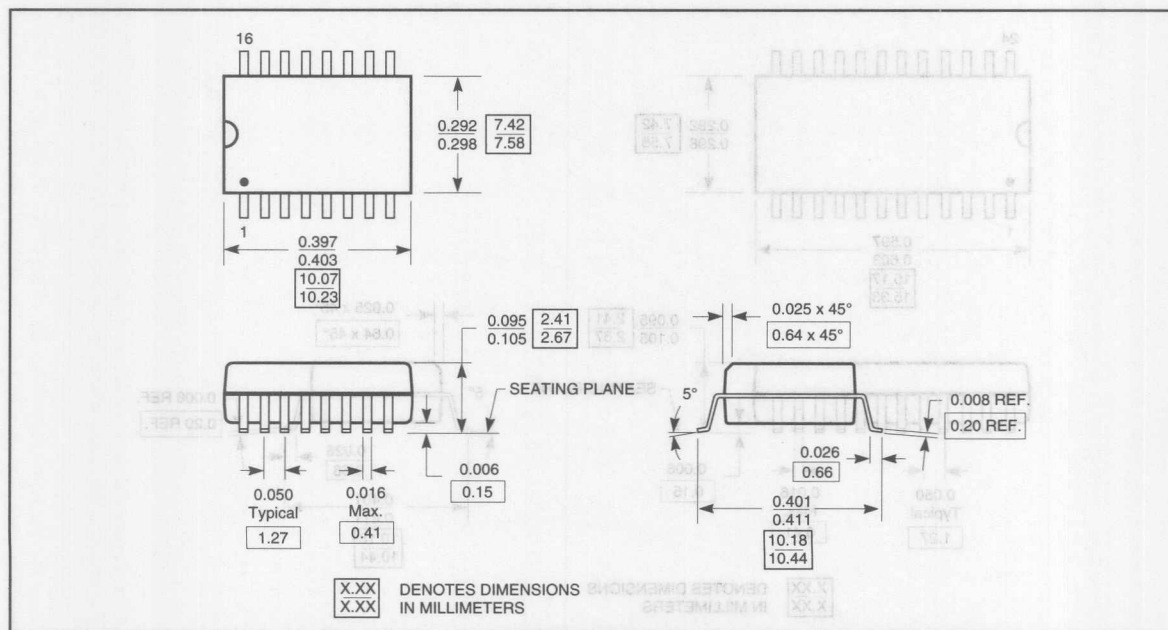
Q24 — 24-Pin QSOP (150 Mil Wide)



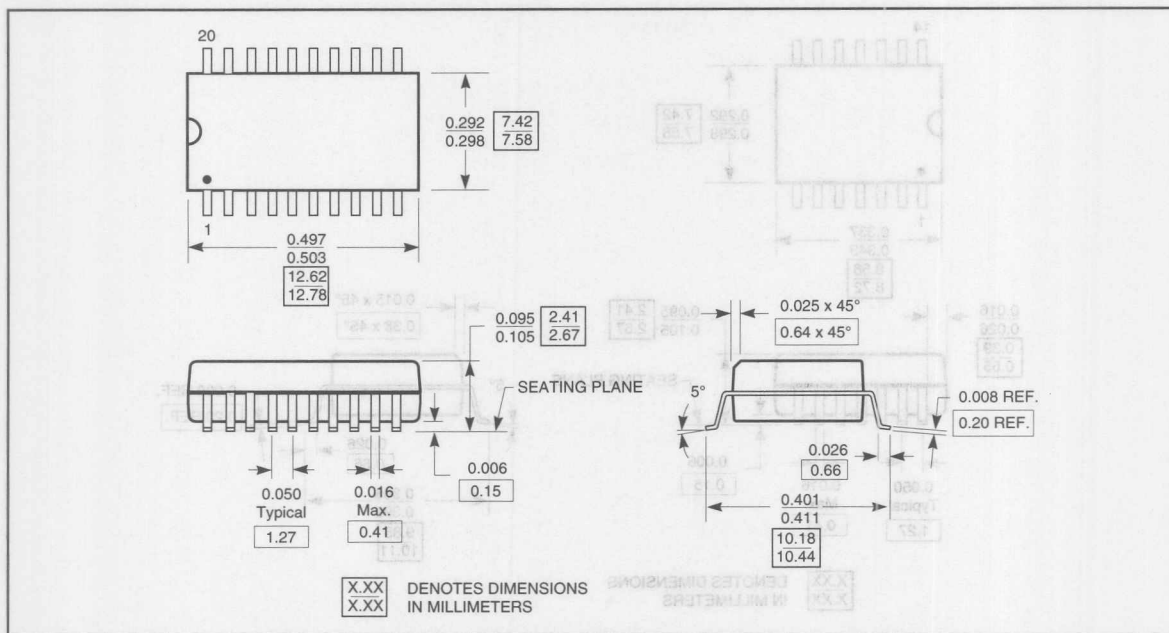
S14 — 14-Pin SOIC (300 Mil Wide)



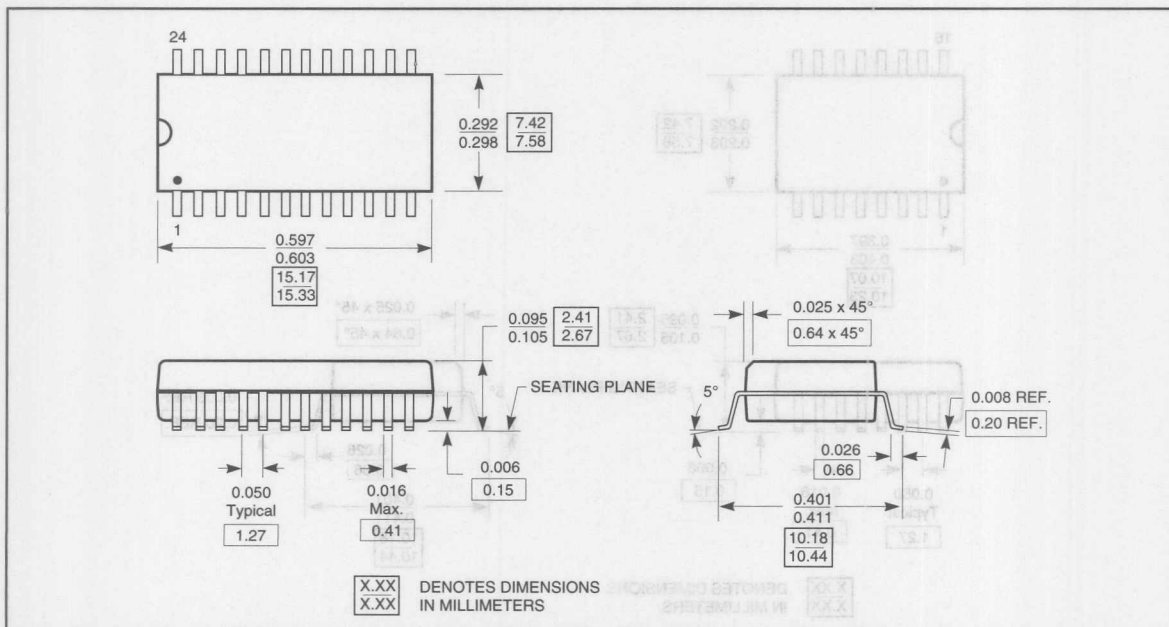
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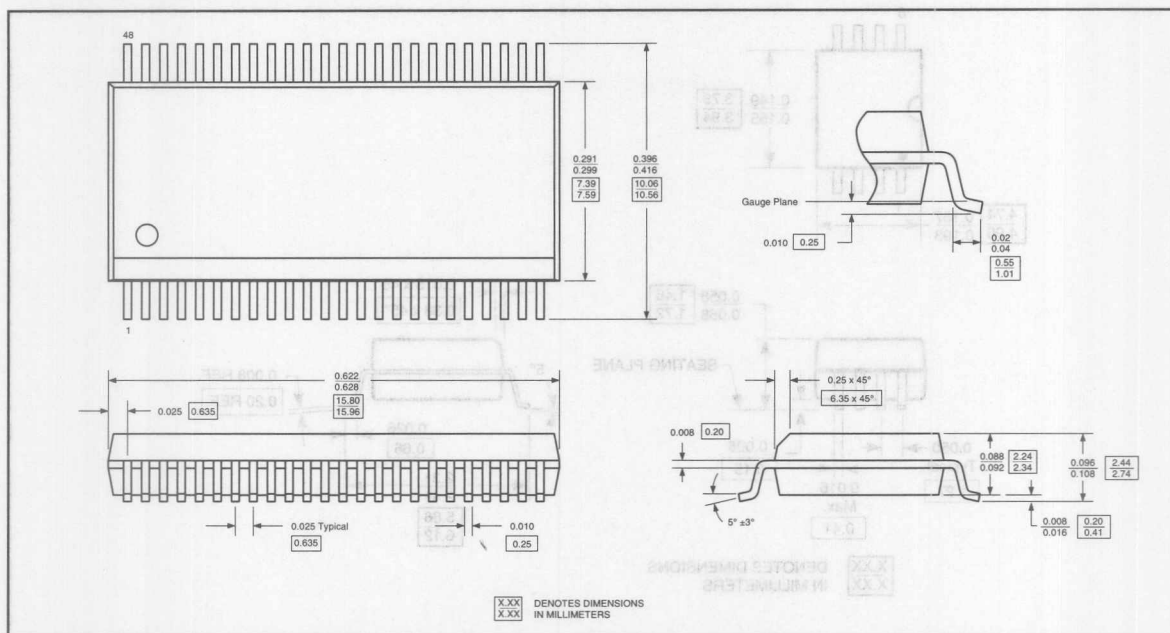
S20 — 20-Pin SOIC (300 Mil Wide)



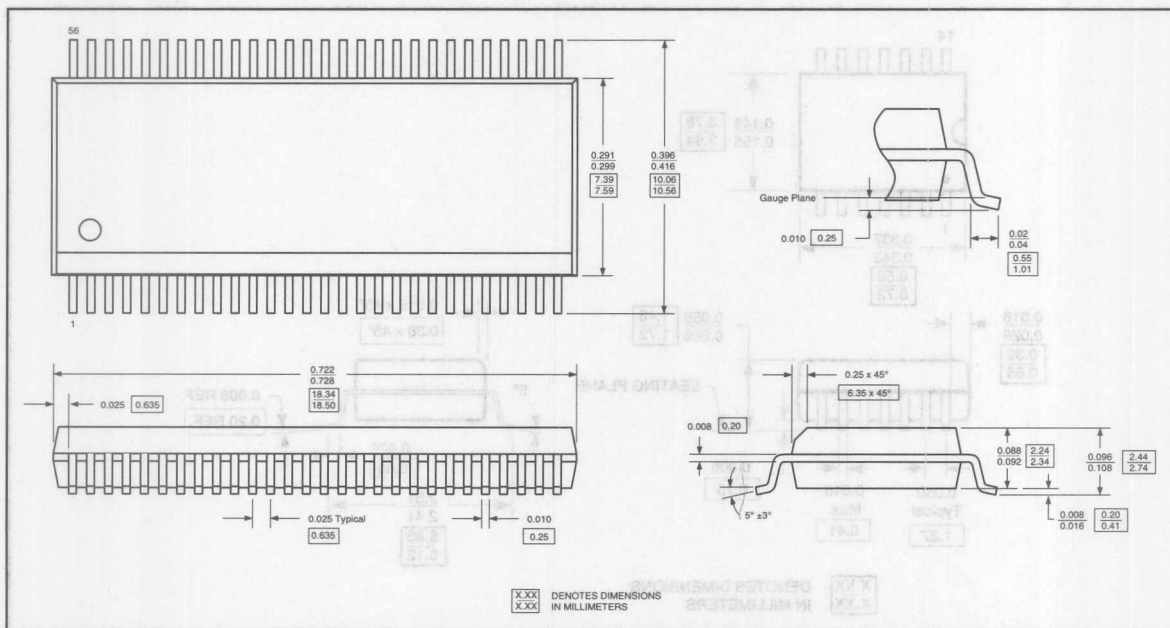
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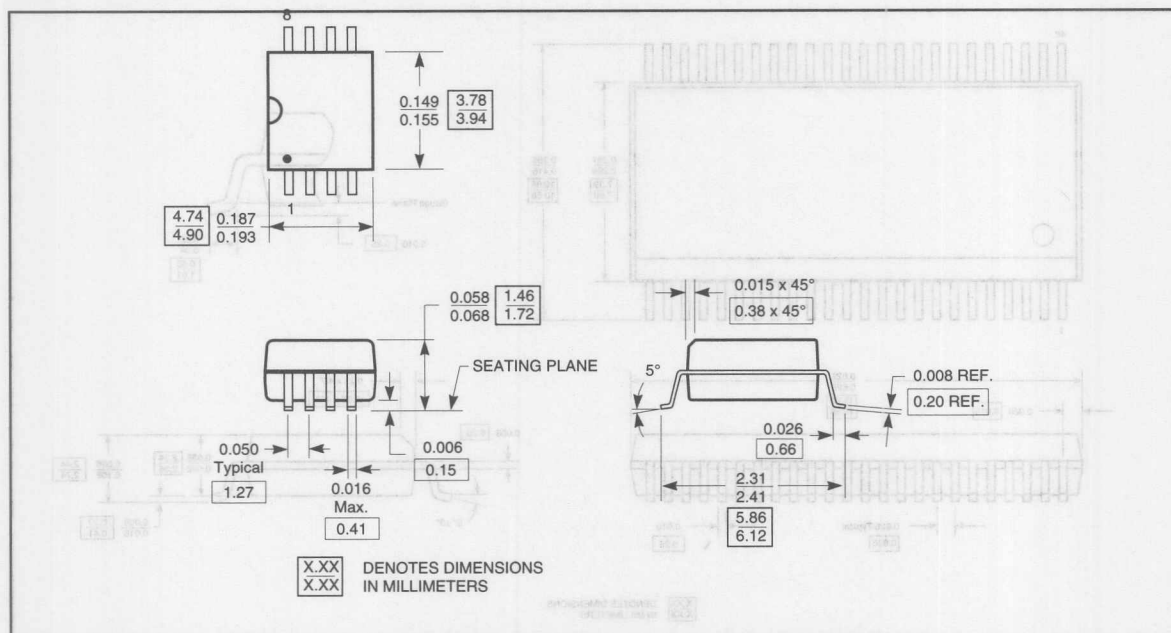
V48 — 48-Pin SSOP (300 Mil Wide)



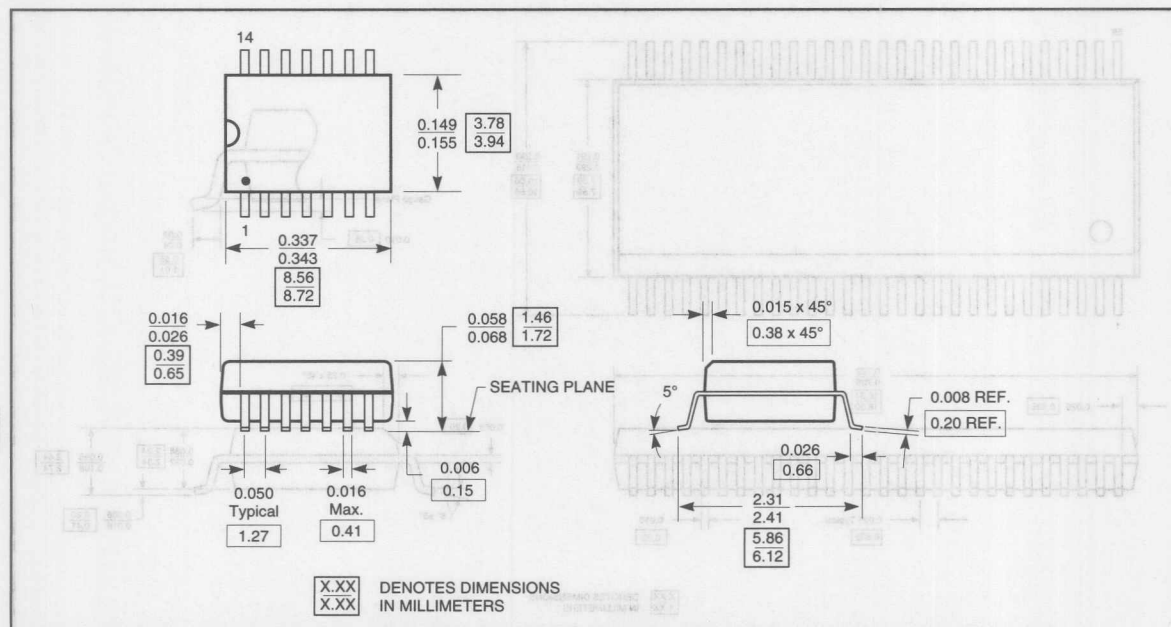
V56 — 56-Pin SSOP (300 Mil Wide)



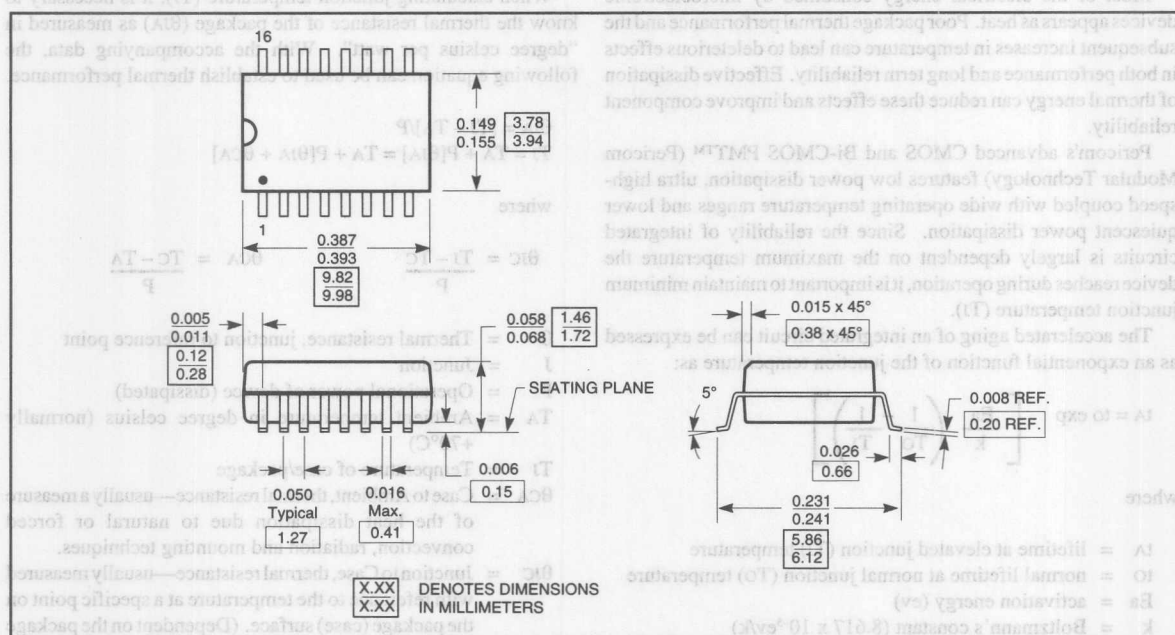
W8 — 8-Pin SOIC (150 Mil Wide)



W14 — 14-Pin SOIC (150 Mil Wide)



W16 — 16-Pin SOIC (150 Mil Wide)



THERMAL IMPEDANCE CALCULATIONS OF PERICOM'S PACKAGES

Most of the electrical energy consumed by microelectronic devices appears as heat. Poor package thermal performance and the subsequent increases in temperature can lead to deleterious effects in both performance and long term reliability. Effective dissipation of thermal energy can reduce these effects and improve component reliability.

Pericom's advanced CMOS and Bi-CMOS PMT™ (Pericom Modular Technology) features low power dissipation, ultra high-speed coupled with wide operating temperature ranges and lower quiescent power dissipation. Since the reliability of integrated circuits is largely dependent on the maximum temperature the device reaches during operation, it is important to maintain minimum junction temperature (T_J).

The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_0 \exp \left[\frac{E_a}{k} \left(\frac{1}{T_0} - \frac{1}{T_J} \right) \right]$$

where

- t_A = lifetime at elevated junction (T_J) temperature
- t_0 = normal lifetime at normal junction (T_0) temperature
- E_a = activation energy (ev)
- k = Boltzmann's constant (8.617×10^{-5} ev/k)

i.e., the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance.

$$\theta_{JA} = (T_J - T_A)/P$$

$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JA} + \theta_{CA}]$$

where

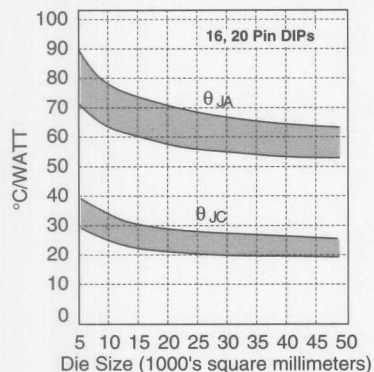
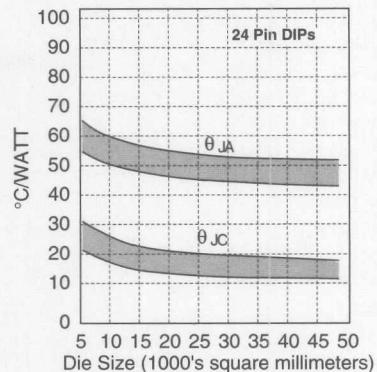
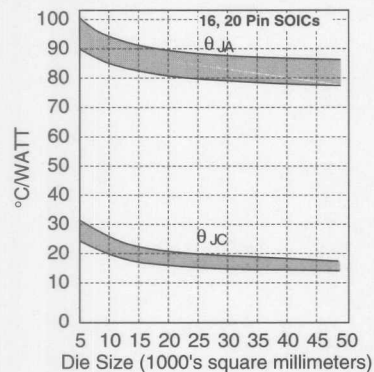
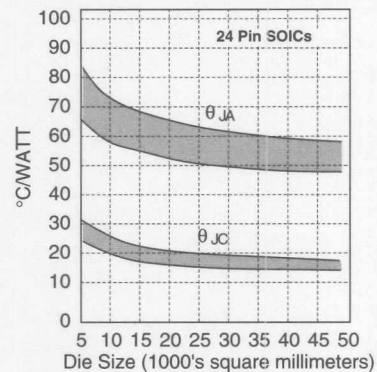
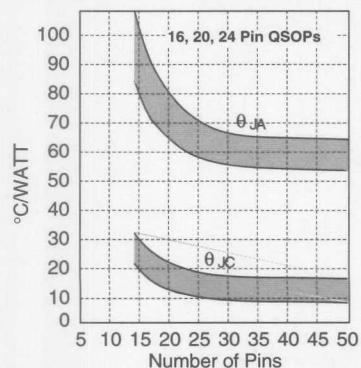
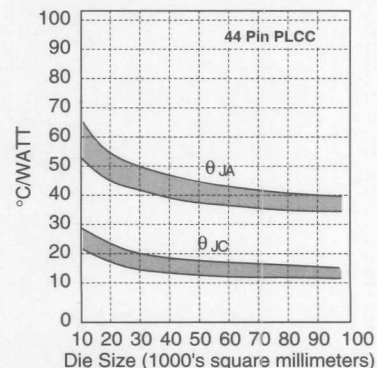
$$\theta_{JC} = \frac{T_J - T_C}{P}$$

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

- θ = Thermal resistance, junction to reference point
- J = Junction
- P = Operational power of device (dissipated)
- T_A = Ambient temperature in degree celsius (normally +70°C)
- T_J = Temperature of case/package
- θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
- θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
- θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on $\theta_{JC} + \theta_{JA}$ which includes the influence of area and environmental condition.)

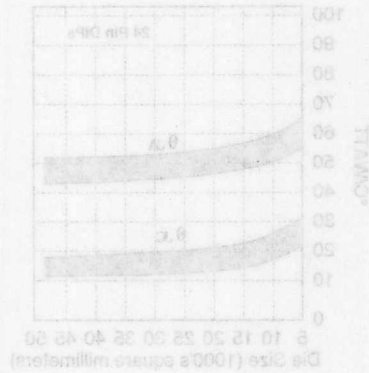
The following figures graphically illustrate the thermal values of Pericom's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package cavity size and die attach integrity. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

Thermal Impedance Measurements

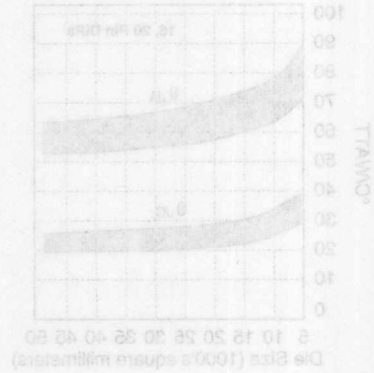
Thermal Resistance of Plastic DIP Packages

Thermal Resistance of Plastic DIP Packages

Thermal Resistance of Plastic SOIC Packages

Thermal Resistance of Plastic SOIC Packages

Thermal Resistance of Plastic QSOP Packages

Thermal Resistance of PLCC Package


Thermal Impedance Measurements

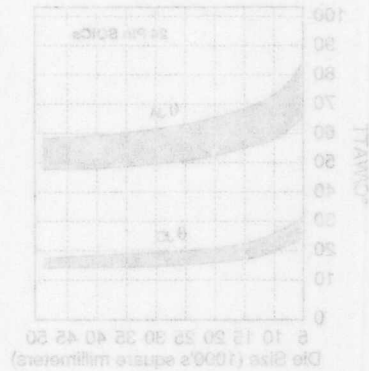
Thermal Resistance of Plastic DIP Packages



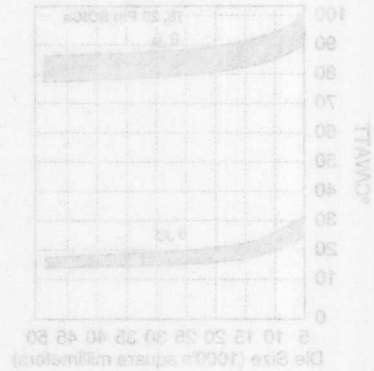
Thermal Resistance of Plastic DIP Packages



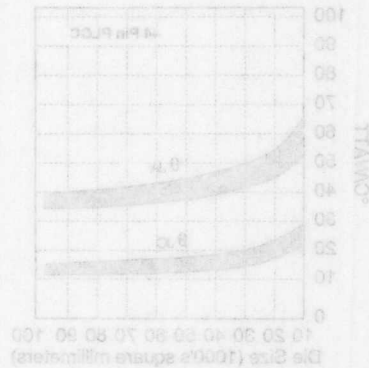
Thermal Resistance of Plastic SOIC Packages



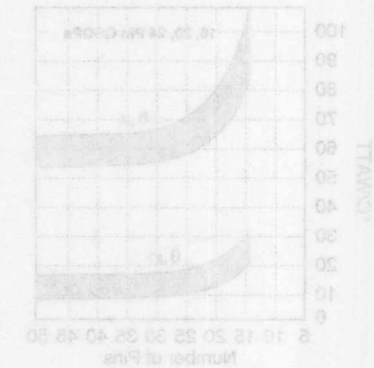
Thermal Resistance of Plastic SOIC Packages



Thermal Resistance of PLCC Packages



Thermal Resistance of Plastic QFP Packages



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